

Octal buffer/line driver with 5-volt tolerant inputs/outputs; 3-state

74LVC541A
74LVCH541A

FEATURES

- 5-volt tolerant inputs/outputs, for interfacing with 5-volt logic
- Supply voltage range of 2.7 to 3.6 V
- In accordance with JEDEC standard no. 8-1A.
- CMOS low power consumption
- Direct interface with TTL levels
- High impedance when $V_{CC}=0$ V
- Non-inverting outputs
- Bushold on all data inputs LVCH541A only).

GENERAL DESCRIPTION

The 74LVC(H)541A is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 V or 5 V devices. In 3-state operation, outputs can handle 5 V. This feature allows the use of these devices as translators in a mixed 3.3 V/5 V environment.

The 74LVC(H)541A is an octal non-inverting buffer/line driver with 5-volt tolerant inputs/outputs. The 3-state outputs are controlled by the output enable inputs $\overline{OE}1$ and $\overline{OE}2$.

A HIGH on $\overline{OEn}$ causes the outputs to assume a high impedance OFF-state.

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE}_1$	$\overline{OE}_2$	nA	nY
L	L	L	L
L	L	H	H
X	H	X	Z
H	X	X	Z

H = HIGH voltage level

L = LOW voltage level

X = don't care

Z = high impedance OFF-state

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25^\circ\text{C}$; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay A_n to Y_n	$C_L = 50$ pF $V_{CC} = 3.3$ V	3.8	ns
C_i	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	20	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz; C_L = output load capacity in pF;
 f_o = output frequency in MHz; V_{CC} = supply voltage in V;
 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is $V_i = \text{GND to } V_{CC}$

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC(H)541AD	20	SO	plastic	SOT163-1
74LVC(H)541ADB	20	SSOP	plastic	SOT339-1
74LVC(H)541APW	20	TSSOP	plastic	SOT360-1

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 19	$\overline{OE}_1, \overline{OE}_2$	output enable input (active LOW)
2, 3, 4, 5, 6, 7, 8, 9	A_0 to A_7	data inputs
10	GND	ground (0 V)
18, 17, 16, 15, 14, 13, 12, 11	Y_0 to Y_7	bus outputs
20	V_{CC}	positive supply voltage

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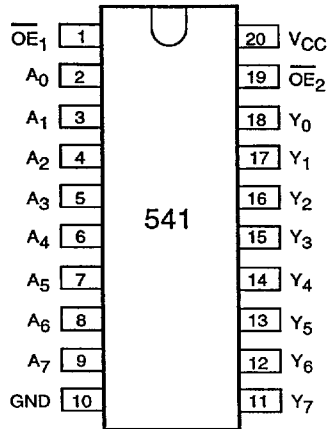


Fig.1 Pin configuration.

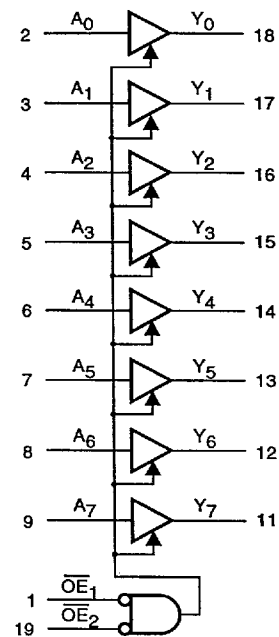


Fig.2 Logic symbol.

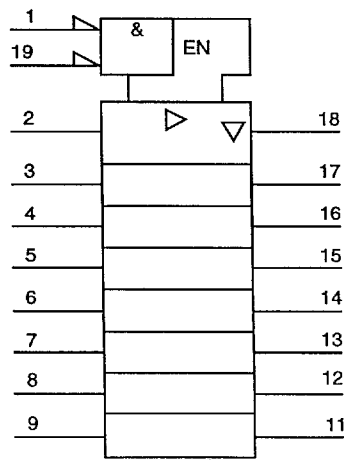


Fig.3 IEC logic symbol.

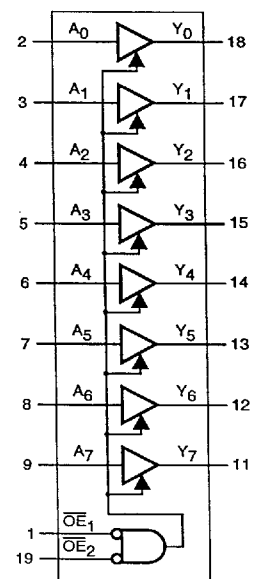


Fig.4 Functional diagram.

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DC CHARACTERISTICS FOR 74LVC(H)541A

For the DC characteristics see chapter "LVC(H)-A family characteristics", section "Family specifications".

I_{CC} category: MSI

AC CHARACTERISTICS FOR 74LVC(H)541A

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T _{amb} (°C)			UNIT	TEST CONDITIONS	
		-40 to +85				V _{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.			
t _{PHL} /t _{PLH}	propagation delay A _n to Y _n	—	—	—	ns	1.2	Figs 5, 7
		—	—	7.5		2.7	
		—	—	6.5		3.0 to 3.6	
t _{PZH} /t _{PZL}	3-state output enable time OE _n to Y _n	—	—	—	ns	1.2	Figs 5, 7
		—	—	9.5		2.7	
		—	—	8.5		3.0 to 3.6	
t _{PHZ} /t _{PLZ}	3-state output disable time OE _n to Y _n	—	—	—	ns	1.2	Figs 5, 7
		—	—	8.5		2.7	
		—	—	7.5		3.0 to 3.6	

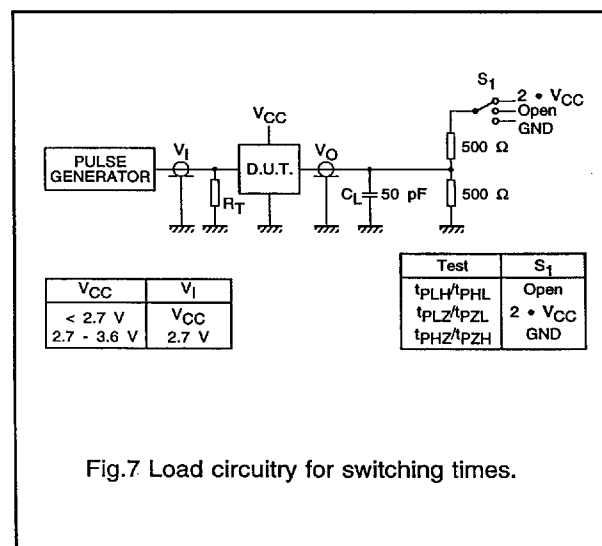
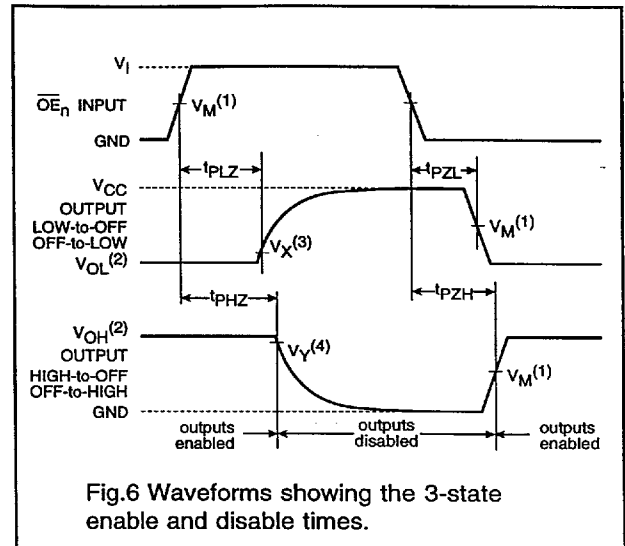
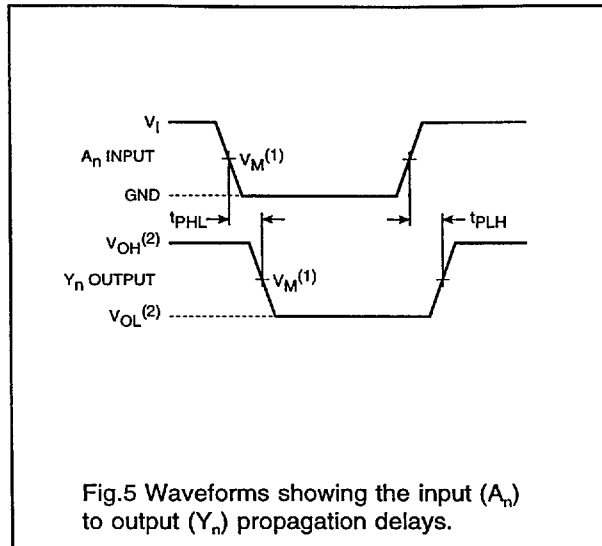
Notes: All typical values are measured at $T_{amb} = 25$ °C.

* Typical values are measured at $V_{CC} = 3.3$ V.

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AC WAVEFORMS



- Notes:
- (1) $V_M = 1.5 \text{ V}$ at $V_{CC} \geq 2.7 \text{ V}$
 $V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7 \text{ V}$
 - (2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load
 - (3) $V_X = V_{OL} + 0.3 \text{ V}$ at $V_{CC} \geq 2.7 \text{ V}$
 $V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7 \text{ V}$
 - (4) $V_Y = V_{OH} - 0.3 \text{ V}$ at $V_{CC} \geq 2.7 \text{ V}$
 $V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7 \text{ V}$