8. ELECTRICAL CHARACTERISTICS

Absolute Maximum Rating (T_a = 25°C)

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}		-0.3 to +7.0	V
Input voltage	V_I		-0.3 to V_{DD}+0.3	V
Output voltage	V_O		-0.3 to V_{DD}+0.3	V
High level output current	I_{OH}	Single pin	-17	mA
		All pins	-20	mA
Low level output current	I_{OL}	Single pin	17	mA
		All pins	55	mA
Operating temperature	T_{opt}		-10 to +70	°C
Storage temperature	T_{stg}		-65 to +150	°C

Capacitance (T_a = 25°C, V_{DD} = 0 V)

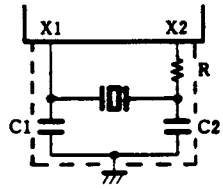
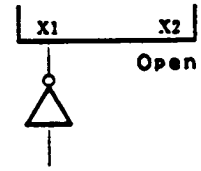
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz Unmeasured pins returned to 0 V			15	pF
Output capacitance	C_{OUT}				15	pF
I/O capacitance	C_{IO}				15	pF

Recommended Oscillation Constant for the System Clock Generator
(T_a = -10°C to +70°C)

Supply voltage range	Recommended oscillation constant	Frequency range (kHz)
4.5 V ≤ V_{DD} ≤ 6.0 V	R = 82 kΩ ±2% C = 33 pF ±5%, |Δ C/°C | ≤ 60 ppm	150 to 200 (*) to 250
2.7 V ≦ V_{DD} ≦ 3.3 V	R = 160 kΩ ±2% C = 33 pF ±5% |Δ C/°C | ≤ 60 ppm	75 to 100 to 120
2.7 V ≦ V_{DD} ≦ 6.0 V		75 to 135
2.5 V ≦ V_{DD} ≦ 3.3 V	R = 240 kΩ ±2% C = 33 pF ±5% | C/°C | ≤ 60 ppm	50 to 80
2.5 V ≦ V_{DD} ≦ 6.0 V		50 to 85

* V_{DD} = 5.0 V

Count Clock Oscillator Characteristics
(T_a = -10°C to + 70°C, V_{DD} = 2.5 to 6.0 V)

Resonator	Recommended constant	Parameter	Condition		MIN.	TYP.	MAX.	Unit
Resonant crystal		Oscillator frequency (f_{XX})			32	32.768	35	kHz
		Oscillation stabilization time	V_{DD}=4.5 to 6.0 V				2	s
							10	s
External clock		Input frequency (f_X)	duty =50%	V_{DD}=4.5 to 6.0 V	0		410	kHz
				V_{DD}=2.7 V	0		125	kHz
		X1 input rising/ falling time (t_{XR}, t_{XF})					0.2	us
		X1 input high/low level width (t_{XH}, t_{XL})	V_{DD}=4.5 to 6.0 V		1.2			us
			V_{DD}=2.7 V		4.0			us

Caution: When using a count clock generator, minimize the wiring within the broken lines to avoid effects such as stray capacitance. (For details, see Section 2.10)

Recommended Resonator for Count Clock: Resonant Crystal
(T_a = -10°C to +70°C)

Manufacturer	Product name	External capacitance			Oscillation voltage range (V)		Remarks
		C1(pf)	C2(pf)	R(kΩ)	MIN.	MAX.	
Kyocera Corp.	KF-38G	12	33	220	2.5	6.0	

Caution: Use a 30-pF trimmer capacitor as C1 for fine adjustment of the frequency of the resonant crystal.

DC Characteristics (T_a = -10°C to +70°C, V_{DD} = 2.7 to 6.0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High level input voltage (except for X1, CL1)	V_{IH1}		$0.7V_{DD}$		V_{DD}	V
High level input voltage (X1, CL1)	V_{IH2}		V_{DD}-0.5		V_{DD}	V
Low level input voltage (except for X1, CL1)	V_{IL1}		0		$0.3V_{DD}$	V
Low level input voltage (X1, CL1)	V_{IL2}		0		0.5	V
High level output voltage	V_{OH}	V_{DD}=4.5 to 6.0 V, I_{OH}=-1mA	V_{DD}-1.0			V
		I_{OH}=-100uA	V_{DD}-0.5			V
Low level output voltage	V_{OL}	V_{DD}=4.5 to 6.0 V, I_{OL}=1.6mA			0.4	V
		I_{OL}=400uA			0.5	V
High level input leakage current (except for X1, CL1)	I_{LIH1}	$V_{IN}=V_{DD}$			3	uA
High level input leakage current (X1, CL1)	I_{LIH2}				10	uA

(to be continued)

(Cont'd)

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Low level input leakage current (except for X1, CL1)	I_{LIL1}	V_{IN}=0 V				-3	uA
Low level input leakage current (X1, CL1)	I_{LIL2}					-10	uA
High level output leakage current	I_{LOH}	$V_{OUT}=V_{DD}$				3	uA
Low level output leakage current	I_{LOL}	V_{OUT}=0 V				-3	uA
Common output impedance	R_{COM}	(*) V_{DD}=4.5 to 6.0 V			3	5	kΩ
		(*)			5	15	kΩ
Segment output impedance	R_S	(*) V_{DD}=4.5 to 6.0 V			15	20	kΩ
		(*)			20	60	kΩ
Supply current	I_{DD1}	Opration mode	V_{DD}=5V±10% R=82kΩ±2% C=33pF±5%		300	900	uA
			V_{DD}=3V±10% R=160kΩ±2% C=33pF±5%		70	300	uA
	I_{DD2}	STOP mode X1=0V	V_{DD}=5 V ±10%		1	20	uA
			V_{DD}=3 V ±10%		0.3	10	uA
Built-in pull-up resistor	R_{L1}	Ports 1, 4, 5, 6	V_{DD}=5 V ±10%	15	40	70	kΩ
			V_{DD}=3 V ±10%	10	30	60	kΩ

* 2.7 V ≤ V_{LCD} ≤ V_{DD}

$$V_{LC1} = V_{DD} - \frac{1}{3}V_{LCD},\ V_{LC2} = V_{DD} - \frac{2}{3}V_{LCD},\ V_{LC3} = V_{DD} - V_{LCD}$$

AC Characteristics (T_a = -10°C to +70°C, V_{DD} = 2.7 to 6.0 V)

Parameter	Symbol	Condition			MIN.	TYP.	MAX.	Unit
System clock oscillator frequency (CL1, CL2)	f_{CC}	C=33pF ±5% |ΔC/°C| ≤ 60ppm	R=82kΩ ±2%,	V_{DD}=5V ±10%	150	200	240	kHz
			R=160kΩ ±2%	V_{DD}=3V ±10%	75	100	120	kHz
					75		135	kHz
System clock input frequency (CL1)	f_C	duty=50%	V_{DD}=4.5 to 6.0 V		10		410	kHz
			V_{DD}=2.7 V		10		125	kHz
CL1 input rising /falling time	t_{CR}, t_{CF}						0.2	us
CL1 input high/ low level width	t_{CH}, t_{CL}	V_{DD}=4.5 to 6.0 V			1.2		50	us
		V_{DD}=2.7 V			4.0		50	us
$\overline{SCK}$ cycle period	t_{KCY}	Input	V_{DD}=4.5 to 6.0 V		3.0			us
		Output			4.9			us
		Input			8.0			us
		Output			16.0			us
$\overline{SCK}$ high/low level width	t_{KH}, t_{KL}	Input	V_{DD}=4.5 to 6.0 V		1.3			us
		Output			2.2			us
		Input			4.0			us
		Output			8.0			us
SI setup time from $\overline{SCK}$↑	t_{SIK}				300			ns
SI hold time from $\overline{SCK}$↑	t_{KSI}				450			ns
$\overline{SCK}$↓→ SO output delay	t_{KSO}	V_{DD}=4.5 to 6.0 V					850	ns
							1200	ns
INT0 high/low level width	t_{I0H}, t_{I0L}				10			us
INT1 high/low level width	t_{I1H}, t_{I1L}				(*)			us
RESET high/low level width	t_{RSH}, t_{RSL}				10			us

* $\frac{2}{f_{CC}}$ or $\frac{2}{f_C}$

DC Characteristics (T_a = -10°C to +70°C, V_{DD} = 2.5 to 3.3 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High level input voltage (except for X1, CL1)	V_{IH1}		$0.8V_{DD}$		V_{DD}	V
High level input voltage (X1, CL1)	V_{IH2}		V_{DD}-0.3		V_{DD}	V
Low level input voltage (except for X1, CL1)	V_{IL1}		0		$0.2V_{DD}$	V
Low level input voltage (X1, CL1)	V_{IL2}		0		0.3	V
High level output voltage	V_{OH}	I_{OH}=-80 uA	V_{DD}-0.5			V
Low level output voltage	V_{OL}	I_{OL}=350 uA			0.5	V
High level input leakage current (except for X1, CL1)	I_{LIH1}	$V_{IN}=V_{DD}$			3	uA
High level input leakage current (X1, CL1)	I_{LIH2}	$V_{IN}=V_{DD}$			10	uA
Low level input leakage current (except for X1, CL1)	I_{LIL1}	V_{IN}=0 V			-3	uA
Low level input leakage current (X1, CL1)	I_{LIL2}	V_{IN}=0 V			-10	uA
High level output leakage current	I_{LOH}	$V_{OUT}=V_{DD}$			3	uA
Low level output leakage current	I_{LOL}	V_{OUT}=0 V			-3	uA
Supply current	I_{DD1}	Opration mode R=240kΩ ±2% C=33pF ±5%, V_{DD}=3V±10%		50	250	uA
		Opration mode R=240kΩ ±2% C=33pF ±5%, V_{DD}=2.5V		35	230	uA
	I_{DD2}	STOP mode X1=0V, V_{DD}=3 V ±10%		0.3	10	uA
		STOP mode X1=0V, V_{DD}=2.5 V		0.2	10	uA
Built-in pull-up resistor	R_{L1}	Ports 1, 4, 5, 6 V_{DD}=3 V ±10%	10	30	60	kΩ

AC Characteristics (T_a = -10°C to +70°C, V_{DD} = 2.5 to 3.3 V)

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
System clock oscillator frequency (CL1, CL2)	f_{CC}	R=240 kΩ ±2% C=33 pF ±5% IΔC/°CI ≤ 60 ppm		50		80	kHz
			V_{DD}=2.5 V	50	64	77	kHz
System clock input frequency (CL1)	f_C	duty=50%		10		80	kHz
CL1 input rising /falling time	t_{CR}, t_{CF}					0.2	us
CL1 input high/low level width	t_{CH}, t_{CL}			6.25		50	us
Count clock oscillator frequency (X1, X2)	f_{XX}	Crystal oscillation		25	32	50	kHz
Count clock input frequency (X1)	f_X	duty=50%		0		80	kHz
X1 input rising/falling time	t_{XR}, t_{XF}					0.2	us
X1 input high/low level width	t_{XH}, t_{XL}			6.25			us
$\overline{SCK}$ cycle period	t_{KCY}	Input		12.5			us
		Output		25			us
$\overline{SCK}$ high/low level width	t_{KH}, t_{KL}	Input		6.25			us
		Output		11.5			us
SI setup time from $\overline{SCK}$↑	t_{SIK}			1			ns
SI hold time from $\overline{SCK}$↑	t_{KSI}			1			ns
$\overline{SCK}$↑→ SO output delay	t_{KSO}					2	us
INT0 high/low level width	t_{I0H}, t_{I0L}			30			us
INT1 high/low level width	t_{I1H}, t_{I1L}			(*)			us
RESET high/low level width	t_{RSH}, t_{RSL}			30			us

* $\frac{2}{f_{CC}}$ or $\frac{2}{f_C}$

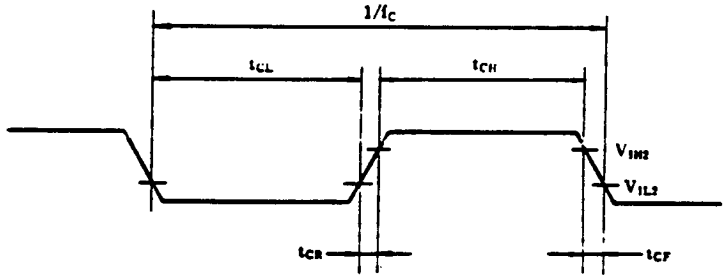
AC Timing Measurement Points (Except for X1, CL1)

(a) 2.7 V ≦ V_{DD} ≦ 6.0 V

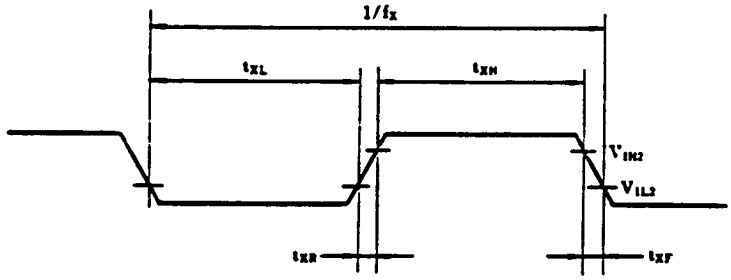
(b) 2.5 V ≦ V_{DD} < 2.7 V

Clock Timing

CL1 input



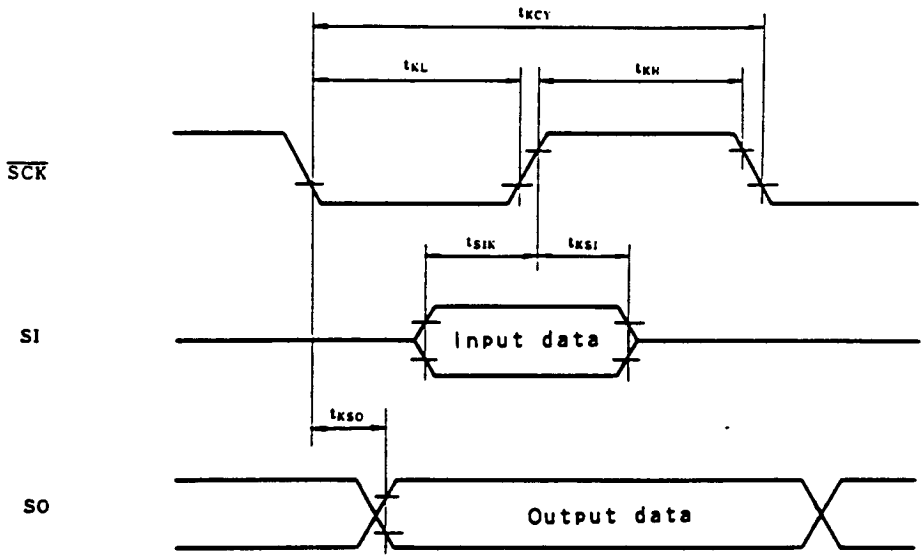
X1 input



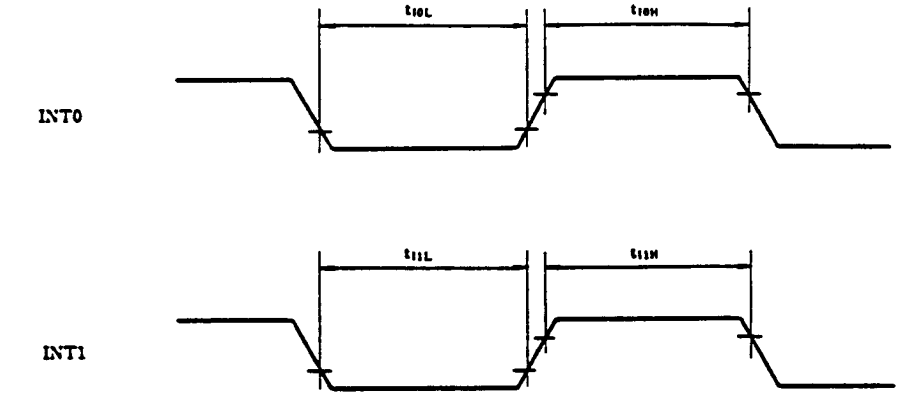
(a) 2.7 V≦V_{DD}≦6.0 V : V_{IH2}=V_{DD}−0.5 V, V_{IL2}=0.5 V

(b) 2.5 V≦V_{DD}<2.7 V : V_{IH2}=V_{DD}−0.3 V, V_{IL2}=0.3 V

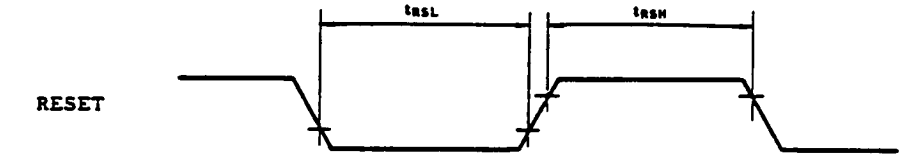
Serial Transfer Timing



Interrupt Timing



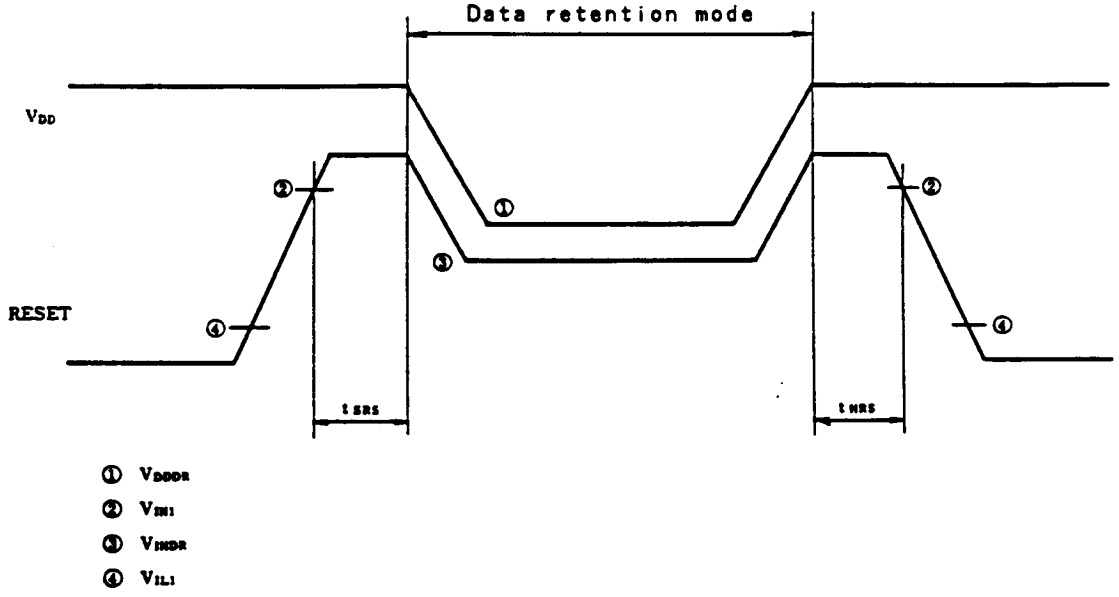
RESET Input Timing



Low Supply Voltage Data Retention Characteristics in Data Memory STOP Mode (T_a = -10°C to +70°C)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Data retention voltage	V_{DDDR}		2.0		6.0	V
Data retention current	I_{DDDR}	V_{DDDDR}=2.0 V		0.2	10	uA
Data retention high level RESET input voltage	V_{IHDR}		$0.9V_{DDDR}$		V_{DDDR}+0.2	V
RESET setup period	t_{SRS}		0			ns
RESET hold period	t_{HRS}		0			ns

Data Retention Timing



Caution: In the data retention mode, all inputs must be on V_{DDDR} or lower.