*PRELIMINARY INFORMATION [1] (SEE LAST PAGE)*

# Quad Programmable Precision Cascade Sequencer and Supervisory Controller with 4k-Bit Nonvolatile Memory

## FEATURES

- Operational from any of four Voltage Monitoring Inputs
- Programmable Power-up Cascade Sequencing
- Programmability allows monitoring any voltage between 0.6V and 5.6V with no external components
- Programmable 5mV steps in the low range
- Programmable Watchdog Timer
- Programmable Reset Pulse Width
- Programmable Nonvolatile Combinatorial Logic for generation of Reset
- Fault Status Register
- 4k-Bit Nonvolatile General Purpose Memory

**APPLICATIONS**

- Desktop/Notebook/Tablet Computers
- Multi-voltage Systems
- Telecom/Network Servers
- Portable Battery-powered Equipment
- Set-top Boxes
- Data-storage Equipment

## INTRODUCTION

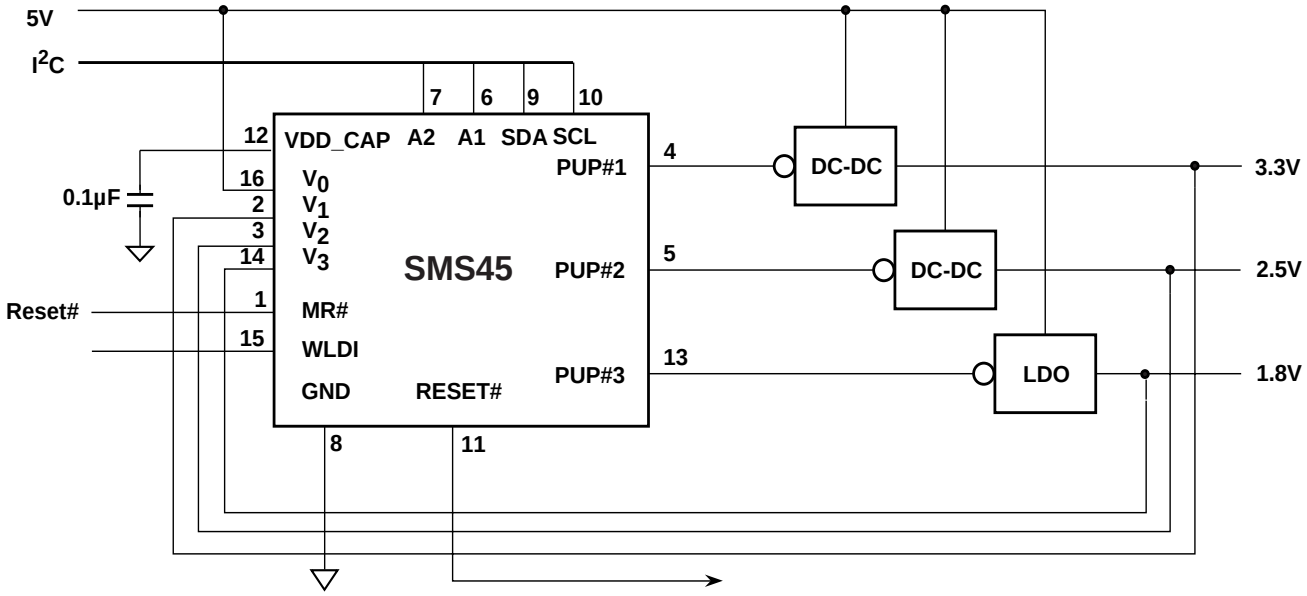
The SMS45 is a nonvolatile user-programmable voltage supply cascade sequencer and supervisory circuit designed specifically for advanced systems that need to monitor multiple voltages. The SMS45 can monitor four separate voltages without the need of any external voltage divider circuitry unlike other devices that need factory-trimmed threshold voltages and external components to accommodate different supply voltages and tolerances.

The SMS45 can also be used to enable DC/DC converters or LDOs to provide a closed loop cascading of the supplies during power-up.

The SMS45 watchdog timer has a user programmable time-out period and it can be placed in an idle mode for system initialization or system debug. All of the functions are user accessible through an industry standard $I^2C$ 2-wire serial interface.

Programming of configuration, control and calibration values by the user is simplified with the SMX3200 interface adapter and Windows GUI software obtainable from Summit Microelectronics.

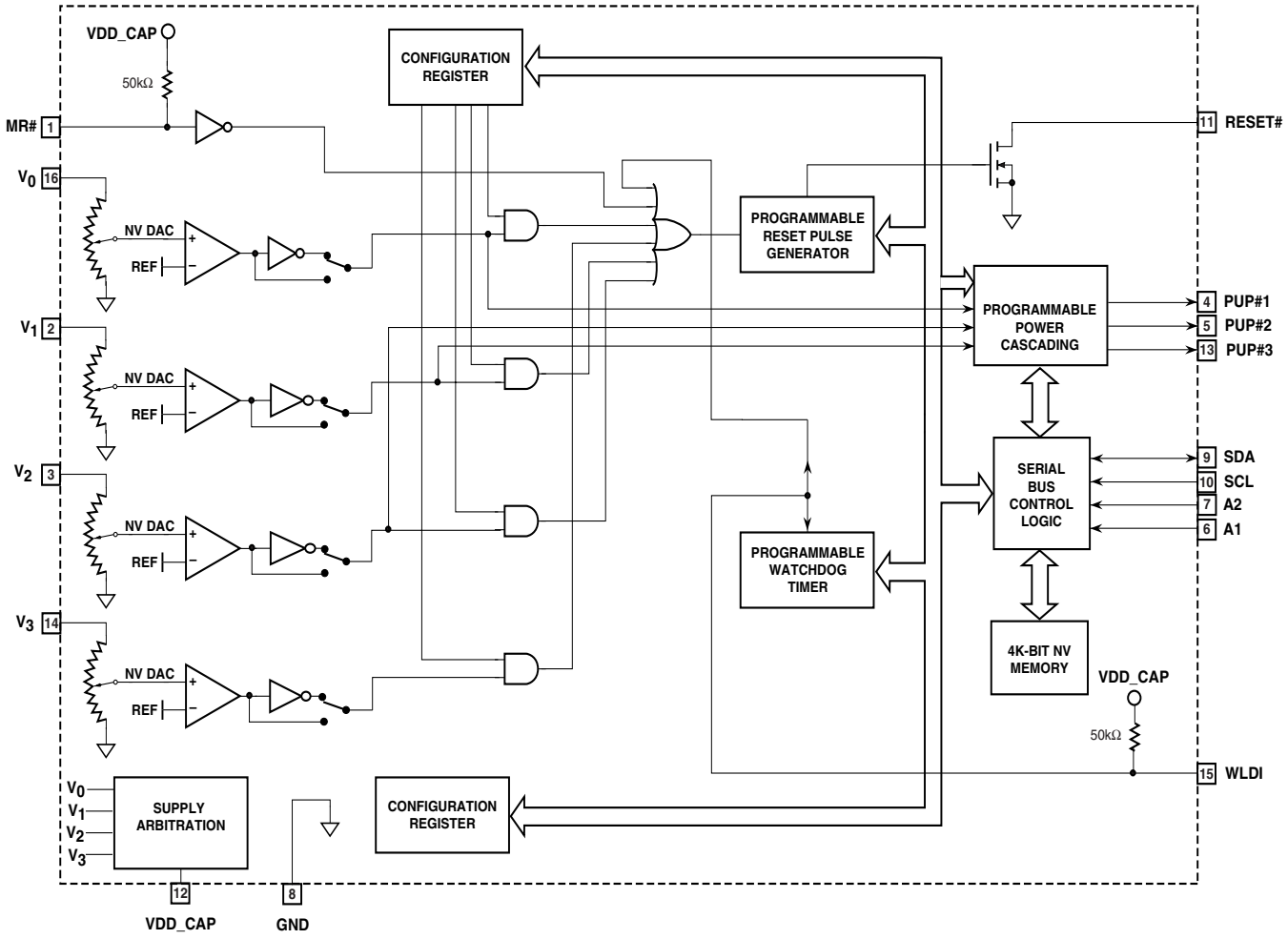
## SIMPLIFIED APPLICATION DRAWING




**Applications Schematic using the SMS45 Controller to provide closed loop power-up cascade sequencing and supervisory functions.**

NOTE: THIS IS AN APPLICATIONS EXAMPLE ONLY. SOME PINS, COMPONENTS AND VALUES ARE NOT SHOWN.

## INTERNAL BLOCK DIAGRAM




## CASCADE SEQUENCING

Time based sequencing has the ability to turn supplies on in a specific order. However, it cannot guarantee that each supply has reached valid voltage levels before the next supply is sequenced on. Cascade sequencing guarantees the supplies are enabled a programmed period of time after the previous voltage has reached its minimum programmed valid level. Figure 1 shows that each succeeding voltage must reach its minimum valid level before the timer is started to time the interval, ***t***, for the next voltage. The duration of each ***t*** is programmable for each supply to supply transition. The next supply is not enabled until the timer has elapsed. See also Figure 5.

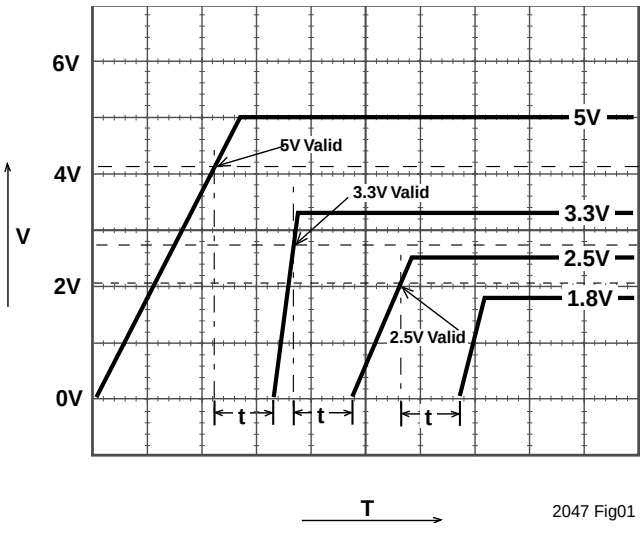
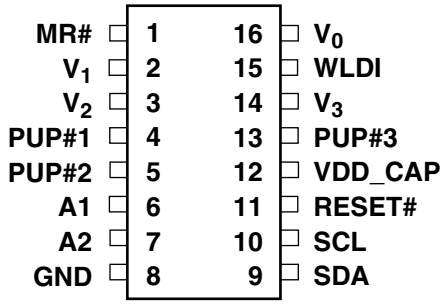



**Figure 1. Cascading Power Supplies**

## PIN CONFIGURATION




2047 PCon 2.0

## PIN NAMES

| Pin | Name | Function |
|---|---|---|
| 1 | MR# | Manual reset input |
| 2 | $V_1$ | Voltage supply and monitor input |
| 3 | $V_2$ | Voltage supply and monitor input |
| 4 | PUP#1 | Power up permitted output |
| 5 | PUP#2 | Power up permitted output |
| 6 | A1 | Address input |
| 7 | A2 | Address input |
| 8 | GND | Power supply return |
| 9 | SDA | Serial data I/O |
| 10 | SCL | Serial data clock |
| 11 | RESET# | Reset out |
| 12 | VDD_CAP | Power supply output |
| 13 | PUP#3 | Power up permitted |
| 14 | $V_3$ | Voltage supply and monitor input |
| 15 | WLDI | Watchdog Timer interrupt |
| 16 | $V_0$ | Voltage supply and monitor input |

2047 Pins Table 2.0

## ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... –55°C to 125°C
Storage Temperature ..... –65°C to 150°C
Lead Solder Temperature (10s) ..... 300 °C
Terminal Voltage with Respect to GND:
$V_0$, $V_1$, $V_2$, and $V_3$ ..... –0.3V to 6.0V
All Others ..... –0.3V to 6.0V
Junction Temperature.....150°C
ESD Rating per JEDEC.....2000V
Latch-Up testing per JEDEC.....±100mA

***Note** - Stresses beyond the listed Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

## RECOMMENDED OPERATING CONDITIONS

Industrial Temperature Range..... –40ºC to +85ºC.
Commercial Temperature Range.....–5ºC to +70ºC.
$V_{SUPPLY}$ Supply Voltage.....2.7V to 5.5V

$V_{SUPPLY}$ = Device supply voltage provided by the highest $V_X$ input.

Package Thermal Resistance (θJA)
16 Lead SSOP.....23ºC/W
Moisture Classification Level 1 (MSL 1) per J-STD- 020

### RELIABILITY CHARACTERISTICS

Data Retention.....100 Years
Endurance.....100,000 Cycles

## DC OPERATING CHARACTERISTICS

(**Over Recommended Operating Conditions; Voltages are relative to GND**)

| Symbol | Parameter | Notes | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{SUPPLY}$ | Operating supply voltage | 1V Min. refers to a valid reset output being generated | 1.0 | | 5.5 | V |
| | | Memory read/write operations: at least one of the $V_X$ inputs must be at or above $V_{SUPPLY}$ min. | 2.7 | | 5.5 | V |
| $I_{CC}$ | Supply current | VDD_CAP = 5.5V; $V_0$ trip point 4.7V; $V_1$, $V_2$, $V_3$ = GND; MR# = $V_{CC}$; all outputs floating | | 200 | 400 | µA |
| | | Configuration register or memory access | | | 3 | mA |
| $V_{PTH}$ Range | Programmable threshold range (low range) | Reset threshold voltage range $V_0$ to $V_3$ (5mV increments) | 0.6 | | 1.875 | V |
| $V_{PTH}$ Range | Programmable threshold range (high range) | Reset threshold voltage range $V_0$ to $V_3$ (15mV increments) | 1.8 | | 5.625 | V |
| $V_{PTHACC}$ | Programmable threshold Accuracy | $V_{PTH}$ is the programmed threshold setpoint within the $V_{PTH}$ Range | –1.0 | $V_{PTH}$ | 1.0 | % |
| $V_{HYST}$ | $V_{RST}$ hysteresis | See Note 1 below | | 30 | | mV |
| $V_{OL}$ | Low voltage output | $I_{SINK}$ = 1mA, $V_{VDD\_CAP} \geq$ 2.7V | | | 0.3 | V |
| | | $I_{SINK}$ = 200µA, $V_{VDD\_CAP}$ = 1.0V | | | 0.3 | V |
| $V_{IL}$ | Input threshold | | | | 0.6 | V |
| $V_{IH}$ | | | $0.7 \times V_{CC}$ | | | V |

Note 1: Low Range Hysteresis = 4.2 X (Vtrip - 0.5 volts) mV. For Vtrip = 1.0 volts, Hysteresis = 2.1 mV (0.21 %),
High Range Hysteresis = 12.6 X (Vtrip -0.5 volts) mV. For Vtrip = 5.0 volts, Hysteresis = 56.7 mV (1.13%).

## AC OPERATING CHARACTERISTICS

(**Over Recommended Operating Conditions; Voltages are relative to GND, also see configuration registers**)

| Symbol | Parameter | Notes | | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|---|
| $t_{PWDTO}$ | Programmable Watchdog timer period | WD2 | WD1 | WD0 | | | | |
| | | 0 | 0 | X | | OFF | | — |
| | | 0 | 1 | 1 | 300 | 400 | 500 | ms |
| | | 1 | 0 | 0 | 600 | 800 | 1000 | |
| | | 1 | 0 | 1 | 1200 | 1600 | 2000 | |
| | | 1 | 1 | 0 | 2400 | 3200 | 4000 | |
| | | 1 | 1 | 1 | 4800 | 6400 | 8000 | |
| $t_{PDLY}X$ | Programmable delay from $V_{PTH}$ to PUP# out | | PUP#X-1 | PUP#X-0 | | | | |
| | | | 0 | 0 | | 0ms | | — |
| | | | 0 | 1 | 19 | 25 | 31 | ms |
| | | | 1 | 0 | 38 | 50 | 63 | |
| | | | 1 | 1 | 75 | 100 | 125 | |
| $I_{MR}$ | MR# pullup current | | | | | 100 | | µA |
| $T_{MR}$ | MR# input pulse width | Minimum | | | | 300 | | ns |
| $T_{DMRRST}$ | Delay from MR# low to RESET# low | | | | | 200 | | ns |
| $t_{PRTO}$ | Programmable reset pulse width | | RTO1 | RTO0 | | | | |
| | | | 0 | 0 | 19 | 25 | 31 | ms |
| | | | 0 | 1 | 38 | 50 | 63 | ms |
| | | | 1 | 0 | 75 | 100 | 125 | ms |
| | | | 1 | 1 | 150 | 200 | 250 | ms |
| $t_{DRST}$ | V in to RESET# delay | 100mV overdrive | | | | 20 | | µs |

## PIN DESCRIPTIONS

**$V_0$, $V_1$, $V_2$, $V_3$ (16, 2, 3, 14)**

These inputs are used as the voltage monitor inputs and as the voltage supply for the SMS45. Internally they are diode ORed and the input with the highest voltage potential will be the default supply voltage (VDD_CAP).

The RESET# output will be valid if any one of the four inputs is above 1V. However, for full device operation at least one of the inputs must be at 2.7V or higher.

The sensing threshold for each input is independently programmable in 5mV increments from 0.6V to 1.875V or 15mV increments from 1.8V to 5.625V. Also, the occurrence of an under- or over-voltage condition that is detected as a result of the threshold setting can be used to generate a RESET#. The programmable nature of the threshold voltage eliminates the need for external voltage divider networks.

**GND**

Power supply return.

**MR# (1)**

The manual reset input always generates a RESET# output whenever it is driven low. The duration of the RESET# output pulse will be initiated when MR# goes low and it will stay low for the duration of MR# low plus the programmed reset time-out period ($t_{PRTO}$). If MR# is brought low during a power-on cascade of the PUP#s the cascade will be halted for the reset duration, and will then resume from the point at which it was interrupted. MR# must be held low during a configuration register write. This signal is pulled up internally through a 50kΩ resistor.

**RESET# (11)**

The reset output is an active low open drain output. It will be driven low whenever the MR# input is low or whenever an enabled under-voltage or over-voltage condition exists. The four voltage monitor inputs are always functioning, but their ability to generate a reset is programmable (**configuration register 4**). Refer to Figures 2 and 3 for a detailed illustration of the relationship between MR#, RESET# and the $V_{IN}$ levels.

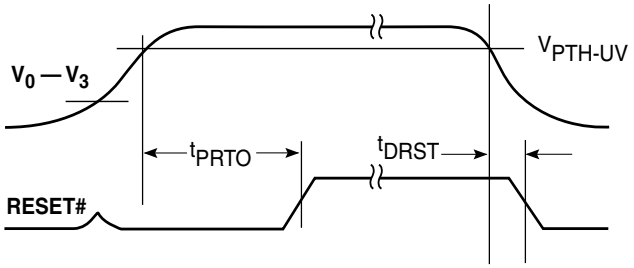



**Figure 3. RESET# Timing**

**VDD_CAP (12)**

The VDD_CAP pin connects to the internal supply voltage for the SMS45. A capacitor is placed on this pin to filter supply noise as well as hold up the device in the event of power failure. The voltage on this node is determined by the highest input voltage. Loading of this pin should be minimized to prevent excessive power dissipation in the part.

**WLDI (15)**

Watchdog timer input. A high-to-low transition on the WLDI input will clear the watchdog timer, effectively starting a new time-out period. This signal is pulled up internally through a 50kΩ resistor.

If WLDI is stuck low and no high-to-low transition is received within the programmed $t_{PWDTO}$ period (programmed watchdog time-out) RESET# will be driven low. Refer to Figure 4 for a detailed illustration.

Holding WLDI low will not block the watchdog from timing out and generating a reset. Refer to Figure 4 for a detailed illustration of the relationship between RESET# and WLDI.

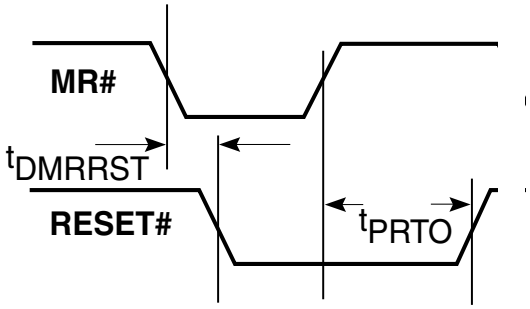



**Figure 2. RESET# Timing with MR#**

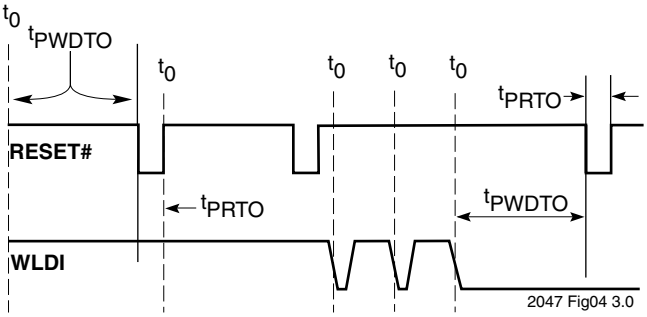



**Figure 4. Watchdog and WLDI Timing**

## PIN DESCRIPTIONS (CONTINUED)

**A1,A2 (6, 7)**

A1 and A2 are the address inputs. When addressing the SMS45 memory or configuration registers the address inputs distinguish which one of four possible devices sharing the common bus is being addressed.

**SDA (9)**

SDA is the serial data input/output pin. It should be tied to VDD_CAP through a pull-up resistor.

**SCL (10)**

SCL is the serial clock input. It should be tied to VDD_CAP through a pull-up resistor.

**PUP#1, PUP#2, PUP#3 (4, 5, 13)**

These are the power-up permitted (PUP) active low open drain outputs. The PUP pins are used when the SMS45 is programmed to provide the cascade sequencing of LDOs or DC/DC converters (***see Figures 1 and 5 for illustrations of cascading***). Each delay is independently enabled and programmable for its duration (**configuration register 7**). If all PUP# outputs are enabled the order of events would be as follows: $V_0$ above threshold then delay to PUP#1 turning on; $V_1$ above threshold then delay to PUP#2 turning on; $V_2$ above threshold then delay to PUP#3 turning on. The delays are programmable.

## DEVICE OPERATION

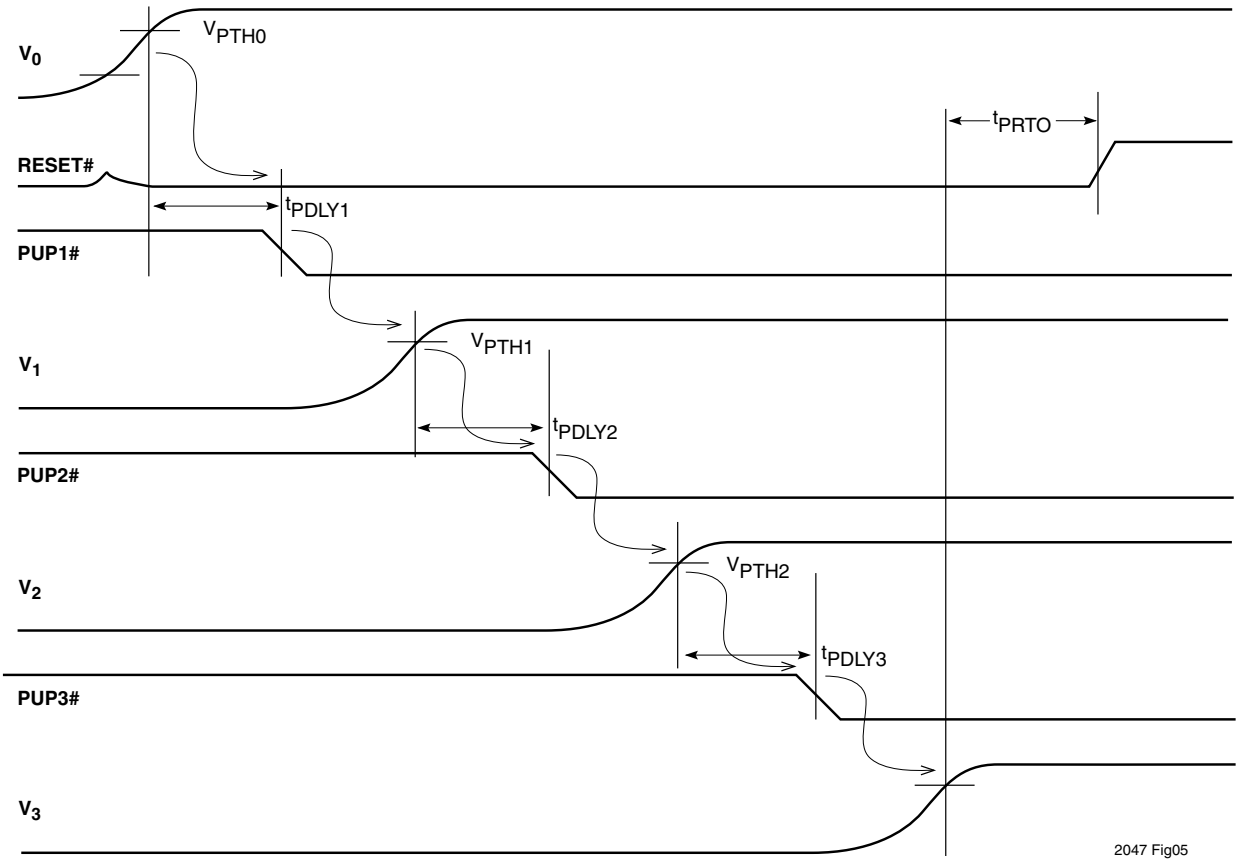



**Figure 5. $V_x$ Input and Resulting PUP# Cascade (RESET# set to trip on $V_3$ Undervoltage)**

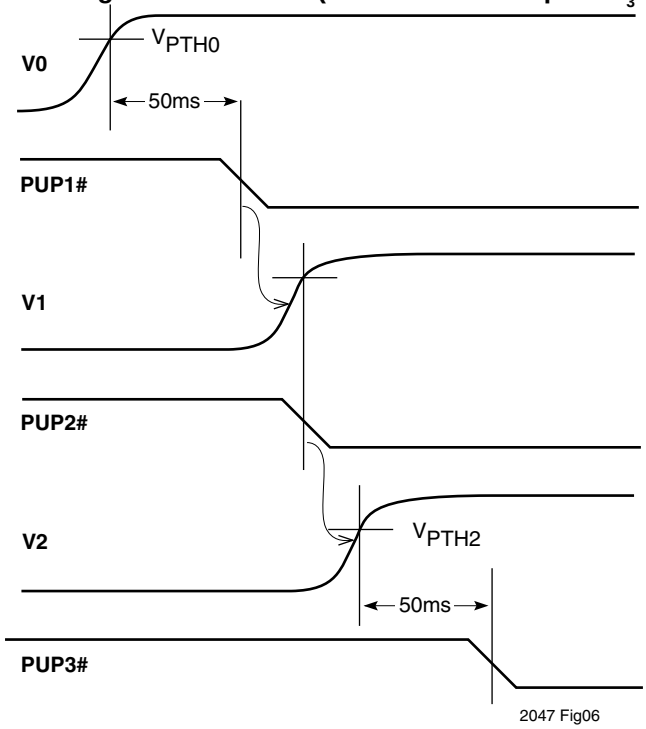



**Figure 6. Timing with Register 7 Contents $22_{HEX}$**

## DEVICE OPERATION (CONTINUED)

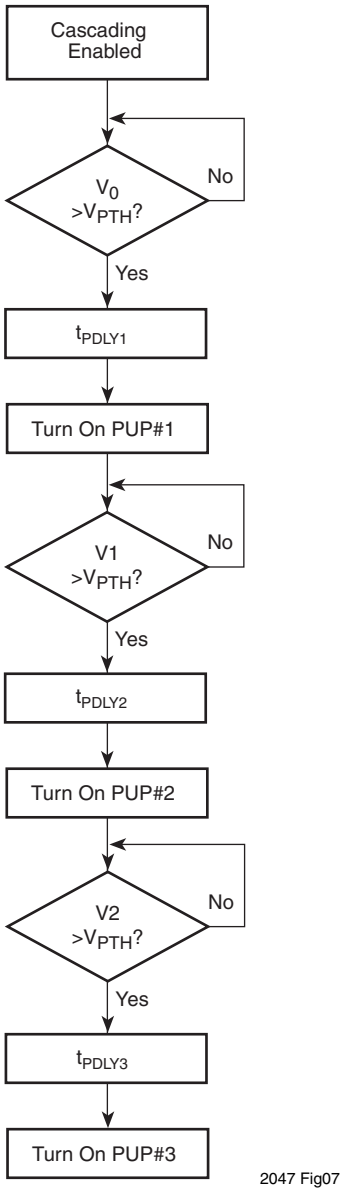



**Figure 7. Cascade Flow Chart**

## CONFIGURATION REGISTERS

### SUPPLY AND MONITOR FUNCTIONS

The $V_0$, $V_1$, $V_2$, and $V_3$ inputs are internally diode-ORed so that any one of the four can act as the device supply. The RESET# output will be guaranteed true so long as one of the four pins is at or above 1V.

> **Note***: for performing a memory operation (Read or Write) and to have the ability to change configuration register contents at least one supply input must be above 2.7V.*

Read/Write operations require a 0.1µF capacitor from the VDD_CAP node to GND. For optimum performance connect capacitors from each of the Vx inputs to GND. Locate the capacitors as physically close to the SMS45 as possible.

If cascading is enabled, the designer must insure $V_0$ is the primary supply and is the first to become active.

Associated with each input is a comparator with a programmable threshold for detection of under-voltage or over-voltage conditions on any of the four supply inputs. The threshold can be programmed in 5mV increments anywhere within the range of 0.6V to 1.875V or 15mV increments within the range of 1.8V to 5.625V. Configuration registers 0, 1, 2, and 3 adjust the thresholds for $V_0$, $V_1$, $V_2$, and $V_3$ respectively.

If the value contained in any register is all zeroes, the corresponding threshold will be 0.6V. If the contents were low range $05_{HEX}$ the threshold would then be 0.625V [0.6V + (5 × 0.005V)]. All four registers are configured as 8-Bit registers.

| D7 MSB | D6 | D5 | D4 | D3 | D2 | D1 | D0 LSB | Action |
|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | Highest threshold adjustment = 5.625V (High Range) |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Lowest threshold adjustment = 0.6V (Low Range) |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | Threshold = 0.6V + (6×0.005V) = 0.625V *(e.g.)* |

**Table 1. Configuration Registers 0, 1, 2, and 3**

### RESET FUNCTION AND THRESHOLD RANGE

The reset output has four programmable sources for activation. Configuration register 4 is used for selecting the activation source (D7:4), which can be any combination of $V_0$, $V_1$, $V_2$ and $V_3$. A monitor input can be programmed to activate on either an under-voltage or over-voltage condition. The low-order four bits of configuration register 5 program these options. The reset threshold voltage range for V0 to V3 can be set for 5mV increments below 1.875V (low Range = "0") or for 15mV increments above 1.8V (high range = "1") using Bits D3:0.

The RESET# output will become active when triggered by a selected activation source such as an under-voltage condition on V1. When this condition ceases, the RESET# output will remain active for $t_{PRTO}$ (programmable reset time-out). This reset time-out interval takes priority over the PUP outputs for use of the timer.

The RESET# output has two hardwired sources for activation: the MR# input, and the expiration of the Watchdog timer. RESET# will remain active so long as MR# is low, and will continue driving the RESET# output for $t_{PRTO}$ (programmable reset time out) after MR# returns high. The MR# input cannot be bypassed or disabled.

Refer to Figures 2, 3 and 4 for a detailed illustration of the relationships among the affected signals.

| D7 MSB | D6 | D5 | D4 | D3 | D2 | D1 | D0 LSB | Action |
|---|---|---|---|---|---|---|---|---|
| X | X | X | X | $V_3$ | $V_2$ | $V_1$ | $V_0$ | |
| RESET Trigger Enable | | | | Voltage Threshold Range Select | | | | |
| | | | | 0 | 0 | 0 | 0 | Low Range |
| | | | | 1 | 1 | 1 | 1 | High Range |

**Table 2. Configuration Register 4**

The status of the four supplies is available at any time over the $I^2C$ bus in the high order configuration bits of register 5 (Table 3). A "1" in a bit location indicates a fault on that supply.

## CONFIGURATION REGISTERS (CONTINUED)

| Action | D3 MSB | D2 | D1 | D0 LSB |
|---|---|---|---|---|
| | $V_3$ | $V_2$ | $V_1$ | $V_0$ |
| Writing a 0 enables undervoltage detection for the selected V input | 0 | 0 | 0 | 0 |
| Writing a 1 enables overvoltage detection for the selected V input | 1 | 1 | 1 | 1 |

**Table 3. Configuration Register 5 (D0 through D3)**

### WATCHDOG TIMER

The Watchdog Timer will generate a reset if it times out. It can be cleared by a high-to-low transition on WLDI and restarted.

If the Watchdog times out RESET# will be driven low until $t_{PRTO}$ at which time it will return high. Refer to Figure 4 which illustrates the action of RESET# with respect to the Watchdog timer and the WLDI input.

If WLDI is held low the timer will free-run generating a series of resets.

| D7 MSB | D6 | D5 | D4 LSB | Action |
|---|---|---|---|---|
| $V_3$ | $V_2$ | $V_1$ | $V_0$ | |
| 0 | 0 | 0 | 0 | Reading a 1 indicates a supply fault |
| 1 | 1 | 1 | 1 | |

**Table 4. Configuration Register 5 (D4 through D7)**

When the Watchdog times out RESET# will be generated. When RESET# returns high (after $t_{PRTO}$) the timer is reset to time zero.

Register 6 is also used to set the programmable reset time-out period ($t_{PRTO}$) and to select the cascade option.

#### Cascade Delay Programming

The cascade delays are programmed in register 7. Bit 7 of register 6 must be set to a 0 in order to enable the cascading of the PUP# outputs. Cascading will not commence until $V_0$ is above its programmed threshold.

Each PUP# (-3, -2 and -1) is delayed according to the states of its Bit 1 and Bit 0 as indicated in Table 9. Refer to Figures 1 and 5 for the detailed timing relationship of the programmable power-on cascading.

| D7 MSB | D6 | D5 | D4 | D3 | Action |
|---|---|---|---|---|---|
| Read[1] Only | RTO1 | RTO0 | Read Only | Read Only | |
| 0 | 0 | 0 | x | x | $t_{PRTO}$ = 25ms |
| 0 | 0 | 1 | x | x | $t_{PRTO}$ = 50ms |
| 0 | 1 | 0 | x | x | $t_{PRTO}$ = 100ms |
| 0 | 1 | 1 | x | x | $t_{PRTO}$ = 200ms |

**Table 5. Configuration Register 6 (D3 through D7)**
**Note 1 - Read Only bit D7 is set to a 0. Read only bits D4 and D3 are revision control and the value indicates the status code of the device (ie. 01 is status code 1).**

| Action | D2 | D1 | D0 LSB |
|---|---|---|---|
| | WD2 | WD1 | WD0 |
| OFF | 0 | 0 | 0 |
| 400ms | 0 | 1 | 1 |
| 800ms | 1 | 0 | 0 |
| 1600ms | 1 | 0 | 1 |
| 3200ms | 1 | 1 | 0 |
| 6400ms | 1 | 1 | 1 |

**Table 6. Configuration Register 6 (D0, D1, D2)**

The delay from $V_{PTH0}$ until PUP#1 low is $t_{PDLY1}$. There is a similar $t_{PDLYX}$ delay for V1 to PUP#2 and for V2 to PUP#3. They are programmed in register 7. Cascading will always occur as indicated in the flow chart (Figure 7).

## CONFIGURATION REGISTERS (CONTINUED)

| D7 MSB | D6 | Action |
|---|---|---|
| Address Select | | |
| Lock | AS0 | |
| x | 0 | DTI = 1010, responds only when address bits = A2 & A1 logic states |
| x | 1 | DTI = 1011, responds only when address bits = A2 & A1 logic states |
| 0 | x | Config. Reg. Read/Write enabled |
| 1 | x | Config. Reg. Read/Write locked out [1] |

2047 Table07 3.0

Note 1 - Setting this bit will cause a permanent Read/Write Lock out.

**Table 7. Configuration Register 7 (D7, D6)**

| D5 | D4 | D3 | D2 | D1 | D0 LSB |
|---|---|---|---|---|---|
| PUP#3 | | PUP#2 | | PUP#1 | |
| Bit 1 | Bit 0 | Bit 1 | Bit 0 | Bit 1 | Bit 0 |

2047 Table08 3.0

**Table 8. Configuration Register 7 (D5 through D0)**

| Bit 1 | Bit 0 | $t_{PDLYX}$ |
|---|---|---|
| 0 | 0 | 0ms (no) Delay |
| 0 | 1 | 25ms Delay |
| 1 | 0 | 50ms Delay |
| 1 | 1 | 100ms Delay |

2047 Table09 1.0

**Table 9. PUP Delays, Configuration Register 7**

## DEVELOPMENT HARDWARE & SOFTWARE

### SMX3200 PROGRAMMER

The end user can use the summit SMX3200 programming cable and software that have been developed to operate with a standard personal computer. The programming cable interfaces directly between a PC's parallel port and the target application. The application's values are entered via an intuitive graphical user interface employing drop-down menus.

The latest revisions of all software and an application brief describing the SMX3200 is available from the website (www.summitmicro.com).

The Windows GUI software will generate the data and send it in $I^2C$ serial bus format so that it can be directly downloaded to the SMS45 via the programming Dongle and cable. An example of the connection interface is shown in Figure 8.

When design prototyping is complete, the software can generate a HEX data file that should be transmitted to Summit for approval. Summit will then assign a unique customer ID to the HEX code and program production devices before the final electrical test operations. This will ensure proper device operation in the end application.

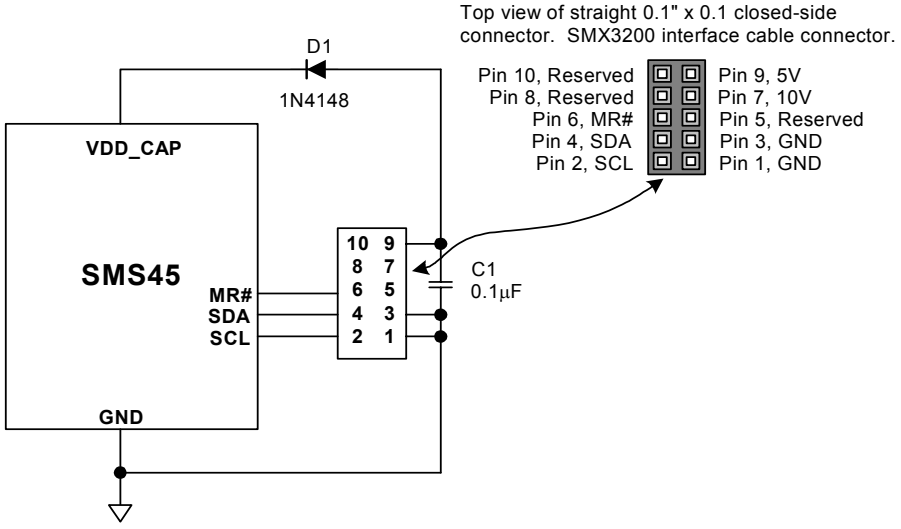



**Figure 8. SMX3200 Programmer $I^2C$ serial bus connections to program the SMS45.**

## I²C PROGRAMMING INFORMATION

### MEMORY OPERATION

Data for the configuration registers and the memory array are read and written via an industry standard two-wire interface. The bus was designed for two-way, two-line serial communication between different integrated circuits. The two lines are a serial data line (SDA) and a serial clock line (SCL). The SDA line must be connected to a positive supply by a pull-up resistor, located somewhere on the bus. See Memory Operating Characteristics: Table 10 and Figure 9.

### Input Data Protocol

The protocol defines any device that sends data onto the bus as a transmitter and any device that receives data as a receiver. The device controlling data transmission is called the Master and the controlled device is called the Slave. In all cases the SMS45 will be a Slave device, since it never initiates any data transfers.

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during clock high time because changes on the data line while SCL is high will be interpreted as start or stop condition.

| Symbol | Parameter | Conditions | MIN | TYP | MAX | Units |
|---|---|---|---|---|---|---|
| $f_{SCL}$ | SCL clock frequency | | 0 | | 100 | kHz |
| $t_{LOW}$ | Clock low period | | 4.7 | | | µs |
| $t_{HIGH}$ | Clock high period | | 4.0 | | | µs |
| $t_{BUF}$ | Bus free time (1) | Before new transmission | 4.7 | | | µs |
| $t_{SU:STA}$ | Start condition setup time | | 4.7 | | | µs |
| $t_{HD:STA}$ | Start condition hold time | | 4.0 | | | µs |
| $t_{SU:STO}$ | Stop condition setup time | | 4.7 | | | µs |
| $t_{AA}$ | Clock edge to valid output | SCL low to valid SDA (cycle n) | 0.2 | | 3.5 | µs |
| $t_{DH}$ | Data Out hold time | SCL low (cycle n+1) to SDA change | 0.2 | | | µs |
| $t_R$ | SCL and SDA rise time (1) | | | | 1000 | ns |
| $t_F$ | SCL and SDA fall time (1) | | | | 300 | ns |
| $t_{SU:DAT}$ | Data In setup time | | 250 | | | ns |
| $t_{HD:DAT}$ | Data In hold time | | 0 | | | ns |
| TI | Noise filter SCL and SDA | Noise suppression | | 100 | | ns |
| $t_{WR}$ | Write cycle time | | | | 5 | ms |

Note (1): These values are guaranteed by design.

2047 Table10 4.0

**Table 10. I²C Operating Characteristics**

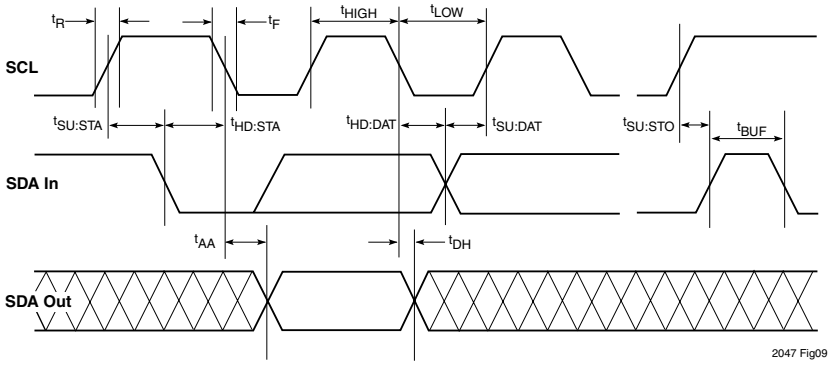



**Figure 9. I²C Operating Characteristics**

## I²C PROGRAMMING INFORMATION (CONTINUED)

### START and STOP Conditions

When both the data and clock lines are high the bus is said to be not busy. A high-to-low transition on the data line, while the clock is high, is defined as the Start condition. A low-to-high transition on the data line, while the clock is high, is defined as the Stop condition. See Figure 10.

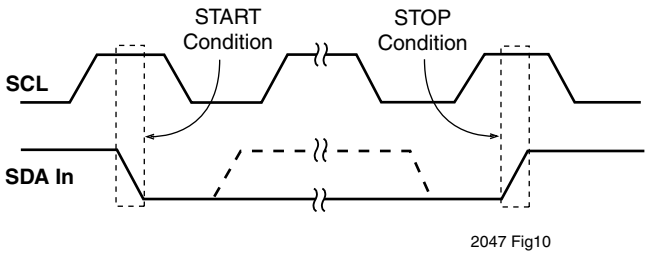



**Figure 10. START and STOP Conditions**

### Acknowledge (ACK)

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either the Master or the Slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line low to Acknowledge that it received the eight bits of data. The Master will leave the SDA line high (NACK) when it terminates a read function.

The SMS45 will respond with an Acknowledge after recognition of a Start condition and its slave address byte. If both the device and a write operation are selected the SMS45 will respond with an Acknowledge after the receipt of each subsequent 8-Bit word. In the READ mode the SMS45 transmits eight bits of data, then releases the SDA line, and monitors the line for an Acknowledge signal. If an Acknowledge is detected and no Stop condition is generated by the Master, the SMS45 will continue to transmit data. If a NACK is detected the SMS45 will terminate further data transmissions and await a Stop condition before returning to the standby power mode.

### Device Addressing

Following a Start condition the Master must output the address of the Slave it is accessing. The most significant four bits of the Slave address are the device type identifier/address. For the SMS45 the default is $1010_{BIN}$. The next two bits are the Bus Address. The next bit (the 7th) is the MSB of the memory address.

| D7 MSB | D6 | D5 | D4 | D3 | D2 | D1 | D0 LSB |
|---|---|---|---|---|---|---|---|
| **Address Bits** | | | | | | | |
| Device Type | | | | Bus | | MSB | R/W |
| SMS45 | | | | x | x | x | x |
| 1 | 0 | 0 | 1 | ⇦ Configuration Register | | | |
| 1 | 0 | 1 | 0 | ⇦ Memory (default) | | | |
| 1 | 0 | 1 | 1 | ⇦ Alternate Memory | | | |

2047 Table11 1.0

**Table 11. Slave Addresses**

### Read/Write Bit

The last bit of the data stream defines the operation to be performed. When set to 1 a Read operation is selected; when set to 0 a Write operation is selected.

## WRITE OPERATIONS

The SMS45 allows two types of Write operations: byte Write and page Write. A byte Write operation writes a single byte during the nonvolatile write period ($t_{WR}$). The page Write operation, limited to the memory array, allows up to 16 bytes in the same page to be written during $t_{WR}$.

### Byte Write

After the Slave address is sent (to identify the Slave device and select either a Read or Write operation), a second byte is transmitted which contains the low order 8 bit address of any one of the 512 words in the array. Upon receipt of the word address the SMS45 responds with an Acknowledge. After receiving the next byte of data it again responds with an Acknowledge. The Master then terminates the transfer by generating a Stop condition, at which time the SMS45 begins the internal Write cycle. While the internal Write cycle is in progress the SMS45 inputs are disabled and the device will not respond to any requests from the Master.

### Page Write (memory only)

The SMS45 is capable of a 16-byte page Write operation. It is initiated in the same manner as the byte Write operation, but instead of terminating the Write cycle after the first data word the Master can transmit up to 15 more bytes of data. After the receipt of each byte the SMS45 will respond with an Acknowledge.

The SMS45 automatically increments the address for subsequent data words. After the receipt of each word the low order address bits are internally incremented by one.

## I²C PROGRAMMING INFORMATION (CONTINUED)

The high order bits of the address byte remain constant. Should the Master transmit more than 16 bytes, prior to generating the Stop condition, the address counter will rollover and the previously written data will be overwritten. As with the byte Write operation, all inputs are disabled during the internal Write cycle. Refer to Figure 11 for the address, Acknowledge, and data transfer sequence.

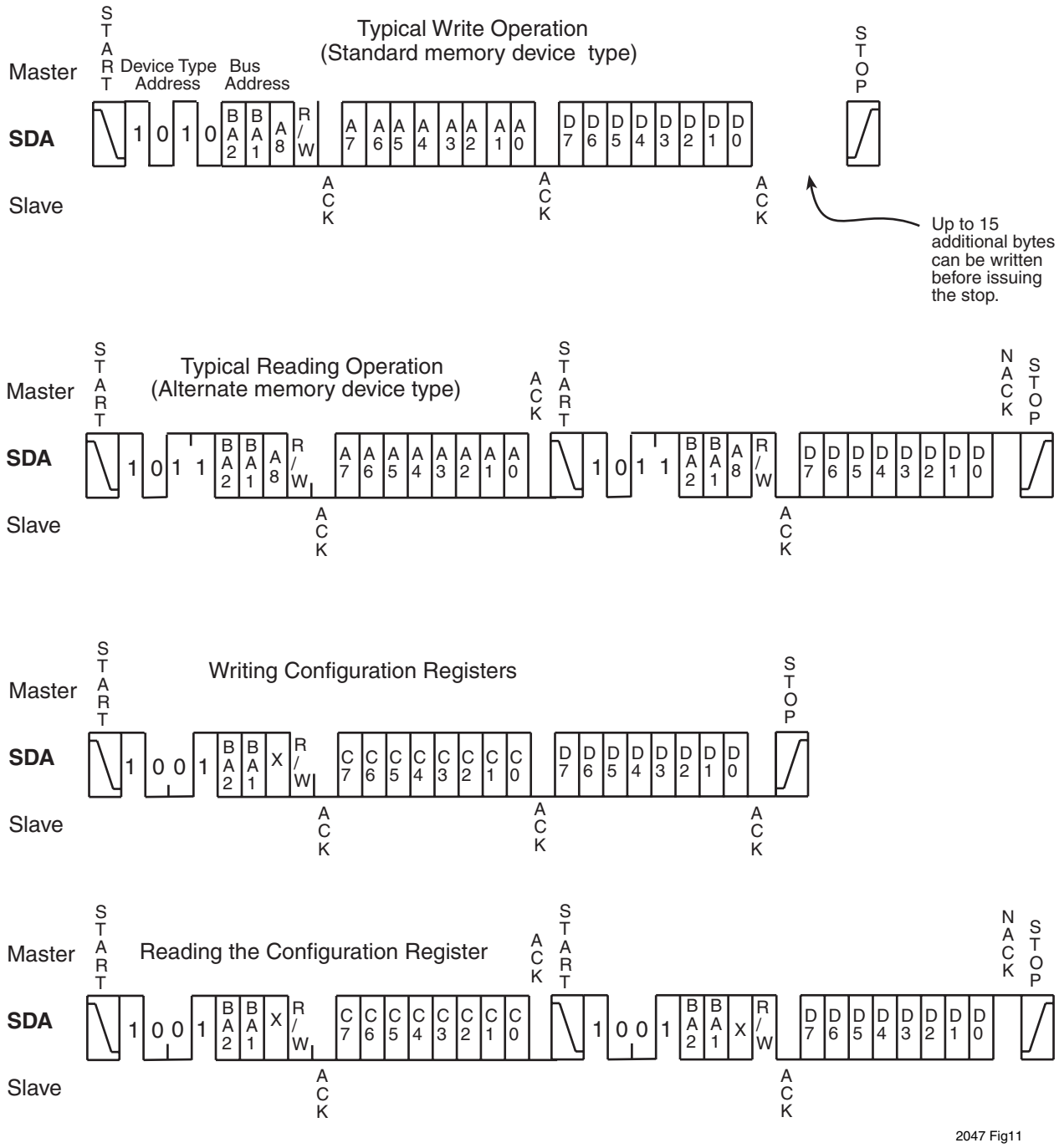



**Figure 11. Read and Write Operations**

## I²C PROGRAMMING INFORMATION (CONTINUED)

### Acknowledge Polling

When the SMS45 is performing an internal Write operation it will ignore any new Start conditions. Since the device will only return an acknowledge after it accepts the Start the part can be continuously queried until an acknowledge is issued, indicating that the internal Write cycle is complete. See the flow chart for the proper sequence of operations for polling.

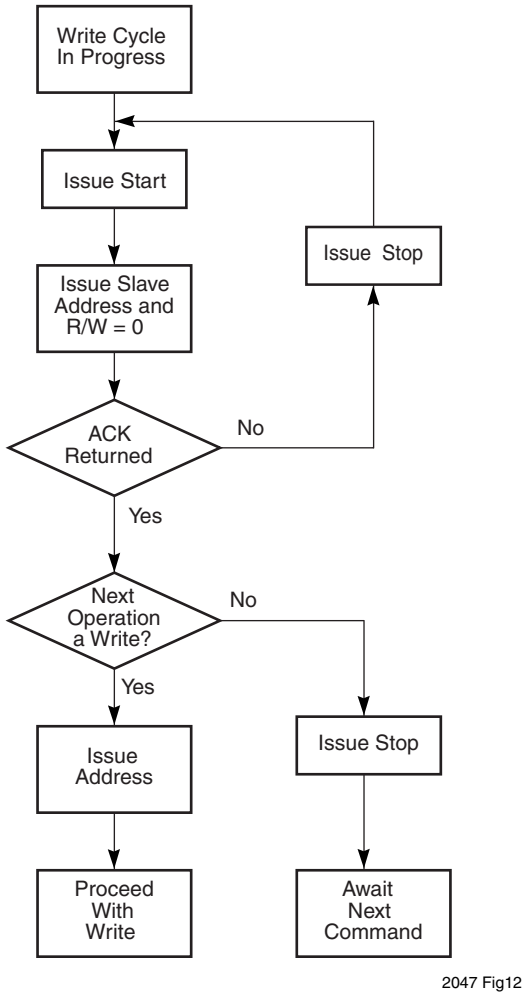



**Figure 12. Write Flow Chart**

## READ OPERATIONS

Read operations are initiated with the R/W bit of the identification field set to 1. There are two different Read options: 1. Current Address Byte Read, and 2. Random Address Byte Read.

### Current Address Read (memory only)

The SMS45 contains an internal address counter which maintains the address of the last word accessed, incremented by one. If the last address accessed (either a Read or Write) was to address location n, the next Read operation would access data from address location n+1 and increment the current address pointer. When the SMS45 receives the Slave address field with the R/W bit set to 1 it issues an acknowledge and transmits the 8-Bit word stored at address location n+1. The current address byte Read operation only accesses a single byte of data. The Master sets the SDA line to NACK and generates a stop condition. At this point the SMS45 discontinues data transmission.

### Random Address Read (Register and Memory)

Random address Read operations allow the Master to access any memory location in a random fashion. This operation involves a two-step process. First, the Master issues a write command which includes the start condition and the Slave address field (with the R/W bit set to Write), followed by the address of the word it is to Read. This procedure sets the internal address counter of the SMS45 to the desired address. After the word address acknowledge is received by the Master it immediately reissues a Start condition, followed by another Slave address field with the R/W bit set to READ. The SMS45 will respond with an Acknowledge and then transmit the 8 data bits stored at the addressed location. At this point the Master sets the SDA line to NACK and generates a Stop condition. The SMS45 discontinues data transmission and reverts to its standby power mode.

### Sequential READ (Memory Only)

Sequential Reads can be initiated as either a current address Read or random access Read. The first word is transmitted as with the other byte Read modes (current address byte Read or random address byte Read); however, the Master now responds with an Acknowledge, indicating that it requires additional data from the SMS45. The SMS45 continues to output data for each Acknowledge received. The Master terminates the sequential Read operation by responding with a NACK, and issues a Stop condition. During a sequential Read operation the internal address counter is automatically incremented with each Acknowledge signal. For Read operations all address bits are incremented, allowing the entire array to be read using a single Read command. After a count of the last memory address the address counter will rollover and the memory will continue to output data.

## APPLICATIONS

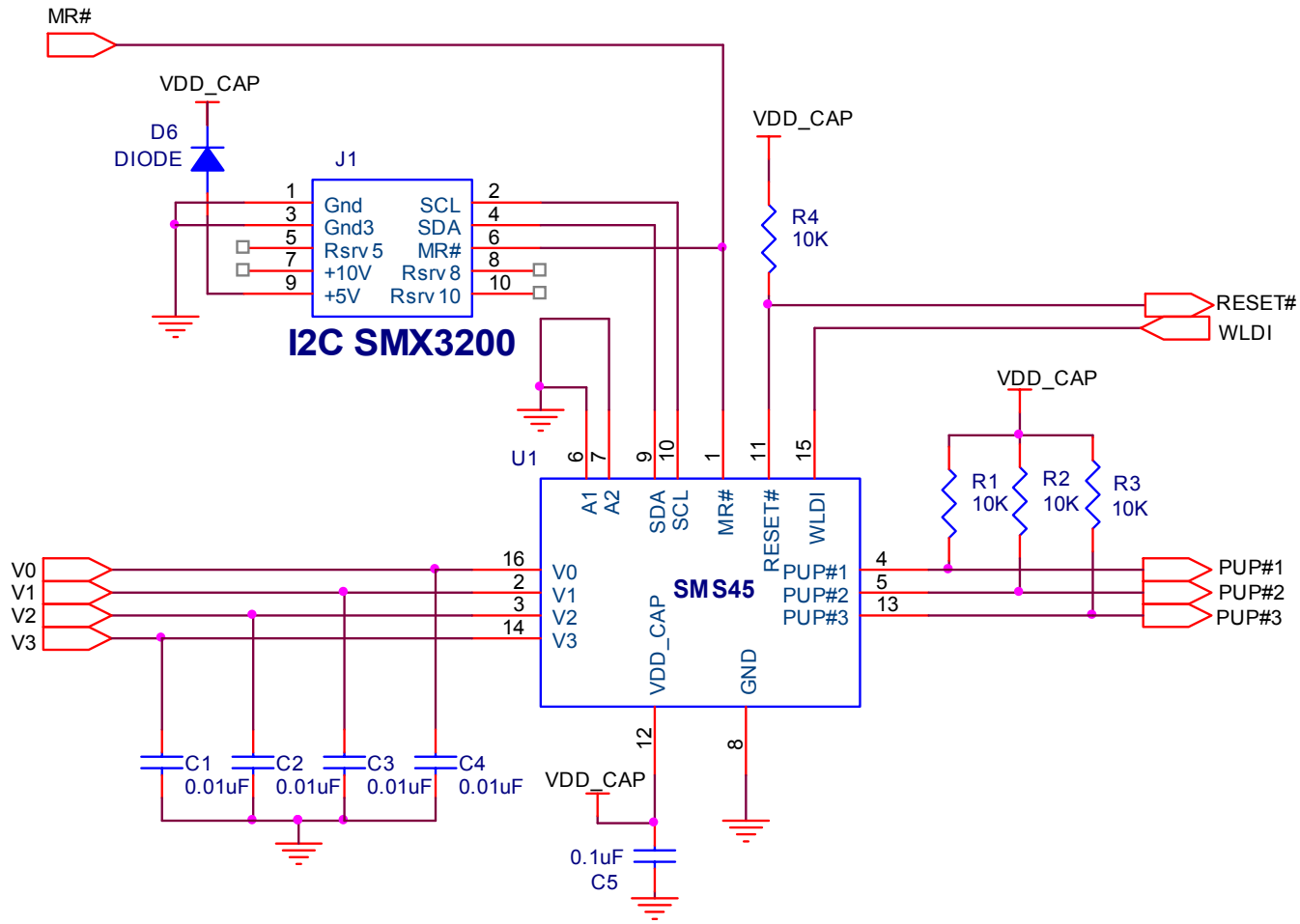



**Figure 13. Typical applications schematic, the SMX3200 programmer has internal SDA and SCL pullup resistors.**

## DEFAULT CONFIGURATION REGISTER SETTINGS - SMS45GC-230

| Register | Contents | Function |
|---|---|---|
| R00 | 56 | V0 threshold set to 3.090V |
| R01 | 28 | V1 threshold set to 2.400V |
| R02 | A0 | V2 threshold set to 1.400V |
| R03 | 14 | V3 threshold set to 0.700V |
| R04 | F3 | Reset Trigger source set for all channels, V0, V1 set to high range and V2, V3 set to low range |
| R05 | X0 | Upper bits are volatile status indication of input supply condition. V0, V1, V2 and V3 set to monitor UV Under Voltage. |
| R06 | 4D | Reset timeout set to 100ms, Watchdog Timer set to 1.6s. Bits D4 and D3 indicate revision control. |
| R07 | 6A | EE memory slave address is 1011, configuration registers are unlocked, cascading delays are all 50ms |

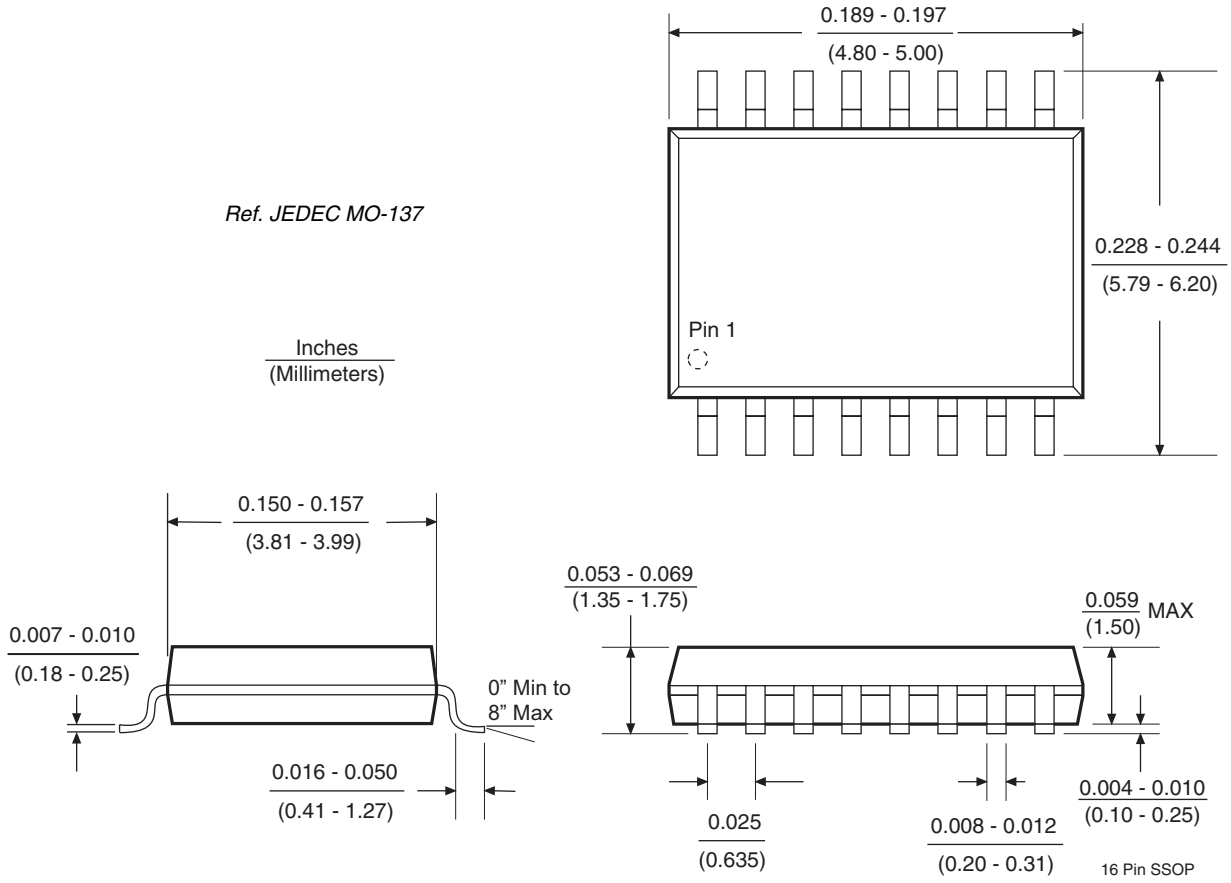
**The default device ordering number is SMS45GC-230, is programmed as described above and tested over the commercial temperature range.**

## PACKAGE

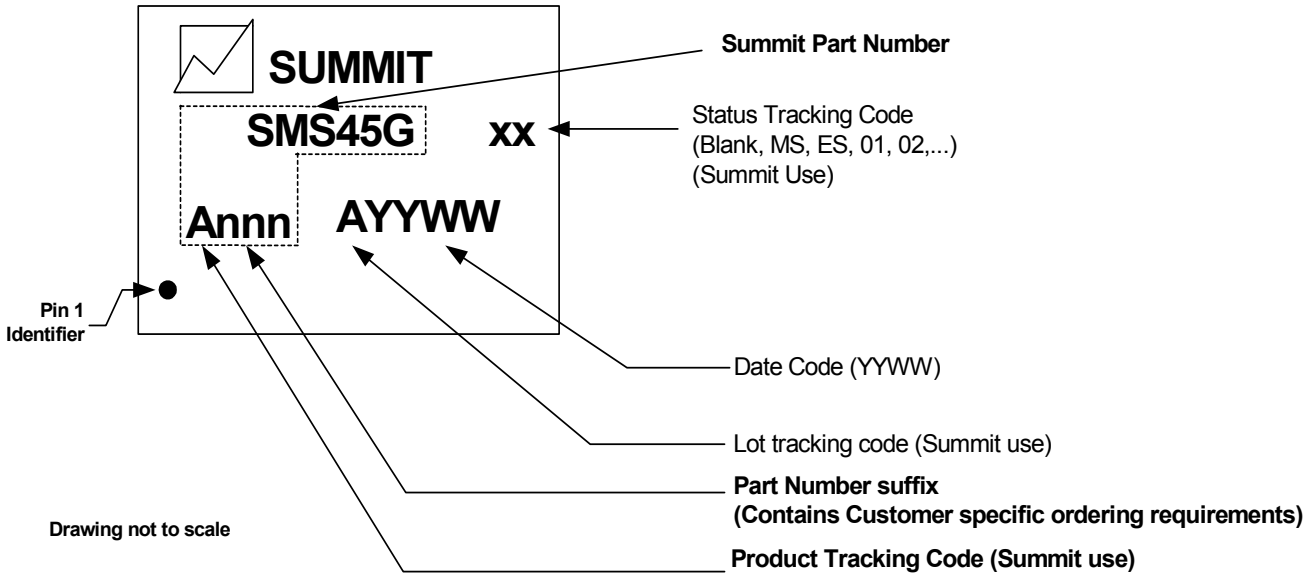
### 16 PIN SSOP PACKAGE

*Ref. JEDEC MO-137*

Inches
(Millimeters)



## PART MARKING




## ORDERING INFORMATION

**SMS45** **G** **C** **nnn**

**Summit Part Number**

**Package**
G=16 Lead SSOP

**Temp Range**
C=Commercial
Blank=Industrial

**Part Number Suffix (see page 18)**
Specific requirements are contained in the suffix such as Hex code, Hex code revision, etc.

NOTICE

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