DATA SHEET

PLUS105-70
Programmable logic sequencer
(16x48x8)

Product specification

IC13

June 15, 1994

hilips Semiconductors

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Programmable logic sequencer (16 × 48 × 8)

PLUS105-70

DESCRIPTION

The PLUS105-70 is a bipolar programmable state machine of the Mealy type. Both the AND and the OR array are user-programmable. All 48 AND gates are connected to the 16 external dedicated inputs (I0 - I15) and to the feedback paths of the 6 buried State Registers (Q_{P0}-Q_{P5}). Because the OR array is programmable, any one or all of the 48 transition terms can be connected to any or all of the State and Output Registers.

All state transition terms can include True, False and Don't Care states of the controlling state variables. A Complement Transition Array supports complex IF-THEN-ELSE state transitions with a single product term.

The PLUS105-70 device features edge-triggered, J-K flip-flops, which provide the added flexibility of the toggle function which is indeterminate on S-R flip-flops. Because the J-K function is a superset of the S-R flip-flop function, the PLUS105-70 is backward compatible with all 105-type devices that have S-R flip-flops. Asynchronous Preset/Output Enable functions are available.

The PLUS105-70 is pin-for-pin and software compatible with Philips Semiconductors PLS105 and PLS105A Logic Sequencers, as well as other commercially available 105-type programmable logic devices.

To facilitate testing of state machine designs, diagnostic mode features for register preset and buried state register observability have been incorporated into the PLUS105-70 device architecture.

Ordering codes are listed in the Ordering Information Table.

FEATURES

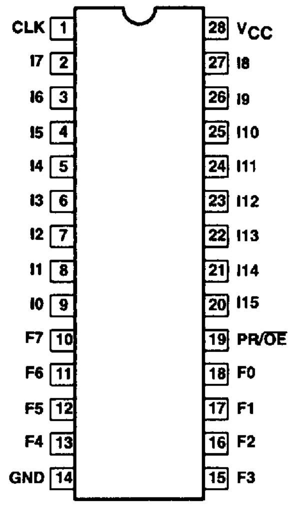
- 70MHz operating frequency
  - 100MHz clock rate
  - No OR term loading restrictions
- Available in 300mil skinny DIP, 600mil-wide DIP, and PLCC packages
- Pin and software compatible with other commercially available 105 sequencers
- 16 input variables
- 8 output functions
- 48 transition terms
- 6-bit State Register
- 8-bit Output Register
- Transition complement array
- Positive edge-triggered clocked J-K (or S-R) flip-flops
- Security fuse
- Programmable Asynchronous Preset or Output Enable
- Power-on preset to (all "1"s) of internal registers
- Power dissipation: 800mW (typ.)
- TTL compatible
- Single +5V supply
- 3-State outputs

APPLICATIONS

- Interface protocols
- Sequence detectors
- Peripheral controllers
- Timing generators
- Sequential circuits
- Elevator controllers
- Security Locking systems
- Counters
- Shift registers

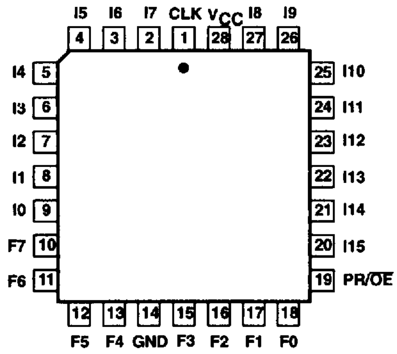
PIN CONFIGURATIONS

N Packages



N = Plastic DIP (600mil-wide)
N3 = Plastic DIP (300mil-wide)

A Package



A = Plastic Leaded Chip Carrier

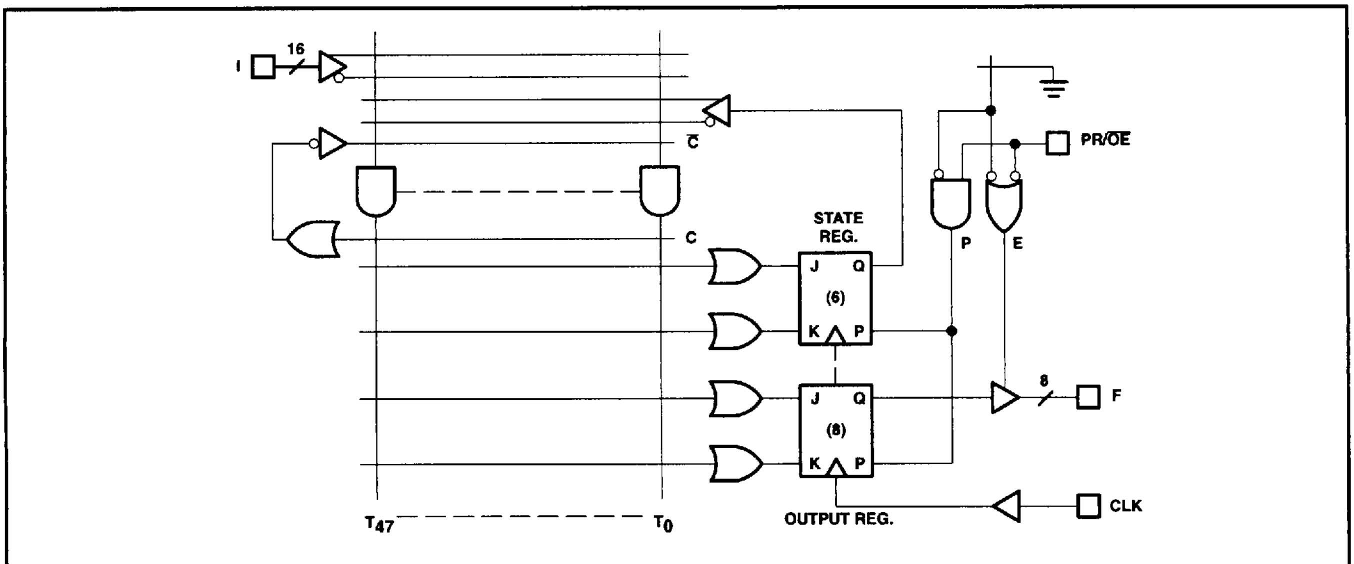
ORDERING INFORMATION

DESCRIPTION	ORDER CODE	DRAWING NUMBER
28-pin Plastic Dual-In-Line, 600mil-wide	PLUS105-70N	0413B
28-pin Plastic Dual-In-Line, 300mil-wide	PLUS105-70N3	0864D
28-pin Plastic Leaded Chip Carrier, 450mil-square	PLUS105-70A	0401F

Programmable logic sequencer (16 × 48 × 8)

PLUS105-70

FUNCTIONAL DIAGRAM



PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION	POLARITY
1	CLK	**Clock:** The Clock input to the State and Output Registers. A Low-to-High transition on this line is necessary to update the contents of both state and output registers.	Active-High (H)
2-9, 26, 27 20-22	I0 - I9, I13 - I15	**Logic Inputs:** The 13 external inputs to the AND array used to program jump conditions between machine states, as determined by a given logic sequence. True and complement signals are generated via use of "H" and "L".	Active-High/ Low (H/L)
23	I12	**Logic/Diagnostic Input:** A 14th external logic input to the AND array, as above, when exercising standard TTL levels. When I12 is held at +10V, device outputs F0 - F5 reflect the contents of State Register bits P0 - P5. The contents of each Output Register remains unaltered.	Active-High/ Low (H/L)
24	I11	**Logic/Diagnostic Input:** A 15th external logic input to the AND array, as above, when exercising standard TTL levels. When I11 is held at +10V, device outputs F0 - F5 become direct inputs for State Register bits P0 - P5; a Low-to-High transition on the clock line loads the values on pins F0 - F5 into the State Register bits P0 - P5. The contents of each Output Register remains unaltered.	Active-High/ Low (H/L)
25	I10	**Logic/Diagnostic Input:** A 16th external logic input to the AND array, as above, when exercising standard TTL levels. When I10 is held at +10V, device outputs F0 - F7 become direct inputs for Output Register bits Q0 - Q7; a Low-to-High transition on the clock line loads the values on pins F0 - F7 into the Output Register bits Q0 - Q7. The contents of each State Register remains unaltered.	Active-High/ Low (H/L)
10-13 15-18	F0 - F7	**Logic Outputs/Diagnostic Outputs/Diagnostic Inputs:** Eight device outputs which normally reflect the contents of Output Register bits Q0 - Q7, when enabled. When I12 is held at +10V, F0 - F5 = (P0 - P5). When I11 is held at +10V, F0 - F5 become inputs to State Register bits P0 - P5. When I10 is held at +10V, F0 - F7 become inputs to Output Register bits Q0 - Q7.	Active-High (H)
19	PR/$\overline{OE}$	**Preset or Output Enable Input: A user programmable function:** • **Preset:** Provides an asynchronous preset to logic "1" of all State and Output Register bits. PR overrides Clock, and when held High, clocking is inhibited and F0 - F7 are High. Normal clocking resumes with the first full clock pulse following a High-to-Low clock transition, after the Preset signal goes Low. See timing definitions. • **Output Enable:** Provides an output enable function to buffers F0 - F7 from the Output Registers.	Active-High (H) Active-Low (L)

TRUTH TABLE[1, 2, 3, 4, 5, 6]

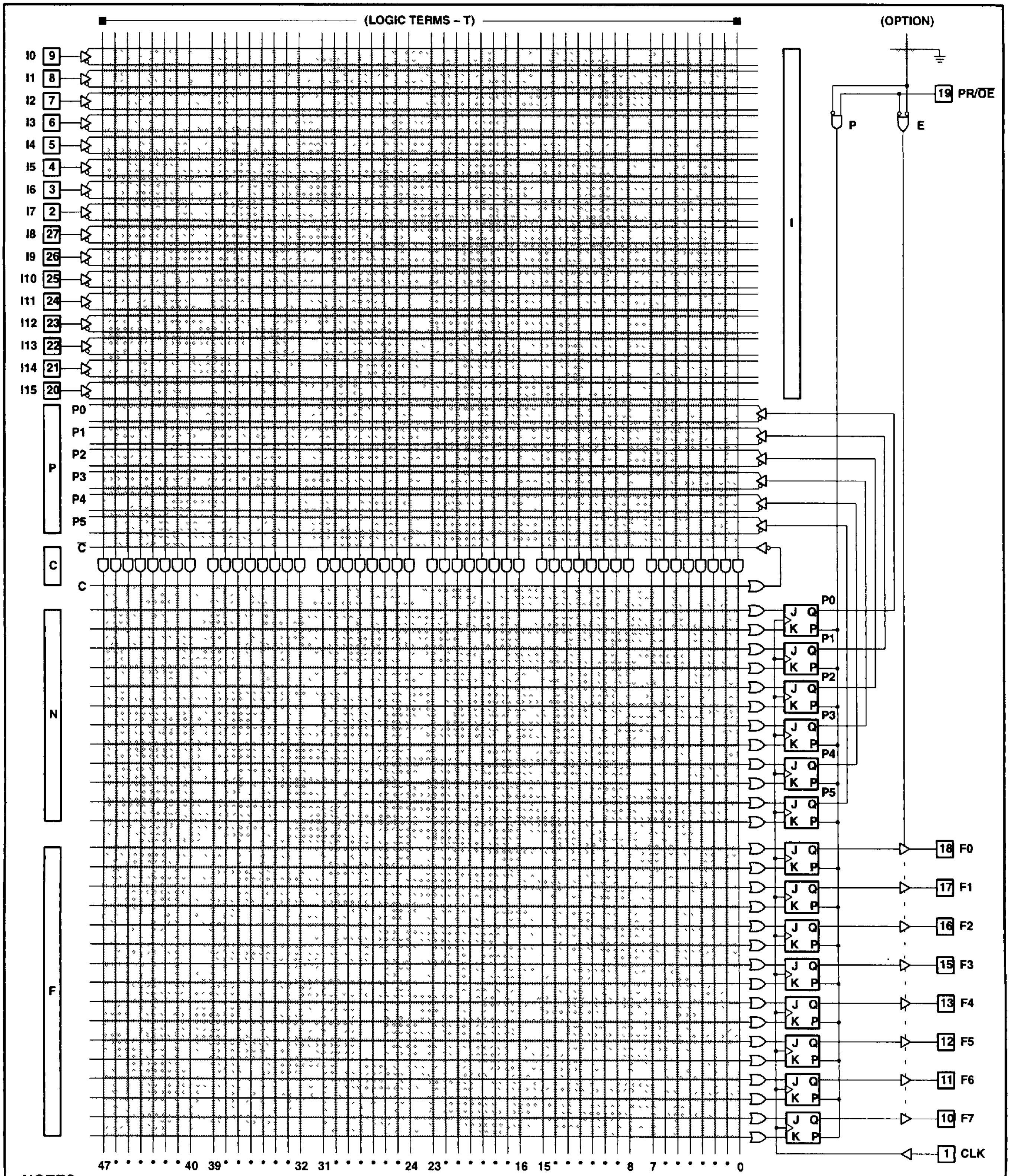
V_{CC}	OPTION PR	OPTION $\overline{OE}$	I10	I11	I12	CK	J	K	Q_P	Q_F	F
	H		*	*	*	X	X	X	H	H	Q_F
	L		+10V	X	X	↑	X	X	Q_P	L	L
	L		+10V	X	X	↑	X	X	Q_P	H	H
	L		X	+10V	X	↑	X	X	L	Q_F	L
	L		X	+10V	X	↑	X	X	H	Q_F	H
	L		X	X	+10V	X	X	X	Q_P	Q_F	Q_P
	L		X	X	X	X	X	X	Q_P	Q_F	Q_F
		H	X	X	*	X	X	X	Q_P	Q_F	Hi-Z
+5V		X	+10V	X	X	↑	X	X	Q_P	L	L
		X	+10V	X	X	↑	X	X	Q_P	H	H
		X	X	+10V	X	↑	X	X	L	Q_F	L
		X	X	+10V	X	↑	X	X	H	Q_F	H
		L	X	X	+10V	X	X	X	Q_P	Q_F	Q_P
		L	X	X	X	X	X	X	Q_P	Q_F	Q_F
		L	X	X	X	↑	L	L	Q_P	Q_F	Q_F
		L	X	X	X	↑	L	H	L	L	L
		L	X	X	X	↑	H	L	H	H	H
		L	X	X	X	↑	H	H	$\overline{Q_P}$	$\overline{Q_F}$	$\overline{Q_F}$
↑	X	X	X	X	X	X	X	X	H	H	

NOTES:
1. Positive Logic:
   J-K (or S/R) = $T_0 + T_1 + T_2 + \ldots T_{48}$
   $T_n = (C_0)\ (I0, I1, I2, \ldots)\ (P_0, P_1, \ldots P_5)$
2. Either Preset (Active-High) or Output Enable (Active-Low) are available, but not both. The desired function is a user-programmable option.
3. ↑ denotes transition from Low-to-High level.
4. * = H or L or +10V
5. X = Don't Care (≤ 5.5V)
6. When using the F_n pins as inputs to the State and Output Registers in diagnostic mode, the F buffers are 3-Stated and the indicated levels on the output pins are forced by the user.

VIRGIN STATE

A factory-shipped virgin device contains all fusible links intact, such that:
1. PR/$\overline{OE}$ option is set to PR. Note that even if the PR function is not used, all registers are preset to "1" by the power-up procedure.
2. All transition terms are disabled (0).
3. All J-K flip-flop inputs are disabled (0).

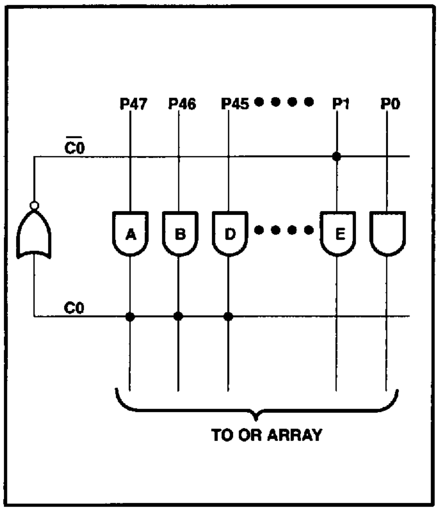
LOGIC DIAGRAM



NOTES:

1. All AND gate inputs with a blown link float to a logic "1".
2. All OR gate inputs with a blown fuse float to logic "0".
3. Programmable connection.

COMPLEMENT ARRAY DETAIL



The complement array is a special sequencer feature that is often used for detecting illegal states. It is also ideal for generating IF-THEN-ELSE logic statements with a minimum number of product terms.

The concept is deceptively simple. If you subscribe to the theory that the expressions (/A * /B * /C) and $(\overline{A + B + C})$ are equivalent, you will begin to see the value of this single term NOR array.

The complement array is a single OR gate with inputs from the AND array. The output of the complement array is inverted and feedback to the AND array (NOR function). The output of the array will be LOW if any one or more of the AND terms connected to it are active (HIGH). If, however, all the connected terms are inactive (LOW), which is a classic unknown state, the output of the complement array will be HIGH.

Consider the product terms A, B and D that represent defined states. They are also connected to the input of the complement array. When the condition (not A and not B and not D) exists, the Complement Array will detect this and propagate an Active-High signal to the AND array. This signal can be connected to product term E, which could be used in turn to preset the state machine to a known state. Without the complement array, one would have to generate product terms for all unknown or illegal states. With very complex state machines, this approach can be prohibitive, both in terms of time and wasted resources.

Note that use of the Complement Array adds an additional delay path through the device. Refer to the AC Electrical Characteristics for details.

THERMAL RATINGS

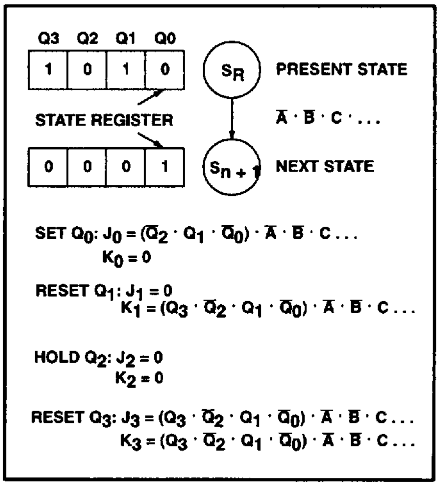
TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS		UNIT
		MIN	MAX	
V_{CC}	Supply voltage		+7.0	V_{DC}
V_{IN}	Input voltage		+5.5	V_{DC}
V_{OUT}	Output voltage		+5.5	V_{DC}
I_{IN}	Input currents	-30	+30	mA
I_{OUT}	Output currents		+100	mA
T_{amb}	Operating temperature range	0	+75	°C
T_{stg}	Storage temperature range	-65	+150	°C

NOTE:
1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

LOGIC FUNCTION



DC ELECTRICAL CHARACTERISTICS

$0°C \leq T_{amb} \leq 75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP[1]	MAX	
Input voltage[2]						
V_{IH}	High	V_{CC} = MAX	2.0			V
V_{IL}	Low	V_{CC} = MIN			0.8	V
V_{IC}	Clamp[3]	V_{CC} = MIN, I_{IN} = –12mA		–0.8	–1.2	V
Output voltage[2]						
		V_{CC} = MIN				
V_{OH}	High	I_{OH} = –2mA	2.4			V
V_{OL}	Low	I_{OL} = 9.6mA		0.35	0.45	V
Input current						
		V_{CC} = MAX				
I_{IH}	High	V_{IN} = V_{CC}		<1	30	µA
I_{IL}	Low	V_{IN} = 0.45V		–20	–250	µA
Output current						
		V_{CC} = MAX				
$I_{O(OFF)}$	Hi-Z state	V_{OUT} = 2.7V		1	40	µA
		V_{OUT} = 0.45V		–1	–40	µA
I_{OS}	Short circuit[3, 4]	V_{OUT} = 0V	–15		–70	mA
I_{CC}	V_{CC} supply current[5]	V_{CC} = MAX		170	190	mA
Capacitance						
		V_{CC} = 5.0V				
C_{IN}	Input	V_{IN} = 2.0V		8		pF
C_{OUT}	Output	V_{OUT} = 2.0V		10		pF

NOTES:
1. All typical values are at V_{CC} = 5V, T_{amb} = +25°C.
2. All voltage values are with respect to network ground terminal.
3. Test one at a time.
4. Duration of short circuit should not exceed 1 second.
5. I_{CC} is measured with the PR/$\overline{OE}$ input grounded, all other inputs at 4.5V and the outputs open.

AC ELECTRICAL CHARACTERISTICS

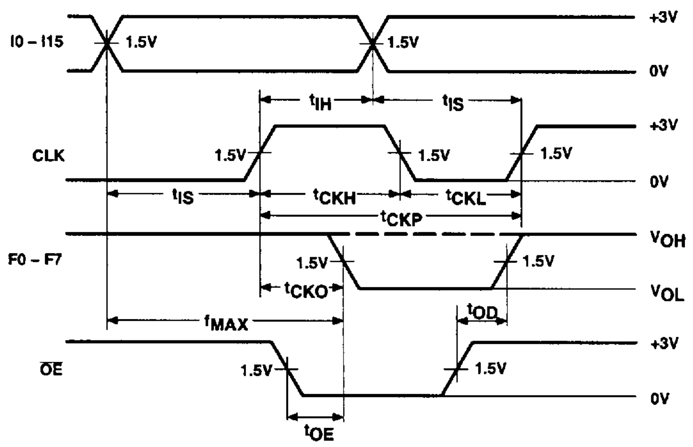
$R_1 = 470\Omega$, $R_2 = 1K\Omega$, $C_L = 30pF$, $0°C \le T_{amb} \le +75°C$, $4.75V \le V_{CC} \le 5.25V$

SYMBOL	PARAMETER	FROM	TO	LIMITS MIN	TYP[1]	MAX	UNIT
Pulse Width							
t_{CKH}	Clock High	CK +	CK –	5	4.0		ns
t_{CKL}	Clock Low	CK –	CK +	5	4.5		ns
t_{CKP}	Clock Period	CK +	CK +	10	8.5		ns
t_{PRH}	Preset pulse	PR +	PR –	10	5.0		ns
Setup Time							
t_{IS1}	Input	Input ±	CK +	8	7		ns
t_{IS2}	Input (through Complement Array)	Input ±	CK +	15	11		ns
t_{VS}	Power-on preset	V_{CC} +	CK –	0	—		ns
t_{PRS}	Clock resume (after preset)	PR –	CK –	0	–6		ns
t_{NVCK}	Clock lockout (before preset)	CK –	PR –	10	6.5		ns
Hold Time							
t_{IH}	Input	CK +	Input ±	0	–5		ns
Diagnostic Mode							
t_{RJS}	Initialization of diagnostic mode	I10, I11 or I12 + (to 10V)	F_n as inputs	50	25		ns
t_{RJH}	Clock for diagnostic mode	CK +	Register input jam	50	25		ns
Propagation Delay[2]							
t_{CKO}	Clock	CK +	Output ±	3.5	5.5	6	ns
t_{OE}	Output enable[3]	OE –	Output –		6.0	6.5	ns
t_{OD}	Output disable[3]	OE +	Output +		6.0	6.5	ns
t_{PR}	Preset	PR +	Output +		7.0	12	ns
t_{PPR}	Power-on preset	V_{CC} +	Output +		5.0	10	ns
Frequency of Operation							
f_{MAX1}	Without Complement Array $\left(\frac{1}{t_{IS1} + t_{CKO}}\right)$	Input ±	Output ±	71.4	80.0		MHz
f_{MAX2}	With Complement Array $\left(\frac{1}{t_{IS2} + t_{CKO}}\right)$	Input thru Complement Array ±	Output ±	47.6	60.6		MHz
f_{MAX3}	Internal feedback without Complement Array $\left(\frac{1}{t_{CKL} + t_{CKH}}\right)$	Register Output ±	Register Input ±	100.0	111.1		MHz
f_{MAX4}	Internal feedback with Complement Array $\left(\frac{1}{t_{IS2}}\right)$	Register Output thru Complement Array ±	Register Input ±	66.7	90.9		MHz
f_{CLK}	Clock period	CK +	CK +	100.0	117.7		MHz

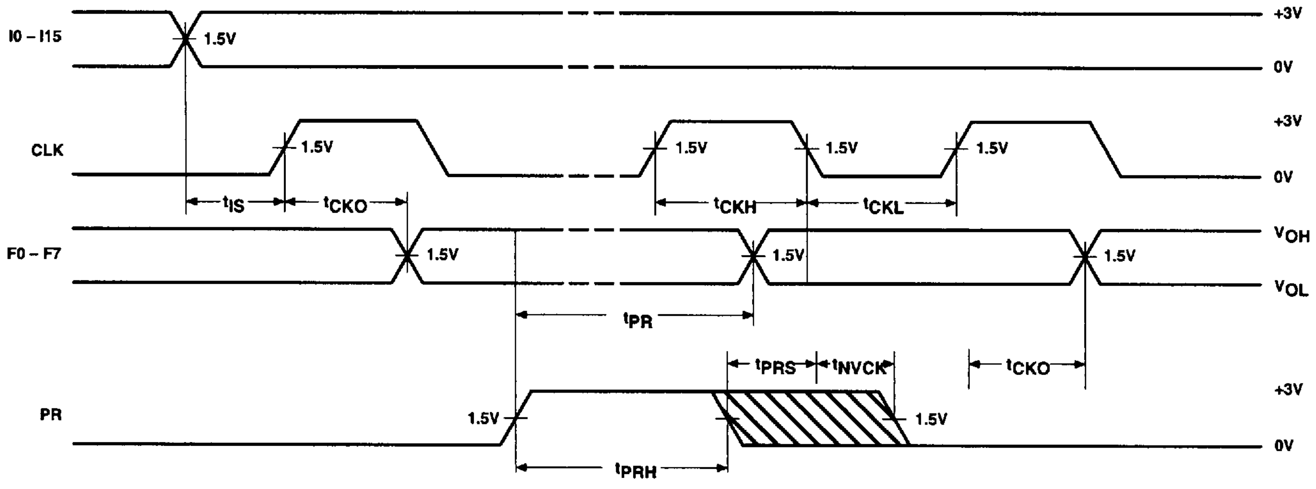
NOTES:

1. All typical values are at $V_{CC} = 5V$, $T_{amb} = +25°C$.
2. All propagation delays and setup times are measured and specified under worst case conditions.
3. For 3-State output; output enable times are tested with $C_L = 30pF$ to the 1.5V level, and S_1 is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with $C_L = 5pF$. High-to-High impedance tests are made to an output voltage of $V_T = (V_{OH} - 0.5V)$ with S_1 open, and Low-to-High impedance tests are made to the $V_T = (V_{OL} + 0.5V)$ level with S_1 closed.

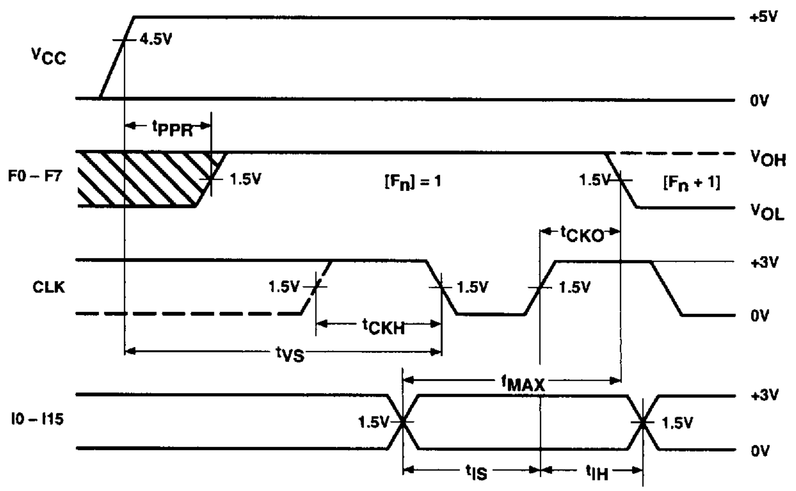
TIMING DIAGRAMS



Sequential Mode

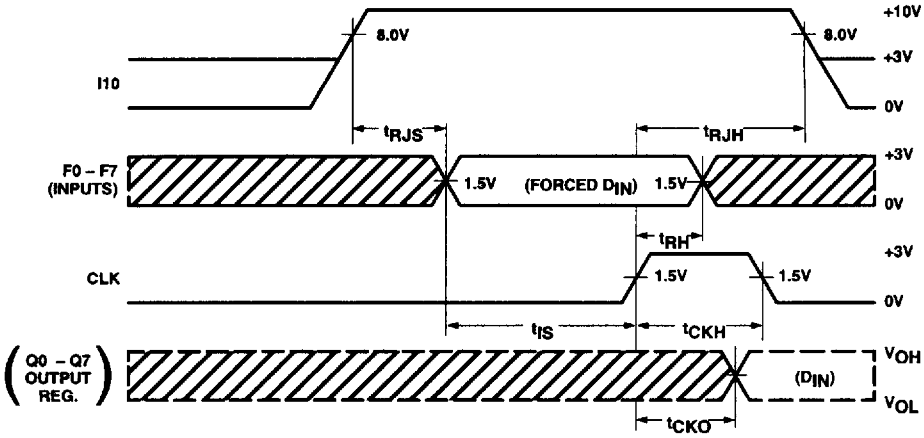


Asynchronous Preset

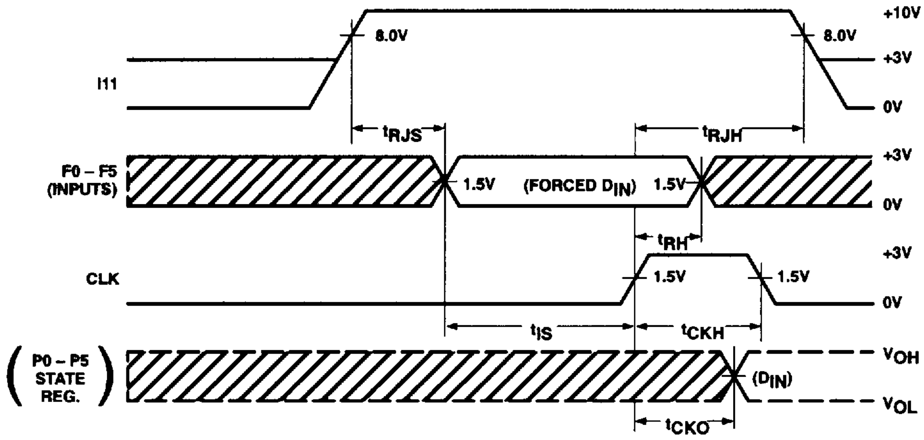


Power-On Preset

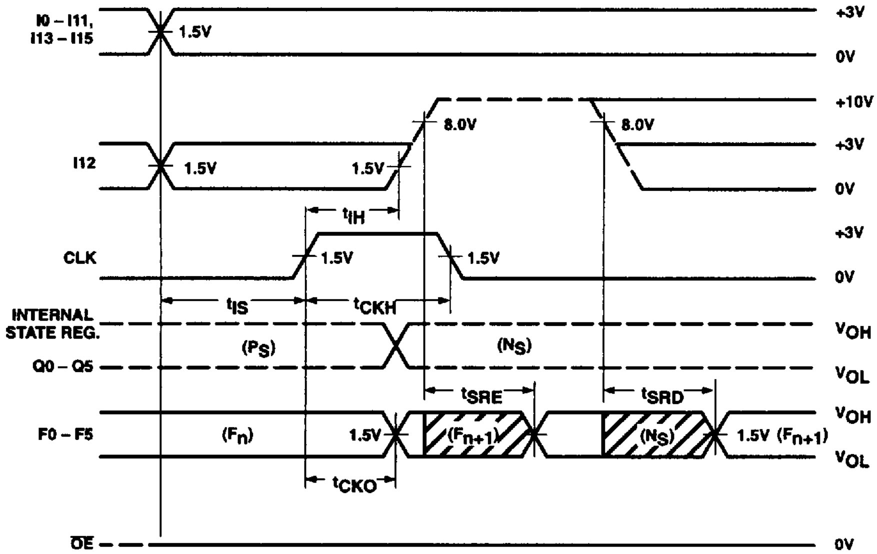
TIMING DIAGRAMS (Continued)



Diagnostic Mode—Output Register Input Jam



Diagnostic Mode—State Register Input Jam



Diagnostic Mode—State Register Outputs

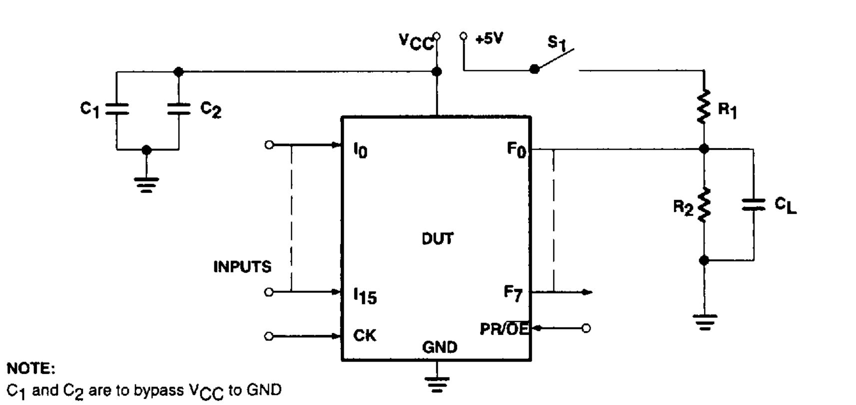
TIMING DEFINITIONS

SYMBOL	PARAMETER
t_{IH}	Required delay between positive transition of Clock and end of valid Input data.
t_{IS1}	Required delay between beginning of valid input and positive transition of Clock.
t_{IS2}	Required delay between beginning of valid Input and positive transition of Clock, when using optional Complement Array (two passes necessary through the AND Array).
t_{CKH}	Width of input clock pulse
t_{CKL}	Interval between clock pulses.
t_{CKO}	Delay between positive transition of Clock and when Outputs become valid (with $PR/\overline{OE}$ Low).
t_{CKP}	Minimum guaranteed clock period.
t_{NVCK}	Required delay between the negative transition of the clock and the negative transition of the Asynchronous PRESET to guarantee that the clock edge is not detected as a valid negative transition.

SYMBOL	PARAMETER
t_{OD}	Delay between beginning of Output Enable High and when Outputs are in the OFF-state.
t_{OE}	Delay between beginning of Output Enable Low and when Outputs become valid.
t_{PPR}	Delay between V_{CC} (after power-on) and when Outputs become preset at "1".
t_{PR}	Delay between positive transition of Preset and when Outputs become valid at "1".
t_{PRH}	Width of preset input pulse.
t_{PRS}	Required delay between negative transition of Asynchronous Preset and the first positive transition of Clock.
t_{RH}	Required delay between positive transition of clock and the end of valid input data (F0 – F7 as inputs), when jamming data into the State or Output registers in the Diagnostic Mode.

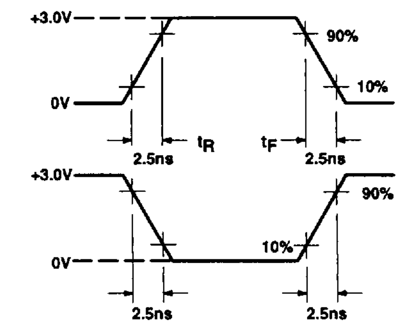
SYMBOL	PARAMETER
t_{RJH}	Required delay between positive transition of clock and return of input I10, I11 or I12 from Diagnostic Mode (10V).
t_{RJS}	Required delay between inputs I10, I11 or I12 transition to Diagnostic Mode (10V), and when the output pins become available as inputs.
t_{SRD}	Delay between input (I12) transition to Logic mode and when the Outputs reflect the contents of the Output Register.
t_{SRE}	Delay between input I12 transition to Diagnostic Mode and when the Outputs reflect the contents of the State Register.
t_{VS}	Required delay between V_{CC} (after power-on) and negative transition of Clock preceding first reliable clock pulse.
f_{CLK}	Minimum guaranteed clock frequency (register toggle frequency)
f_{MAX}	Minimum guaranteed operating frequency.

TEST LOAD CIRCUITS



NOTE:
C_1 and C_2 are to bypass V_{CC} to GND

VOLTAGE WAVEFORMS



MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified

Input Pulses

LOGIC PROGRAMMING

PLUS105-70 is fully supported by industry standard (JEDEC compatible) PLD CAD tools, including Philips Semiconductors' SNAP design software package. ABEL™, CUPL™ and PALASM® 90 design software packages also support the PLUS105-70 architecture.

All packages allow Boolean and state equation entry formats. SNAP, ABEL and CUPL also accept, as input, schematic capture format.

PLUS105-70 logic designs can also be generated using the program table entry format, which is detailed on the following pages. This program table entry format is supported by SNAP.

To implement the desired logic functions, the state of each logic variable from logic equations (I, B, O, P, etc.) is assigned a symbol. The symbols for TRUE, COMPLEMENT, INACTIVE, PRESET, etc., are defined below.

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CUPL is a trademark of Logical Devices, Inc.
PALASM is a registered trademark of AMD Corp.