FAIRCHILD SEMICONDUCTOR®

May 2001

QFET™

# FQB50N06L / FQI50N06L

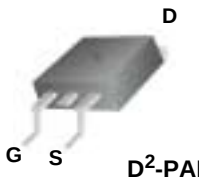
## 60V LOGIC N-Channel MOSFET

### General Description

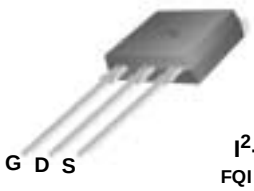
These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.
This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for low voltage applications such as automotive, DC/DC converters, and high efficiency switching for power management in portable and battery operated products.

### Features

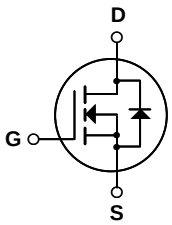
- 52.4A, 60V, $R_{DS(on)}$ = 0.021Ω @$V_{GS}$ = 10 V
- Low gate charge ( typical 24.5 nC)
- Low Crss ( typical 90 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability
- 175°C maximum junction temperature rating




$D^2$-PAK
FQB Series




$I^2$-PAK
FQI Series




## Absolute Maximum Ratings

$T_C$ = 25°C unless otherwise noted

| Symbol | Parameter | | FQB50N06L / FQI50N06L | Units |
|---|---|---|---|---|
| $V_{DSS}$ | Drain-Source Voltage | | 60 | V |
| $I_D$ | Drain Current - Continuous ($T_C$ = 25°C) | | 52.4 | A |
| | - Continuous ($T_C$ = 100°C) | | 37.1 | A |
| $I_{DM}$ | Drain Current - Pulsed | (Note 1) | 210 | A |
| $V_{GSS}$ | Gate-Source Voltage | | ± 20 | V |
| $E_{AS}$ | Single Pulsed Avalanche Energy | (Note 2) | 990 | mJ |
| $I_{AR}$ | Avalanche Current | (Note 1) | 52.4 | A |
| $E_{AR}$ | Repetitive Avalanche Energy | (Note 1) | 12.1 | mJ |
| dv/dt | Peak Diode Recovery dv/dt | (Note 3) | 7.0 | V/ns |
| $P_D$ | Power Dissipation ($T_A$ = 25°C) * | | 3.75 | W |
| | Power Dissipation ($T_C$ = 25°C) | | 121 | W |
| | - Derate above 25°C | | 0.81 | W/°C |
| $T_J$, $T_{STG}$ | Operating and Storage Temperature Range | | -55 to +175 | °C |
| $T_L$ | Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds | | 300 | °C |

## Thermal Characteristics

| Symbol | Parameter | Typ | Max | Units |
|---|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case | -- | 1.24 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient * | -- | 40 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient | -- | 62.5 | °C/W |

* When mounted on the minimum pad size recommended (PCB Mount)

## Electrical Characteristics

$T_C$ = 25°C unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_D$ = 250 µA | 60 | -- | -- | V |
| $\Delta BV_{DSS}$ / $\Delta T_J$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 250 µA, Referenced to 25°C | -- | 0.06 | -- | V/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 60 V, $V_{GS}$ = 0 V | -- | -- | 1 | µA |
| | | $V_{DS}$ = 48 V, $T_C$ = 150°C | -- | -- | 10 | µA |
| $I_{GSSF}$ | Gate-Body Leakage Current, Forward | $V_{GS}$ = 20 V, $V_{DS}$ = 0 V | -- | -- | 100 | nA |
| $I_{GSSR}$ | Gate-Body Leakage Current, Reverse | $V_{GS}$ = -20 V, $V_{DS}$ = 0 V | -- | -- | -100 | nA |
| **On Characteristics** | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | 1.0 | -- | 2.5 | V |
| $R_{DS(on)}$ | Static Drain-Source On-Resistance | $V_{GS}$ = 10 V, $I_D$ = 26.2 A | -- | 0.017 | 0.021 | Ω |
| | | $V_{GS}$ = 5 V, $I_D$ = 26.2 A | -- | 0.020 | 0.025 | |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 25 V, $I_D$ = 26.2 A (Note 4) | -- | 40 | -- | S |
| **Dynamic Characteristics** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 25 V, $V_{GS}$ = 0 V, f = 1.0 MHz | -- | 1250 | 1630 | pF |
| $C_{oss}$ | Output Capacitance | | -- | 445 | 580 | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | -- | 90 | 120 | pF |
| **Switching Characteristics** | | | | | | |
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD}$ = 30 V, $I_D$ = 26.2 A, $R_G$ = 25 Ω (Note 4, 5) | -- | 20 | 50 | ns |
| $t_r$ | Turn-On Rise Time | | -- | 380 | 770 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | -- | 80 | 170 | ns |
| $t_f$ | Turn-Off Fall Time | | -- | 145 | 300 | ns |
| $Q_g$ | Total Gate Charge | $V_{DS}$ = 48 V, $I_D$ = 52.4 A, $V_{GS}$ = 5 V (Note 4, 5) | -- | 24.5 | 32 | nC |
| $Q_{gs}$ | Gate-Source Charge | | -- | 6 | -- | nC |
| $Q_{gd}$ | Gate-Drain Charge | | -- | 14.5 | -- | nC |
| **Drain-Source Diode Characteristics and Maximum Ratings** | | | | | | |
| $I_S$ | Maximum Continuous Drain-Source Diode Forward Current | | -- | -- | 52.4 | A |
| $I_{SM}$ | Maximum Pulsed Drain-Source Diode Forward Current | | -- | -- | 210 | A |
| $V_{SD}$ | Drain-Source Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 52.4 A | -- | -- | 1.5 | V |
| $t_{rr}$ | Reverse Recovery Time | $V_{GS}$ = 0 V, $I_S$ = 52.4 A, $dI_F$ / dt = 100 A/µs (Note 4) | -- | 65 | -- | ns |
| $Q_{rr}$ | Reverse Recovery Charge | | -- | 125 | -- | nC |

**Notes:**
1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 300µH, $I_{AS}$ = 52.4A, $V_{DD}$ = 25V, $R_G$ = 25 Ω, Starting $T_J$ = 25°C
3. $I_{SD} \leq$ 52.4A, di/dt $\leq$ 300A/µs, $V_{DD} \leq BV_{DSS}$, Starting $T_J$ = 25°C
4. Pulse Test : Pulse width $\leq$ 300µs, Duty cycle $\leq$ 2%
5. Essentially independent of operating temperature

## Typical Characteristics

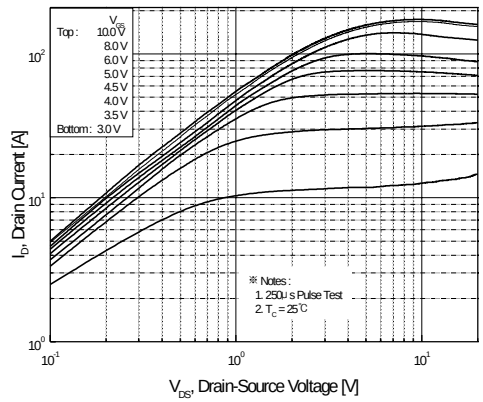



**Figure 1. On-Region Characteristics**

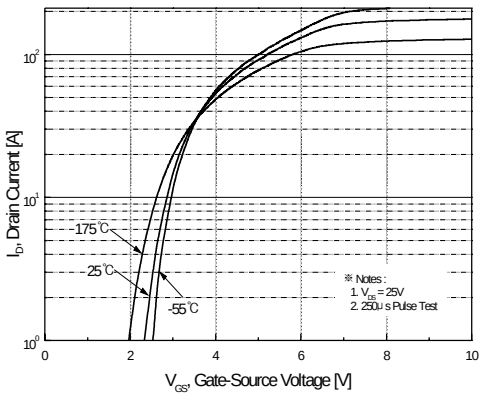



**Figure 2. Transfer Characteristics**

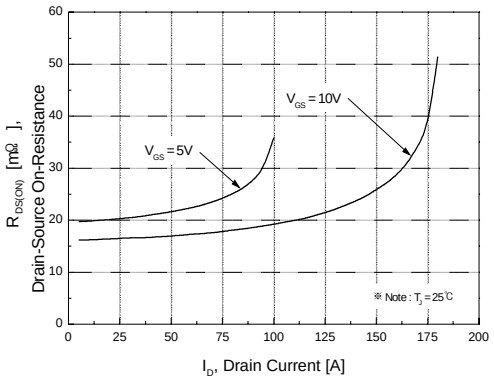



**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**

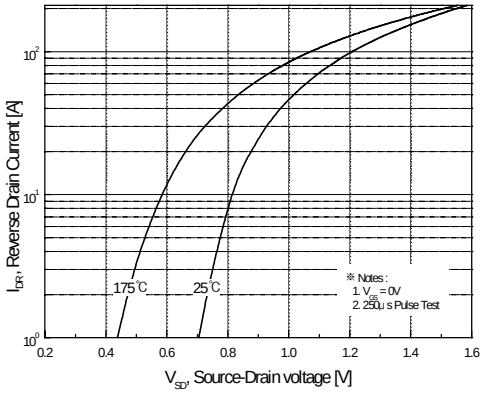



**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**

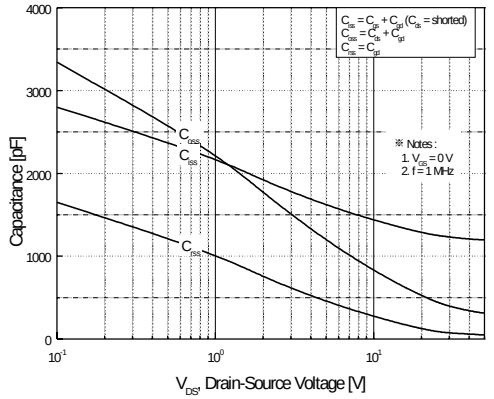



**Figure 5. Capacitance Characteristics**

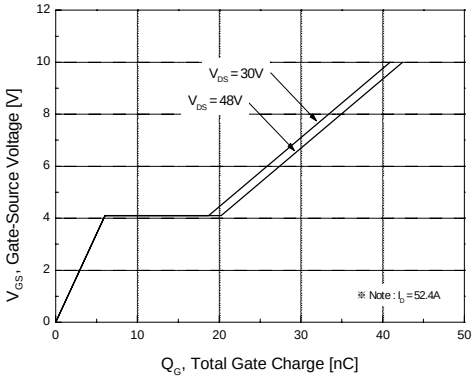



**Figure 6. Gate Charge Characteristics**

## Typical Characteristics (Continued)

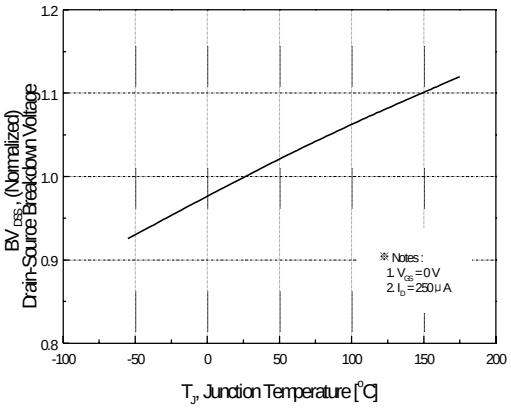



**Figure 7. Breakdown Voltage Variation vs. Temperature**

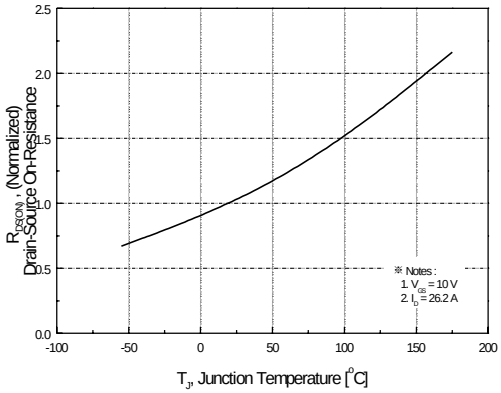



**Figure 8. On-Resistance Variation vs. Temperature**

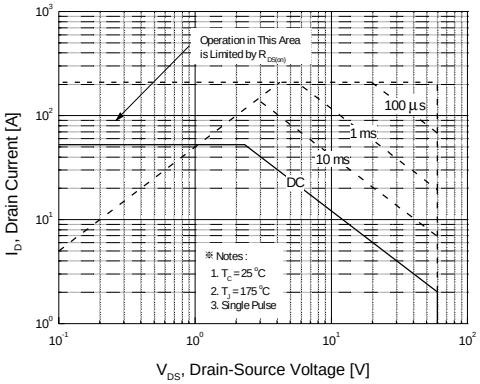



**Figure 9. Maximum Safe Operating Area**

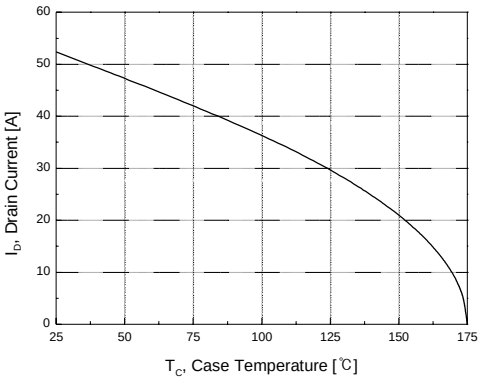



**Figure 10. Maximum Drain Current vs. Case Temperature**

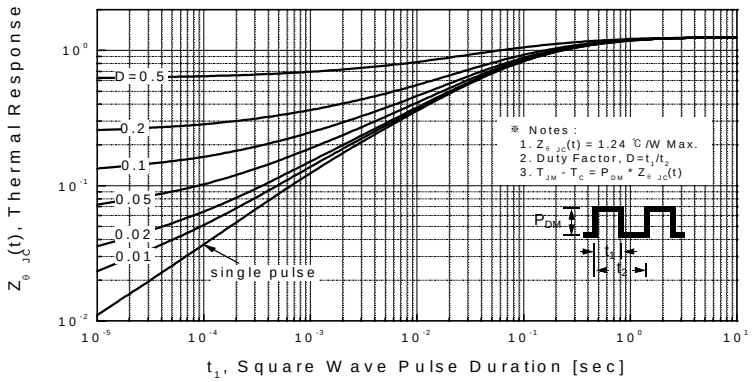
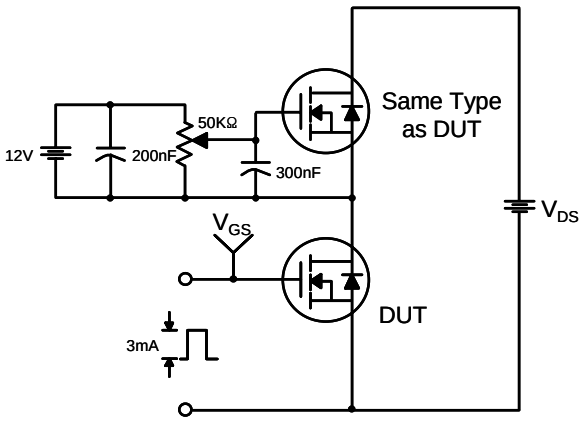
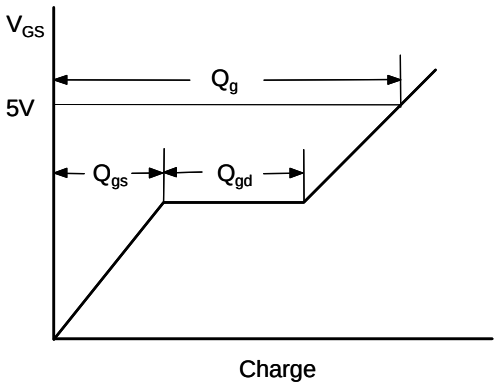


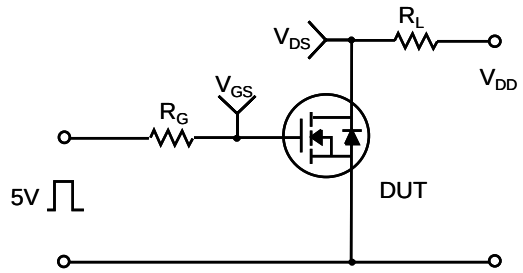

**Figure 11. Transient Thermal Response Curve**

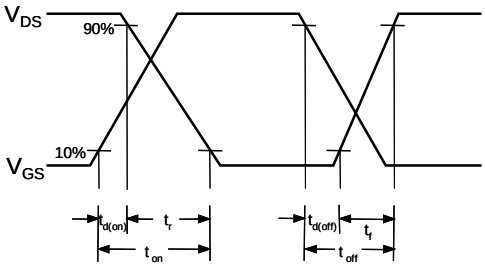
## Gate Charge Test Circuit & Waveform



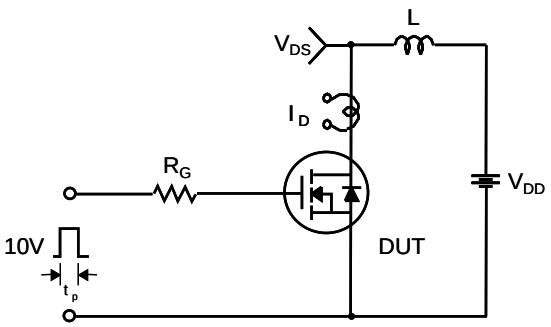




## Resistive Switching Test Circuit & Waveforms

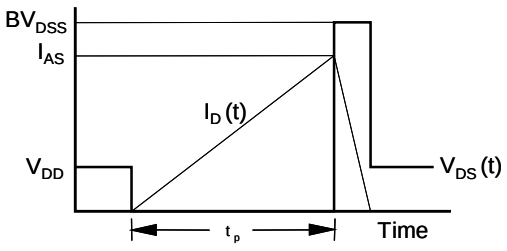


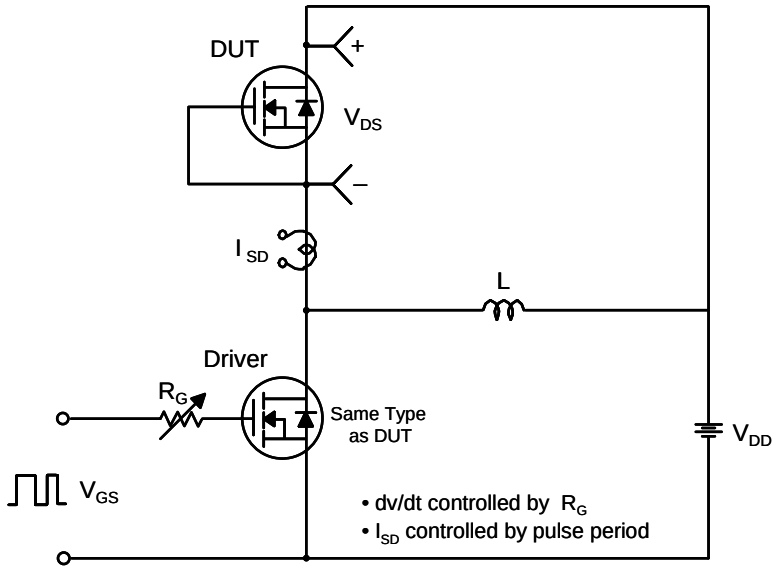

## Unclamped Inductive Switching Test Circuit & Waveforms

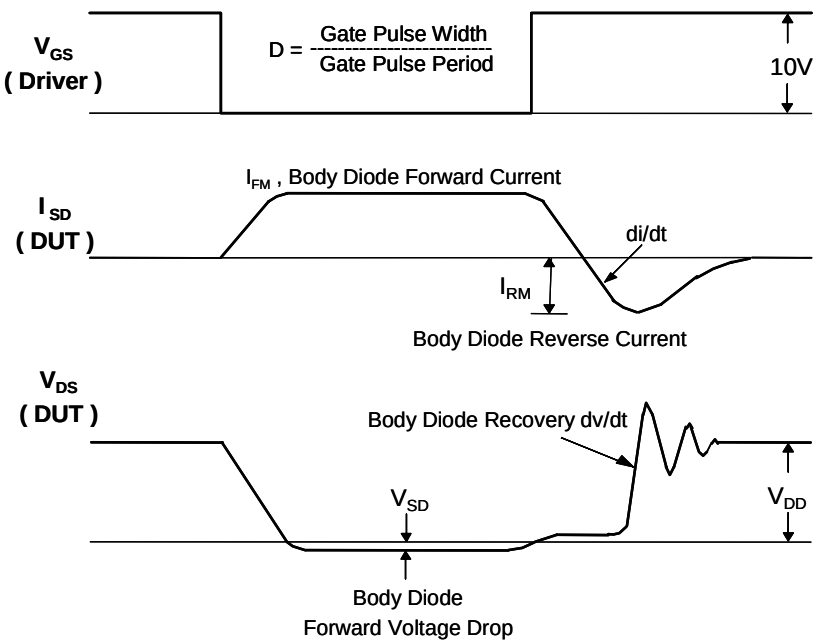



$$E_{AS} = \frac{1}{2} L I_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$



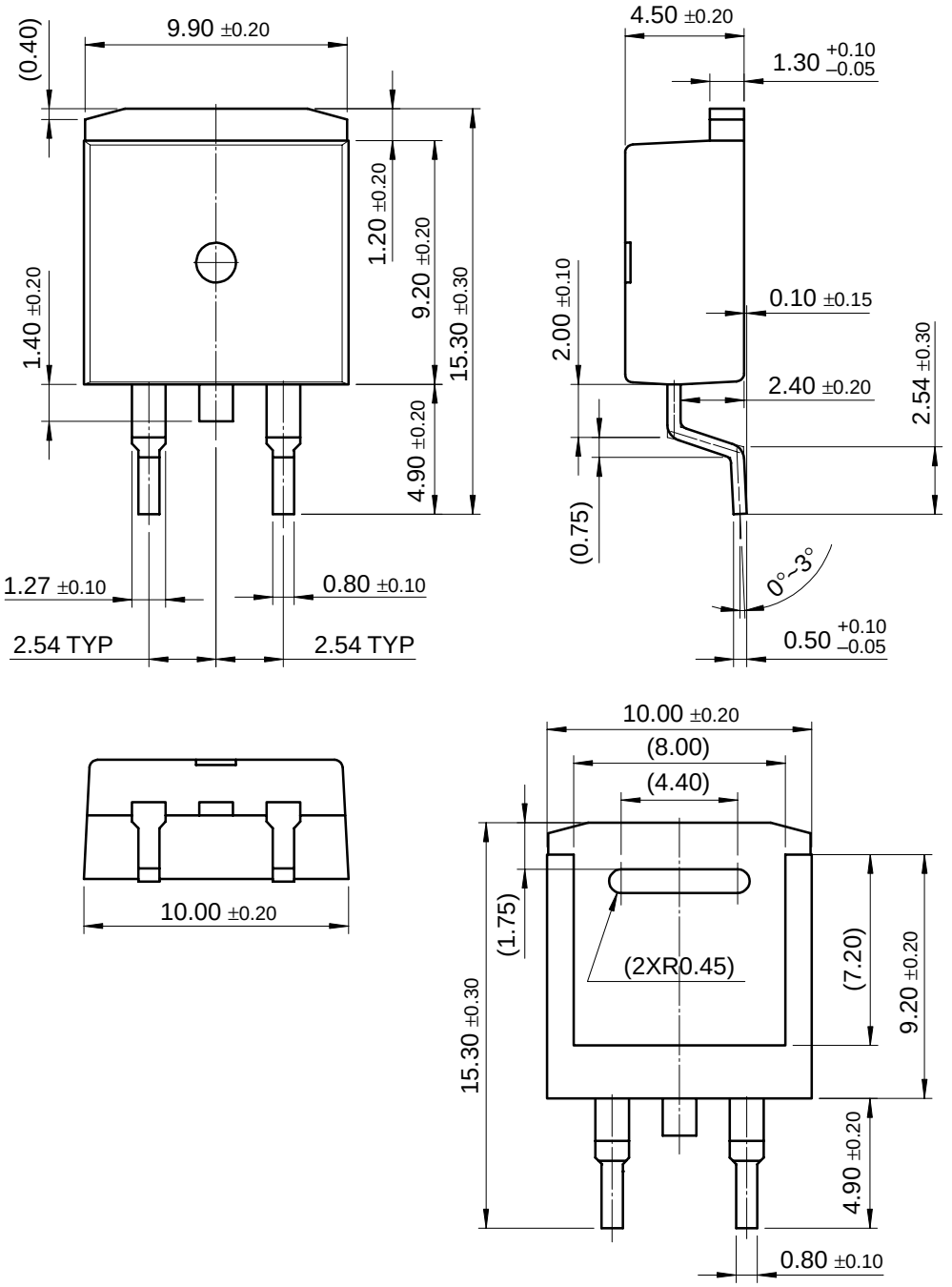
**Peak Diode Recovery dv/dt Test Circuit & Waveforms**



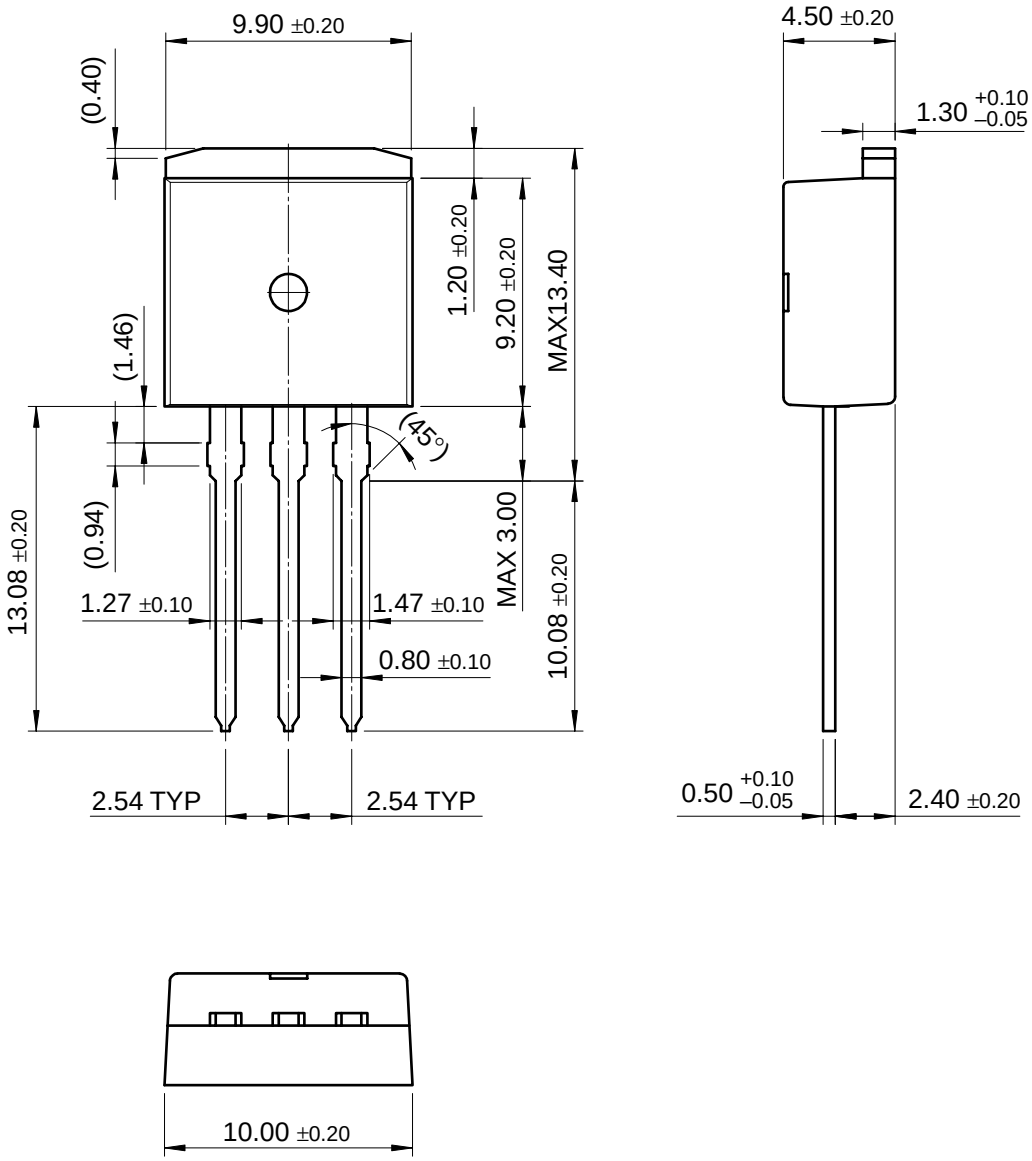
**Package Dimensions**

# $D^2PAK$



**Package Dimensions** (Continued)

# $I^2PAK$



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FASTr™
FRFET™
GlobalOptoisolator™
GTO™
HiSeC™
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## PRODUCT STATUS DEFINITIONS

### Definition of Terms

| Datasheet Identification | Product Status | Definition |
|---|---|---|
| Advance Information | Formative or In Design | This datasheet contains the design specifications for product development. Specifications may change in any manner without notice. |
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| No Identification Needed | Full Production | This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design. |
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FQB50N06L
60V N-Channel Logic level QFET

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## General description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.
This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for low voltage applications such as DC/DC converters, high efficiency switching for power management in portable and battery operated products.

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## Features

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- Low gate charge ( typical 24.5 nC)
- Low Crss ( typical 90 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability
- 175°C maximum junction temperature rating

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## Product status/pricing/packaging

| Product | Product status | Pricing* | Package type | Leads | Packing method |
|---|---|---|---|---|---|
| FQB50N06LTM | Full Production | $0.87 | TO-263(D2PAK) | 2 | TAPE REEL |

* 1,000 piece Budgetary Pricing

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Models

| Package & leads | Condition | Temperature range | Software version | Revision date |
|---|---|---|---|---|
| PSPICE | | | | |
| TO-263(D2PAK)-2 | Electrical/Thermal | -55°C to 175°C | 9 | Jan 12, 2000 |

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