Bt473

110 MHz Monolithic CMOS Triple 8-bit True-Color RAMDAC™

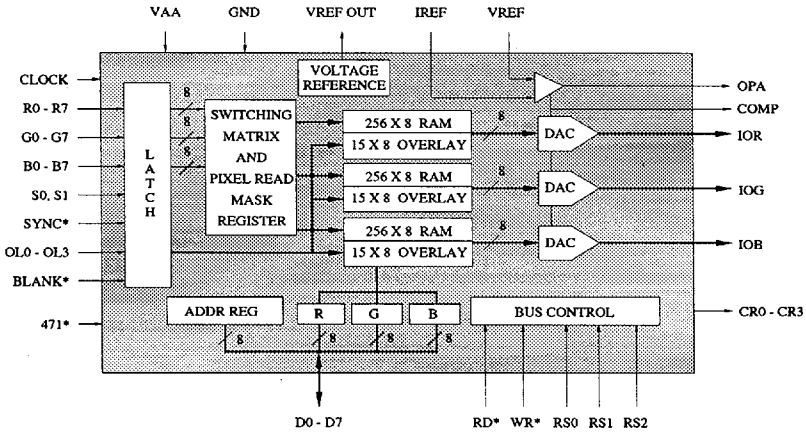
Distinguishing Features

- Bt471/478 Software Compatibility
- 110, 80, 66, 50, 35 MHz Operation
- Triple 8-bit D/A Converters
- Three 256 x 8 Color Palette RAMs
- Three 15 x 8 Overlay Registers
- RS-343A-Compatible Outputs
- Sync on All Three Channels
- Programmable Pedestai (0 or 7.5 IRE)
- On-Chip Voltage Reference
- Standard MPU Interface
- +5 V CMOS Monolithic Construction
- 68-pin PLCC Package
- Typical Power Dissipation: 1.1 W

Applications

- High-Resolution Color Graphics
- CAE/CAD/CAM
- Image Processing
- Instrumentation
- Desktop Publishing

Functional Block Diagram



Product Description

The Bt473 true-color RAMDAC is designed specifically for true-color computer graphics. It has three 256 x 8 color lookup tables with triple 8-bit video D/A converters to support 24-bit true-color operation. In addition, 8-bit pseudo- color, 8-bit true-color, and 15-bit true-color operations are supported.

Features include a programmable pedestal (0 or 7.5 IRE) and optional on-chip voltage reference. The 15 overlay registers provide, for example, overlaying cursors, grids, menus, and EGA emulation. Also supported are a pixel read mask register and sync generation on all three channels.

An external current reference, an external voltage reference, or the internal voltage reference may be used.

The Bt473 generates RS-343A-compatible video signals into a doubly-terminated 75 Ω load. Differential and integral linearity errors are guaranteed to be a maximum of ±1 LSB over the full temperature range.

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L473001 Rev. I

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Circuit Description

MPU Interface

As illustrated in the functional block diagram, the Bt473 supports a standard MPU bus interface, allowing the MPU direct access to the color palette RAM and overlay color registers.

The RS0–RS2 select inputs specify whether the MPU is accessing the address register, color palette RAM, overlay registers, or read mask register as shown in Table 1. The 8-bit address register is used to address the color palette RAM and overlay registers, eliminating the requirement for external address multiplexers. ADDR0 corresponds to D0 and is the least significant bit.

Writing Color Palette RAM Data

To write color data, the MPU writes the address register (RAM write mode) with the address of the color palette RAM location to be modified. The MPU performs three successive write cycles (8 bits each of red, green, and blue), using RS0–RS2 to select the color palette RAM. After the blue write cycle, the 3 bytes of color information are concatenated into a 24-bit word and written to the location specified by the address register. The address register then increments to the next location, which the MPU may modify by writing another sequence of red, green, and blue data. A block of color values in consecutive locations may be written to by writing the start address and performing continuous R, G, B write cycles until the entire block has been written. (See Figure 1.)

Reading Color Palette RAM Data

To read color palette RAM data, the MPU loads the address register (RAM read mode) with the address of the color palette RAM location to be read. The contents of the color palette RAM at the specified address are copied into the RGB registers, and the address register is incremented to the next RAM location. The MPU performs three successive read cycles (8 bits each of red, green, and blue), using RS0–RS2 to select the color palette RAM. Following the blue read cycle, the contents of the color palette RAM at the address specified by the address register are copied into the RGB registers, and the address register increments. A block of color values in consecutive locations may be read by writing the start address and performing continuous R, G, B read cycles until the entire block has been read.

Writing Overlay Color Data

To write overlay color data, the MPU writes the address register (overlay write mode) with the address of the overlay location to be modified. The MPU performs three successive write cycles (8 bits each of red, green, and blue), using RS0–RS2 to select the overlay registers. After the blue write cycle, the 3 bytes of color information are concatenated into a 24-bit word and written to the overlay location specified by the address register. The address register then increments to the next location, which the MPU may modify by writing another sequence of red, green, and blue data. A block of color values in consecutive locations may be written to by writing the start address and performing continuous R, G, B write cycles until the entire block has been written.

Reading Overlay Color Data

To read overlay color data, the MPU loads the address register (overlay read mode) with the address of the overlay location to be read. The contents of the overlay register at the specified address are copied into the RGB registers, and the address register is incremented to the next overlay location. The MPU performs three successive read cycles (8 bits each of red, green, and blue), using RS0–RS2 to select the overlay registers.

RS2	RS1	RS0	Addressed by MPU
0	0	0	address register (RAM write mode)
0	1	1	address register (RAM read mode)
0	0	1	color palette RAMs
0	1	0	pixel read mask register
1	0	0	address register (overlay write mode)
1	1	1	address register (overlay read mode)
1	0	1	overlay registers
1	1	0	command register

Table 1. Control Input Truth Table.

Circuit Description *(continued)*

Following the blue read cycle, the contents of the overlay location at the address specified by the address register are copied into the RGB registers, and the address register increments. A block of color values in consecutive locations may be read by writing the start address and performing continuous R, G, B read cycles until the entire block has been read.

Additional Information

When accessing the color palette RAM, the address register resets to $00 following a blue read or write cycle to RAM location $FF. While accessing the overlay color registers, the 4 most significant bits of the address register (ADDR4–7) are ignored.

The MPU interface operates asynchronously to the pixel clock. Data transfers that occur between the color palette RAM/overlay registers and the color registers (R, G, and B in the block diagram) are synchronized by internal logic and take place in the period between MPU accesses. Occasional accesses to the color palette RAM can be made without noticeable disturbance on the display screen; however, operations requiring frequent access to the color palette (such as, block fills of the color palette) should take place during the blanking interval.

To keep track of the red, green, and blue read/write cycles, the address register has 2 additional bits(ADDRa and ADDRb) that count modulo three, as shown in Table 2. They are reset to zero when the MPU writes to the address register and are not reset to zero when the MPU reads the address register. The MPU does not have access to these bits. The other 8 bits of the address register, incremented following a blue read or write cycle (ADDR0–7), are accessible to the MPU. They are used to address color palette RAM locations and overlay registers, as specified in table 2. The MPU may read the address register at any time without modifying its contents or the existing read/write mode.

8-Bit / 6-Bit Operation

The command register specifies whether the MPU is reading and writing 8 bits or 6 bits of color information each cycle.

For 8-bit operation, D0 is the LSB and D7 is the MSB of color data.

For 6-bit operation, color data is contained on the lower 6 bits of the data bus. D0 is the LSB and D5 is the MSB of color data. When writing color data, D6 and D7 are ignored. During color read cycles, D6 and D7 will be logical zeros. In the 6-bit mode, the Bt473's full-scale output current will be about 1.5-percent lower than when in the 8-bit mode. This is because the 2 LSBs of each 8-bit DAC are logical zeros in the 6-bit mode.

Bt471 Mode

The Bt473 can be forced into a Bt471 operating mode after power-up by holding the 471* external control pin low. In this mode, 8-bit pseudo-color pixel address data is enabled by R7–R0. This also forces 0 IRE setup and 6-bit DAC operation. The S0 and S1 inputs cannot override the enabled 8-bit pseudo-color (red) mode while the 471* pin is held low.

Color Modes

Four color modes are supported by the Bt473: 24-bit true color, 15-bit true color, 8-bit true color, and 8-bit pseudo color. The mode of operation is determined by the S0 and S1 inputs in conjunction with CR7 and CR6 of the command register. S0 and S1 are pipelined to maintain synchronization with the R0–R7, G0–G7, B0–B7, and OL0–OL3 pixel and overlay data inputs.

Table 3 lists the modes of operation.

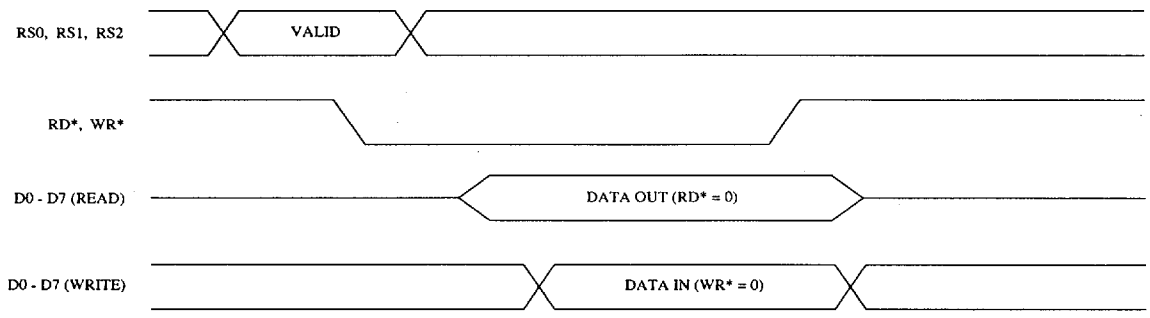


Figure 1. MPU Read/Write Timing.

Circuit Description *(continued)*

	Value	RS2	RS1	RS0	Addressed by MPU
ADDRa, b (counts modulo 3)	00 01 10	x x x	0 0 0	1 1 1	red value green value blue value
ADDR0–7 (counts binary)	$00–$FF xxxx 0000 xxxx 0001 : xxxx 1111	0 1 1 : 1	0 0 0 : 0	1 1 1 : 1	color palette RAMs reserved overlay color 1 : overlay color 15

Table 2. Address Register (ADDR) Operation.

OL3–OL0	S1, S0	CR7, CR6	Mode	R7–R0	G7–G0	B7–B0
1111 : 0001	xx : xx	xx : xx	overlay color 15 : overlay color 1	$xx : $xx	$xx : $xx	$xx : $xx
0000 0000 0000 0000	00 00 00 00	00 01 10 11	24-bit true color 24-bit true color 24-bit true color reserved	R7–R0 R7–R0 R7- R0 reserved	G7–G0 G7–G0 G7–G0 reserved	B7–B0 B7–B0 B7–B0 reserved
0000 0000 0000 0000	01 01 01 01	00 01 10 11	24-bit true-color bypass 24-bit true-color bypass 24-bit true-color bypass reserved	R7–R0 R7–R0 R7–R0 reserved	G7–G0 G7–G0 G7–G0 reserved	B7–B0 B7–B0 B7–B0 reserved
0000 0000 0000 0000	10 10 10 10	00 01 10 11	8-bit pseudo color (red) 8-bit pseudo color (green) 8-bit pseudo color (blue) 15-bit true color	P7–P0 ignored ignored 0rrrrrgg	ignored P7–P0 ignored gggbbbbb	ignored ignored P7–P0 ignored
0000 0000 0000 0000	11 11 11 11	00 01 10 11	8-bit true-color bypass (red) 8-bit true-color bypass (green) 8-bit true-color bypass (blue) 15-bit true-color bypass	rrrgggbb ignored ignored 0rrrrrgg	ignored rrrgggbb ignored gggbbbbb	ignored ignored rrrgggbb ignored

Table 3. Color Operation Modes.

Circuit Description *(continued)*

24-Bit True-Color Mode

Every clock cycle, 24 bits of RGB color information may be input to the Bt473. The 24 bits of pixel information are input by the R0–R7, G0–G7, and B0–B7 inputs. R0–R7 address the red color palette RAM, G0–G7 address the green color palette RAM, and B0–B7 address the blue color palette RAM. Each RAM provides 8 bits of color information to the corresponding D/A converter. The pixel read mask register is used in this mode.

24-Bit True-Color Bypass Mode

Every clock cycle, 24 bits of pixel information may be input to the Bt473. The 24 bits of pixel information are input by the R0–R7, G0–G7, and B0–B7 inputs. R0–R7 drive the red DAC directly, G0–G7 drive the green DAC directly, and B0–B7 drive the blue DAC directly. The color palette RAMs and pixel read mask register are bypassed.

8-Bit Pseudo-Color Mode

Every clock cycle, 8 bits of pixel information may be input to the Bt473. The 8 bits of pixel information (P0–P7) are input by the R0–R7, G0–G7, or B0–B7 inputs, as specified by CR7 and CR6. All three color palette RAMs are addressed by the same 8 bits of pixel data (P0–P7). Each RAM provides 8 bits of color information to the corresponding D/A converter. The pixel read mask register is used in this mode.

8-Bit True-Color Bypass Mode

Every clock cycle, 8 bits of pixel information may be input to the Bt473 by the R0–R7, G0–G7, or B0–B7 inputs, as specified by CR7 and CR6:

R0–R7 Inputs Selected	G0–G7 Inputs Selected	B0–B7 Inputs Selected	Input Format
R7	G7	B7	R7
R6	G6	B6	R6
R5	G5	B5	R5
R4	G4	B4	G7
R3	G3	B3	G6
R2	G2	B2	G5
R1	G1	B1	B7
R0	G0	B0	B6

As specified in the above table, 3 bits of red, 3 bits of green, and 2 bits of blue data are input. The 3 MSBs of the red and green DACs are driven directly by the inputs, while the 2 MSBs of the blue DAC are driven directly. The 5 LSBs for the red and green DACs, and the 6 LSBs for the blue DAC, are logical zeros. The color palette RAMs and pixel read mask register are bypassed.

15-Bit True-Color Mode

Every clock cycle, 15 bits of pixel information may be input to the Bt473. The 15 bits of pixel information (5 bits each of red, green, and blue) are input by the R0–R7 and G0–G7 inputs, as specified in the pixel table below. Five LSBs from red, green, and blue address 32 locations of each corresponding RAM. R6–R2 address 32 locations of the red color palette RAM; R1, R0, G7, G6, and G5 address 32 locations of the green color palette RAM, and G5–G0 address 32 locations of the blue color palette RAM. The 3 MSBs of red, green, and blue are forced to zero. Each RAM provides 8 bits of color information to the corresponding D/A converter. The pixel read mask register is used in this mode.

15-Bit True-Color Bypass Mode

Every clock cycle, 15 bits of pixel information (5 bits each of red, green, and blue) may be input to the Bt473 by the R0–R7 and G0–G7 inputs as specified below.

The 5 MSBs of the red, green, and blue DACs are driven directly by the inputs. The 3 LSBs are logical zeros. The color palette RAMs and pixel read mask register are bypassed.

Pixel Inputs	Input Format
R7	0
R6	R7
R5	R6
R4	R5
R3	R4
R2	R3
R1	G7
R0	G6
G7	G5
G6	G4
G5	G3
G4	B7
G3	B6
G2	B5
G1	B4
G0	B3

Circuit Description *(continued)*

Overlays

The overlay inputs, OL0–OL3, have priority regardless of the color mode, as detailed in Table 3.

Pixel Read Mask Register

The 8-bit pixel read mask register is implemented as three 8-bit pixel read mask registers, one each for the R0–R7, G0–G7, and B0–B7 inputs. When writing to the pixel read mask register, the same data is written to all three registers. The read mask registers are located just before the color palette RAMs. Thus, they are used only in the 24-bit true-color and 8-bit pseudo-color modes, since these are the only modes that use the color palette RAMs.

The contents of the pixel read mask register, which may be accessed by the MPU at any time, are bitwise logically ANDed with the 8-bit inputs before addressing the color palette RAMs. Bit D0 of the pixel read mask register corresponds to pixel input P0 (R0, G0, or B0, depending on the mode). Bit D0 also corresponds to data bus bit D0.

The Pixel read mask register is not initialized. For proper operation, it must be initialized by the user after power-up.

Programmable Setup

The command register specifies whether a 0 IRE or 7.5 IRE blanking pedestal is to be used.

Video Generation

The SYNC* and BLANK* inputs, also latched on the rising edge of CLOCK to maintain synchronization with the color data (see Figure 2), add appropriately weighted currents to the analog outputs. This produces the specific output levels required for video applications, as illustrated in Figures 3 and 4. Tables 4 and 5 detail how the SYNC* and BLANK* inputs modify the output levels.

The analog outputs of the Bt473 can directly drive a 37.5 Ω load, such as a doubly-terminated 75 Ω coaxial cable.

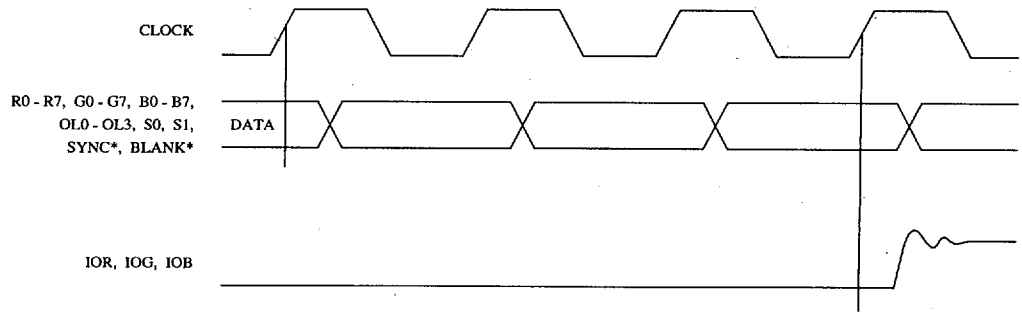
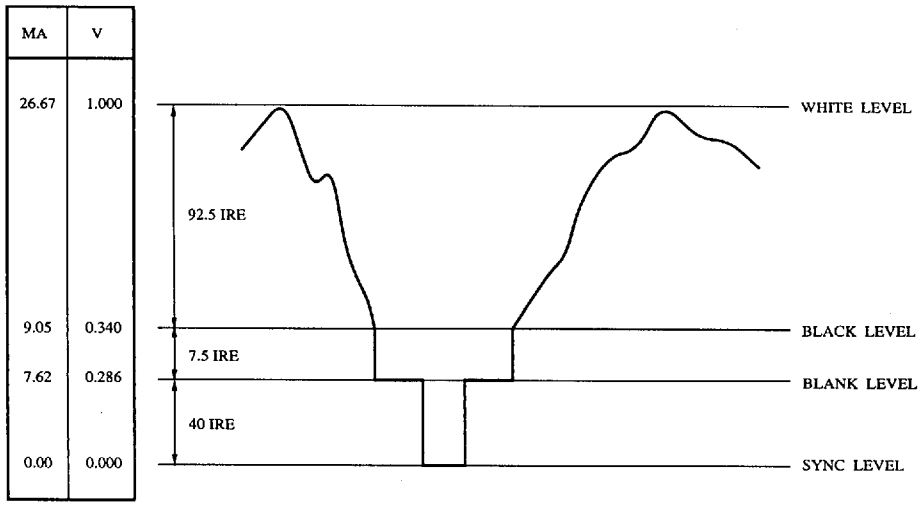


Figure 2. Video Input/Output Timing.

Circuit Description *(continued)*



Note: 75 Ω doubly-terminated load, SETUP = 7.5 IRE, VREF = 1.235 V, and RSET = 143 Ω. RS-343A levels and tolerances are assumed on all levels.

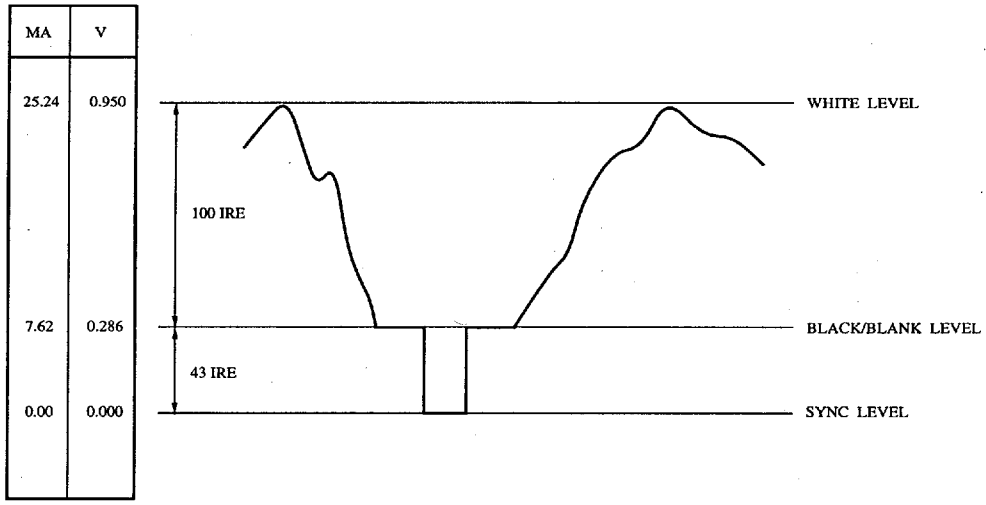
Figure 3. Composite Video Output Waveforms (SETUP = 7.5 IRE).

Description	Iout (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	1	1	$FF
DATA	data + 9.05	1	1	data
DATA - SYNC	data + 1.44	0	1	data
BLACK	9.05	1	1	$00
BLACK - SYNC	1.44	0	1	$00
BLANK	7.62	1	0	$xx
SYNC	0	0	0	$xx

Note: Typical with full-scale IOR, IOG, IOB = 26.67 mA, SETUP = 7.5 IRE, VREF = 1.235 V, and RSET = 143 Ω.

Table 4. Video Output Truth Table (SETUP = 7.5 IRE).

Circuit Description *(continued)*



Note: 75 Ω doubly-terminated load, SETUP = 0 IRE, VREF = 1.235 V, and RSET = 143 Ω. RS-343A levels and tolerances are assumed on all levels.

Figure 4. Composite Video Output Waveforms (SETUP = 0 IRE).

Description	Iout (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	25.24	1	1	$FF
DATA	data + 7.62	1	1	data
DATA - SYNC	data	0	1	data
BLACK	7.62	1	1	$00
BLACK - SYNC	0	0	1	$00
BLANK	7.62	1	0	$xx
SYNC	0	0	0	$xx

Note: Typical with full-scale IOR, IOG, IOB = 25.24 mA, SETUP = 0 IRE, VREF = 1.235 V, and RSET = 143 Ω.

Table 5. Video Output Truth Table (SETUP = 0 IRE).

Internal Registers

Command Register

The command register may be written to or read by the MPU at any time and is not initialized. It must be initialized by the user after power-up for proper operation. CR0 is the least significant bit and corresponds to D0.

CR7, CR6	Color mode select	These bits are used to control the various color modes, as specified in Table 3.
CR5	Setup select (0) 0 IRE (1) 7.5 IRE	This bit is used to specify either a 0 IRE (logical zero) or 7.5 IRE (logical one) blanking pedestal.
CR4	8-bit / 6-bit color select (0) 6 bits (1) 8 bits	This bit specifies whether the MPU is reading and writing 8 bits (logical one) or 6 bits (logical zero) of color information each cycle. For 8-bit operation, D7 is the most significant data bit during color read/write cycles. For 6-bit operation, D5 is the most significant data bit during color read/write cycles (D6 and D7 are ignored during color write cycles and logical zeros during color read cycles).
CR3–CR0	CR3–CR0 outputs	These bits are output onto the CR3–CR0 pins.

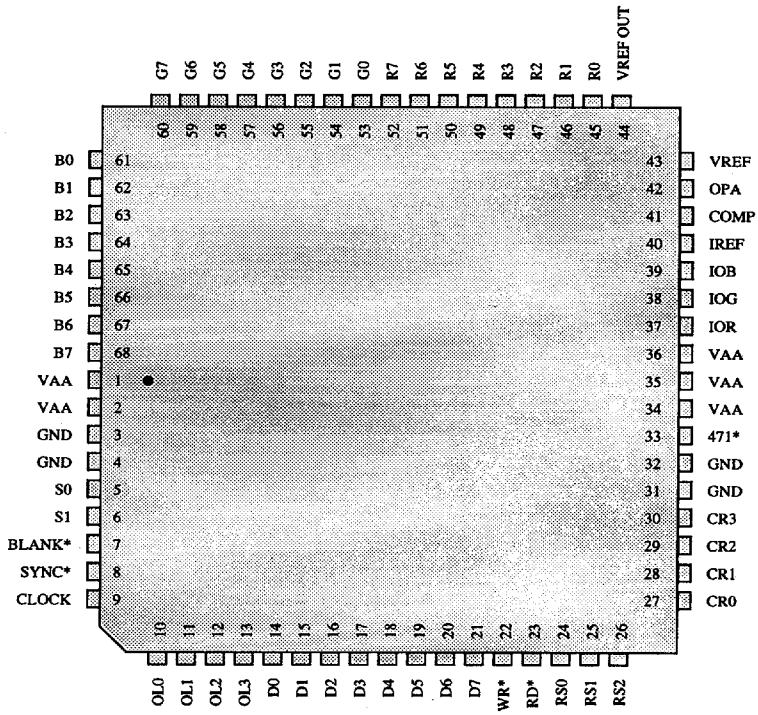
Pin Descriptions

Pin Name	Description
BLANK*	Composite blank control input (TTL compatible). A logical zero drives the analog outputs to the blanking level, as detailed in Tables 4 and 5. It is latched on the rising edge of CLOCK. When BLANK* is a logical zero, the pixel and overlay inputs are ignored.
SYNC*	Composite sync control input (TTL compatible). A logical zero on this input switches off a 40 IRE current source on the analog outputs (see Figures 3 and 4). SYNC does not override any other control or data input; therefore, it should be asserted only during the blanking interval. SYNC* is latched on the rising edge of CLOCK. If sync information is not required on the video outputs, SYNC should be connected to GND.
CLOCK	Clock input (TTL compatible). The rising edge of CLOCK latches the R0–R7, G0–G7, B0–B7, S0, S1, OL0–OL3, SYNC*, and BLANK* inputs. It is typically the pixel clock rate of the video system. It is recommended that CLOCK be driven by a dedicated TTL buffer to avoid reflection-induced jitter. Refer to the PC Board Layout Considerations section for critical layout criteria.
R0–R7, G0–G7, B0–B7	Red, green, and blue pixel select inputs (TTL compatible). These inputs specify, on a pixel basis, which 1 of the 256 entries in the red, green, and blue color palette RAMs is to be used to provide color information. These inputs are latched on the rising edge of CLOCK. R0, G0, and B0 are the LSBs. Unused inputs should be connected to GND.
S0, S1	Color mode select inputs (TTL compatible). These inputs specify the mode of operation as detailed in Table 3. They are latched on the rising edge of CLOCK.
OL0–OL3	Overlay select inputs (TTL compatible). These inputs specify which palette is to be used to provide color information, as detailed in Table 3. When accessing the overlay palette, the R0–R7, G0–G7, B0–B7, S0, and S1 inputs are ignored. OL0–OL3 are latched on the rising edge of CLOCK. OL0 is the LSB. Unused inputs should be connected to GND.
IOR, IOG, IOB	Red, green, and blue current outputs. These high-impedance current sources can directly drive a doubly-terminated 75 Ω coaxial cable (Figures 5, 6, and 7 in the PC Board Layout Considerations section).
IREF	Full-scale adjust control. When voltage reference is used (Figures 5 and 6), a resistor (RSET) connected between this pin and GND controls the magnitude of the full-scale video signal. The relationship between RSET and the full-scale output current on each output is: RSET (Ω) = K*1000 * VREF (V) / Iout (mA) K is defined in the table and note below. Pedestal / K (with SYNC) / K (without SYNC): 7.5 IRE: 3.063 / 2.205 0 IRE: 2.898 / 2.040 When an external current reference is used (Figure 7), the relationship between IREF and the full-scale output current on each output is: IREF (mA) = Iout (mA) / K *Note :* The K values in this table represent an ideal DAC circuit. However, because of a small difference (~3 percent) between the actual drain-source voltages on the DAC output transistor and the reference transistor, an RSET value of 143 Ω is recommended.

Pin Descriptions *(continued)*

Pin Name	Description
COMP	Compensation pin. If an external voltage reference is used (Figures 5 and 6), this pin should be connected to OPA. If an external current reference is used (Figure 7), this pin should be connected to IREF. A 0.1 µF ceramic capacitor must be used to bypass this pin to VAA. The COMP capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. The PC Board Layout Considerations section contains critical layout criteria.
VREF	Voltage reference input. If a voltage reference is used (Figures 5 and 6), it must supply this input with a 1.2 V (typical) reference. If an external current reference is used (Figure 7), this pin should be biased with the VREF OUT pin. A 0.1 µF ceramic capacitor is used to decouple this input to GND, as shown in Figures 5, 6, and 7. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. When the internal reference is used, this pin should not drive any external circuitry, except the decoupling capacitor. Refer to the PC Board Layout Considerations section for critical layout criteria.
OPA	Reference amplifier output. If a voltage reference is used (Figures 5 and 6), this pin must be connected to COMP. When an external current reference is used (Figure 7), this pin should be left floating.
VREF OUT	Voltage reference output. This output provides a 1.2 V (typical) reference, and may be connected directly to the VREF pin. If the on-chip reference is not used, this pin may be left floating in external voltage reference mode. (See Figure 6.) Up to four Bt473s may be driven by this output.
VAA	Analog power. All VAA pins must be connected together on the same PCB plane to prevent latchup. Refer to the PC Board Layout Considerations section for critical layout criteria.
GND	Analog ground. All GND pins must be connected together on the same PCB plane to prevent latchup. Refer to the PC Board Layout Considerations section for critical layout criteria.
WR*	Write control input (TTL compatible). D0–D7 data is latched on the rising edge of WR*, and RS0–RS2 are latched on the falling edge of WR* during MPU write operations. RD* and WR* should not be asserted simultaneously. (See Figure 1, and Figure 8 in the Timing Waveforms section.)
RD*	Read control input (TTL compatible). To read data from the device, RD* must be a logical zero. RS0–RS2 are latched on the falling edge of RD* during MPU read operations. RD* and WR* should not be asserted simultaneously. (See Figures 1 and 8.)
RS0, RS1, RS2	Register select inputs (TTL compatible). RS0–RS2 specify the type of read or write operation being performed, as shown in Tables 1 and 2.
D0–D7	Data bus (TTL compatible). Data is transferred into and out of the device over this 8-bit bidirectional data bus. D0 is the least significant bit.
CR0–CR3	Control outputs (TTL compatible). These outputs are used to control application-specific features. The output values are determined by the command register. (See Figure 8.)
471*	This pin forces the device into a Bt471 operating mode (i.e., it enables 8-bit pseudo-color mode with R7–R0, 0 IRE setup, and 6-bit DAC operation). This pin must be held at a logical-zero level to maintain this mode of operation.

Pin Descriptions *(continued)*



PC Board Layout Considerations

PC Board Considerations

For optimum performance of the Bt473, proper CMOS RAMDAC layout techniques should be studied in the Bt451/7/8 Evaluation Module Operation and Measurements, Application Note (AN-16), before PC board layout is begun. This application note can be found in Brooktree's *Applications Handbook*.

The layout should be optimized for lowest noise on the Bt473 power and ground planes by providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. The ground plane must provide a low-impedance return path for the digital circuits. A PC board with a minimum of four layers is recommended, with layers 1 (top) and 4 (bottom) for signals and layers 2 and 3 for power and ground.

Component Placement

Components should be placed as close as possible to the associated RAMDAC pin. Whenever possible, components should be placed so traces can be connected point to point.

The optimum layout enables the Bt473 to be located as close as possible to the power supply connector and the video output connector.

Ground Planes

For optimum performance, a common digital and analog ground plane is recommended.

Power Planes

Separate digital and analog power planes are recommended. The digital power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt473 power pins, VREF circuitry, and COMP and VREF decoupling. There should be at least a 1/8-inch gap between the digital power plane and the analog power plane.

The analog power plane should be connected to the digital power plane (VCC) at a single point through a ferrite bead, as illustrated in Figures 5, 6, and 7. This bead should be located within 3 inches of the Bt473. The bead provides resistance to switching currents, acting as a resistance at high frequencies. A low-resistance bead should be used, such as Ferroxcube 5659065-3B, Fair-Rite 2743001111, or TDK BF45-4001.

Device Decoupling

For optim13 ·œerformance, all capacitors should be located as close as possible to the device, and the shortest possible leads (consistent with reliable operation) should be used to reduce the lead inductance. Chip capacitors are recommended for minimum lead inductance. Radial lead ceramic capacitors may be substituted for chip capacitors and are better than axial lead capacitors for self-resonance. Values are chosen to have self-resonance above the pixel clock.

Power Supply Decoupling

The best power supply decoupling performance is obtained with a 0.1 µF ceramic capacitor, decoupling each of the two groups of VAA pins to GND. For operation above 75 MHz, a 0.1 µF capacitor in parallel with a 0.01 µF chip capacitor is recommended. The capacitors should be placed as close as possible to the device VAA and GND pins and connected with short, wide traces.

The 10 µF capacitor shown in Figures 5, 6, and 7 is for low-frequency power supply ripple; the 0.1 µF capacitors are for high-frequency power supply noise rejection.

When a linear regulator is used, the power-up sequence must be verified to prevent latchup. A linear regulator is recommended to filter the analog power supply if the power supply noise is greater than or equal to 200 mV. This is especially important when a switching power supply is used, and the switching frequency is close to the raster scan frequency. About 10 percent of the power supply hum and ripple noise less than 1 MHz will couple onto the analog outputs.

COMP Decoupling

The COMP pin must be decoupled to VAA, typically with a 0.1 µF ceramic capacitor. Low-frequency supply noise will require a larger value. The COMP capacitor must be as close as possible to the COMP and VAA pins. A surface-mount ceramic chip capacitor is preferred for minimal lead inductance. Lead inductance degrades the noise rejection of the circuit. Short, wide traces will also reduce lead inductance.

If the display has a ghosting problem, additional capacitance in parallel with the COMP capacitor may help.

VREF Decoupling

A 0.1 µF ceramic capacitor should be used to decouple this input to GND.

PC Board Layout Considerations *(continued)*

Digital Signal Interconnect

The digital inputs to the Bt473 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power plane or analog output signals.

Most of the noise on the analog outputs will be caused by excessive edge rates (less than 3 ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge rates should not be faster than necessary, as feedthrough noise is proportional to the digital edge rates. Lower-speed applications will benefit from using lower-speed logic (3–5 ns edge rates) to reduce data-related noise on the analog outputs.

Transmission lines will mismatch if the lines do not match the source and destination impedance. This will degrade signal fidelity if the line length reflection time is greater than one fourth the signal edge time (refer to Brooktree Application Notes AN-11 and AN-12). Line termination or line-length reduction is the solution. For example, logic edge rates of 2 ns require line lengths of less than 4 inches without use of termination. Ringing may be reduced by damping the line with a series resistor (30–300 Ω). The RS-select inputs and RD*/WR* lines must be verified for proper levels with no ringing, undershoot, or overshoot. Ringing on these lines can cause improper operation.

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge rates (rise/fall time), minimizing ringing with damping resistors, and minimizing coupling through PC board capacitance by routing the digital signals at a 90 degree angle to any analog signals.

The clock driver and all other digital devices must be adequately decoupled to prevent noise generated by the digital devices from coupling into the analog circuitry.

Clock Interfacing

The Bt473 requires a pixel clock with monotonic clock edges for proper operation. Impedance mismatch on the pixel clock line will induce reflections on the pixel clock, which may cause erratic operation.

The Pixel Clock Pulse Width High Time and Pixel Clock Pulse Width Low Time minimum specifications (see the AC Characteristics section) must not be violated, or erratic operation can occur.

The pixel clock line must be terminated to prevent impedance mismatch. A series termination of 33–68 Ω placed at the pixel clock driver may be used, or a parallel termination may be used at the pixel clock input to the RAMDAC. A parallel termination of 220 Ω to VCC and 330 Ω to ground will provide a Thevenin equivalent of a 110 Ω termination, which is normally sufficient to absorb reflections. The series or parallel resistor values should be adjusted to provide the optimum clock signal fidelity.

For 110 MHz operation, the clock signal requires a constant impedance line between the clock driver and the clock input pin. This signal should be driven by a dedicated driver, and should be terminated at the device input pin. At 110 MHz, CLOCK rise/fall times should be controlled to maximize the clock high and low times. This will help minimize duty cycle skew.

MPU Control Signal Interfacing

The Bt473 uses the RD*, WR*, and RS lines to determine which MPU accesses will take place. Glitches or ringing on any of these lines may cause improper MPU operation. When a VGA controller with edge rate control is used on these lines, a series termination is not necessary. In non-VGA controller application or in applications where the MPU control signals are daisy chained, a series termination, pull-down resistors, or additional capacitance to ground should be used to prevent glitches that could cause improper MPU accesses.

Analog Signal Interconnect

The Bt473 should be located as close as possible to the output connectors to minimize noise pickup and reflections caused by impedance mismatch.

The analog outputs are susceptible to crosstalk from digital lines; digital traces must not be routed under or adjacent to the analog output traces.

To maximize the high-frequency power supply rejection, the video output signals should not overlay the analog power plane.

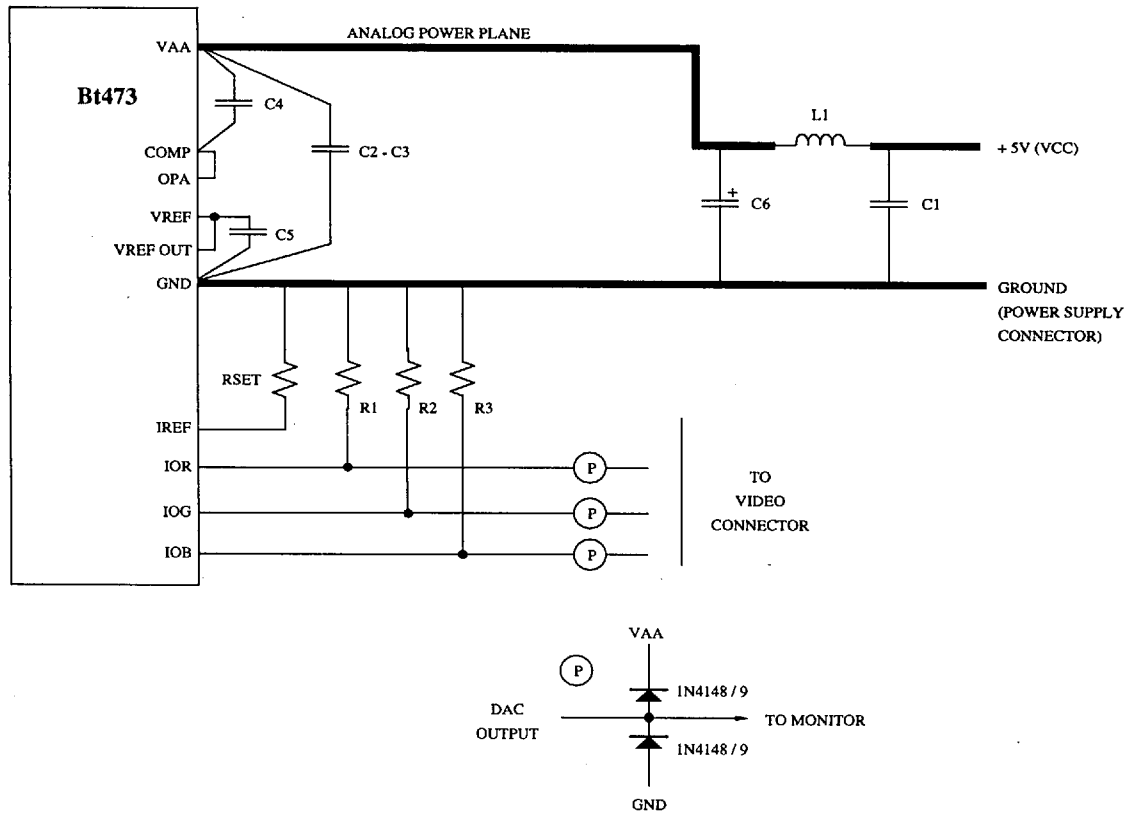
For maximum performance, the analog video output impedance, cable impedance, and load impedance should be the same. The load resistor connection between the video outputs and GND should be as close as possible to the Bt473 to minimize reflections. Unused analog outputs should be connected to GND.

Analog output video edges exceeding the CRT monitor bandwidth can be reflected, producing cable-length dependent ghosts. Simple pulse filters can reduce high-frequency energy, reducing EMI and noise. The filter impedance must match the line impedance.

Analog Output Protection

The Bt473 analog output should be protected against high-energy discharges, such as those from monitor arc-over or from hot-switching AC-coupled monitors. The diode protection circuit shown in Figures 5, 6, and 7 can prevent latchup under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 parts are low-capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

PC Board Layout Considerations *(continued)*



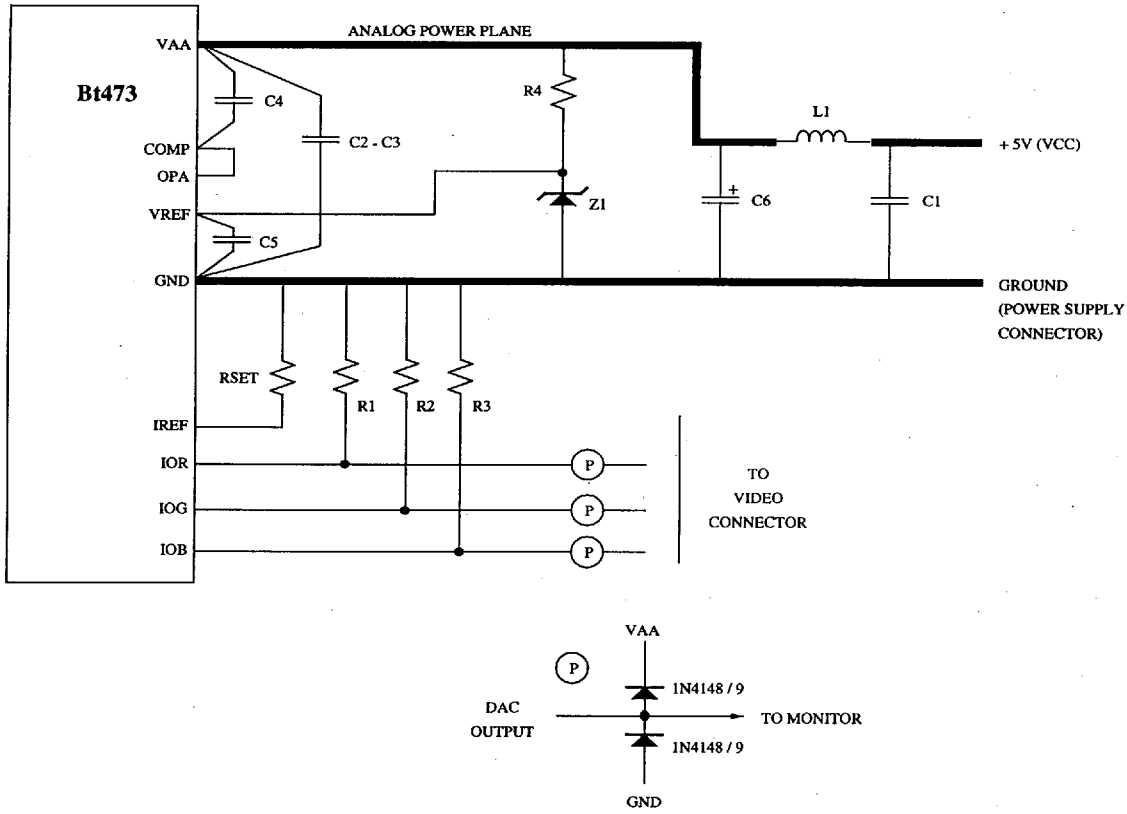
Note: Each set of VAA and GND pins must be separately decoupled.

Location	Description	Vendor Part Number
C1–C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 µF tantalum capacitor	Mallory CSR13G106KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
RSET	1% metal film resistor	Dale CMF-55C

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt473.

Figure 5. Typical Connection Diagram and Parts List (Internal Voltage Reference).

PC Board Layout Considerations *(continued)*



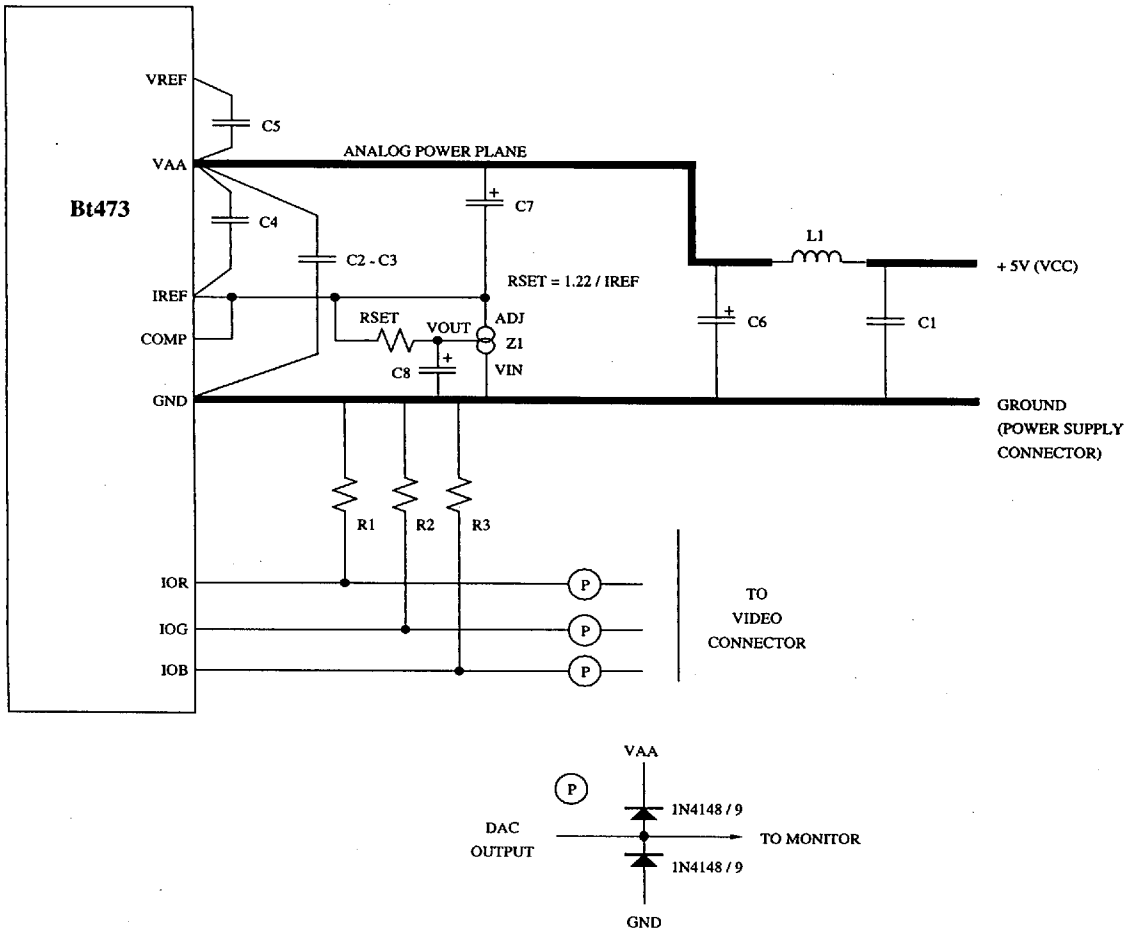
Note: Each set of VAA and GND pins must be separately decoupled.

Location	Description	Vendor Part Number
C1– C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 µF tantalum capacitor	Mallory CSR13G106KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
R4	1 kΩ 5% resistor	
RSET	1% metal film resistor	Dale CMF-55C
Z1	1.2 V voltage reference	National Semiconductor LM385BZ-1.2

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt473.

Figure 6. Typical Connection Diagram and Parts List (External Voltage Reference).

PC Board Layout Considerations *(continued)*



Note: Each set of VAA and GND pins must be separately decoupled.

Location	Description	Vendor Part Number
C1–C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 µF tantalum capacitor	Mallory CSR13G106KM
C7, C8	1 µF capacitor	Mallory CSR13G105KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
Z1	adjustable regulator	National Semiconductor LM337LZ
RSET	1% metal film resistor	Dale CMF-55C

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt473.

Figure 7. Typical Connection Diagram and Parts List (External Current Reference).

Application Information

Using Multiple Devices

When multiple Bt473s are being used, each Bt473 should have its own power plane ferrite bead.

Although the VREF OUT of a single Bt473 may drive multiple Bt473s, higher performance may be obtained if each RAMDAC uses its own reference. This will reduce the amount of color channel crosstalk and color palette interaction.

Each Bt473 must still have its own RSET resistor, analog output termination resistors, power supply bypass capacitors, COMP capacitor, and reference capacitors.

Reference Selection

An external voltage reference provides about 10 times the power supply rejection on the analog outputs than does an external current reference.

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat leaky inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. DAC power decoupling networks with large time constants should be avoided. They could delay VAA power to the device. Ferrite beads must be used only for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

Latchup can be prevented by ensuring that all VAA pins are at the same potential and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence ensures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA				
110, 80, 66 MHz Parts		4.75	5.00	5.25	V
50, 35 MHz Parts		4.5	5.00	5.5	V
Ambient Operating Temperature	TA	0		+70	°C
Output Load	RL		37.5		Ω
Voltage Reference Configuration					
Reference Voltage	VREF	1.12	1.235	1.358	V
Current Reference Configuration					
IREF Current	IREF				
Standard RS-343A		–3	–8.39	–10	mA
PS/2 Compatible		–3	–8.88	–10	mA

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				7.0	V
Voltage on any Signal Pin (Note 1)		GND–0.5		VAA + 0.5	V
Analog Output Short Circuit Duration to any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+150	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Resolution (each DAC)		8	8	8	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL			±1	LSB
Differential Linearity Error	DL			±1	LSB
Gray-Scale Error					
Using External Reference				±5	% Gray Scale
Using Internal Reference				±10	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs					
Input High Voltage	VIH	2.0		VAA + 0.5	V
Input Low Voltage	VIL	GND–0.5		0.8	V
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN			7	pF
Digital Outputs					
Output High Voltage (IOH = –400 µA)	VOH	2.4			V
Output Low Voltage (IOL = 3.2 mA)	VOL			0.4	V
3-State Current (D0–D7)	IOZ			50	µA
Output Capacitance	CDOUT			7	pF

See test conditions on next page.

DC Characteristics *(continued)*

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Gray Scale Current Range				20	mA
Output Current (Standard RS-343A)					
White Level Relative to Black		16.74	17.62	18.50	mA
Black Level Relative to Blank					
SETUP = 7.5 IRE		0.95	1.44	1.90	mA
SETUP = 0 IRE		0	5	50	µA
Blank Level		6.29	7.62	8.96	mA
Sync Level		0	5	50	µA
LSB Size			69.1		µA
DAC-to-DAC Matching			2	5	%
Output Compliance	VOC	–0.5		+1.5	V
Output Impedance	RAOUT		10		kΩ
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	CAOUT			30	pF
VREF Input Current	IREF IN		10		µA
VREF OUT Output Voltage	VREFOUT	1.08	1.2	1.32	V
VREF OUT Output Current	IREF OUT		100		µA
Power Supply Rejection Ratio (COMP = 0.1 µF, f = 1 kHz)	PSRR			0.5	% / % ΔVAA

Test conditions to generate RS-343A standard video signals (unless otherwise specified): "Recommended Operating Conditions" with external voltage reference, RSET = 143 Ω, and VREF = 1.235 V. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

When the internal voltage reference is used, RSET may require adjustment to meet these limits. Also, the gray-scale output current (white level relative to black) will have a typical tolerance of ±10 percent rather than the ±5 percent specified above.

Analog Output Levels—PS/2 Compatibility

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Output Current					
White Level Relative to Black		18.00	18.65	20.00	mA
Black Level Relative to Blank					
SETUP = 7.5 IRE		1.01	1.51	2.0	mA
SETUP = 0 IRE		0	5	50	µA
Blank Level		6.6	8	9.4	mA
Sync Level		0	5	50	µA

Test conditions to generate PS/2-compatible video signals (unless otherwise specified): "Recommended Operating Conditions" with external voltage reference, RSET = 143 Ω, and VREF = 1.235 V; or external current reference with IREF = –8.88 mA.

AC Characteristics

Parameter	Symbol	110 MHz Devices Min	Typ	Max	Units
Clock Rate	Fmax			110	MHz
RS0–RS2 Setup Time	1	10			ns
RS0–RS2 Hold Time	2	10			ns
RD* Asserted to Data Bus Driven	3	3			ns
RD* Asserted to Data Valid	4			40	ns
RD* Negated to Data Bus 3-Stated	5			20	ns
Read Data Hold Time	6	3			ns
Write Data Setup Time	7	10			ns
Write Data Hold Time	8	10			ns
CR0–CR3 Output Delay	9			100	ns
RD*, WR* Pulse Width Low	10	50			ns
RD*, WR* Pulse Width High	11	6*p14			ns
Pixel and Control Setup Time	12	3			ns
Pixel and Control Hold Time	13	3			ns
Clock Cycle Time (p14)	14	9.1			ns
Clock Pulse Width High Time	15	4			ns
Clock Pulse Width Low Time	16	4			ns
Analog Output Delay	17			30	ns
Analog Output Rise/Fall Time	18		2		ns
Analog Output Settling Time (Note 1)	19		13		ns
Clock and Data Feedthrough (Note 1)			–30		dB
Glitch Impulse (Note 1)			150		pV-sec
DAC-to-DAC Crosstalk			–23		dB
Analog Output Skew			0	2	ns
Pipeline Delay		4	4	4	Clocks
VAA Supply Current (Note 2)	IAA				
At 0° C			260	300	mA
At 70° C			230	270	mA

See test conditions at the end of this section.

AC Characteristics *(continued)*

Parameter	Symbol	80 MHz Devices			66 MHz Devices			Units
		Min	Typ	Max	Min	Typ	Max	
Clock Rate	Fmax			80			66	MHz
RS0–RS2 Setup Time	1	10			10			ns
RS0–RS2 Hold Time	2	10			10			ns
RD* Asserted to Data Bus Driven	3	3			3			ns
RD* Asserted to Data Valid	4			40			40	ns
RD* Negated to Data Bus 3-Stated	5			20			20	ns
Read Data Hold Time	6	5			5			ns
Write Data Setup Time	7	10			10			ns
Write Data Hold Time	8	10			10			ns
CR0–CR3 Output Delay	9			100			100	ns
RD*, WR* Pulse Width Low	10	50			50			ns
RD*, WR* Pulse Width High	11	6*p14			6*p14			ns
Pixel and Control Setup Time	12	3			3			ns
Pixel and Control Hold Time	13	3			3			ns
Clock Cycle Time (p14)	14	12.5			15.15			ns
Clock Pulse Width High Time	15	4			5			ns
Clock Pulse Width Low Time	16	4			5			ns
Analog Output Delay	17			30			30	ns
Analog Output Rise/Fall Time	18		3			3		ns
Analog Output Settling Time (Note 1)	19		13			13		ns
Clock and Data Feedthrough (Note 1)			–30			–30		dB
Glitch Impulse (Note 1)			150			150		pV - sec
DAC-to-DAC Crosstalk			–23			–23		dB
Analog Output Skew			0	2		0	2	ns
Pipeline Delay		4	4	4	4	4	4	Clocks
VAA Supply Current (Note 2)	IAA		180	250		180	250	mA

See test conditions at the end of this section.

AC Characteristics *(continued)*

Parameter	Symbol	50 MHz Devices			35 MHz Devices			Units
		Min	Typ	Max	Min	Typ	Max	
Clock Rate	Fmax			50			35	MHz
RS0–RS2 Setup Time	1	10			10			ns
RS0–RS2 Hold Time	2	10			10			ns
RD* Asserted to Data Bus Driven	3	3			3			ns
RD* Asserted to Data Valid	4			40			40	ns
RD* Negated to Data Bus 3-Stated	5			20			20	ns
Read Data Hold Time	6	5			5			ns
Write Data Setup Time	7	10			10			ns
Write Data Hold Time	8	10			10			ns
CR0–CR3 Output Delay	9			100			100	ns
RD*, WR* Pulse Width Low	10	50			50			ns
RD*, WR* Pulse Width High	11	6*p14			6*p14			ns
Pixel and Control Setup Time	12	3			3			ns
Pixel and Control Hold Time	13	3			3			ns
Clock Cycle Time (p14)	14	20			28			ns
Clock Pulse Width High Time	15	6			7			ns
Clock Pulse Width Low Time	16	6			9			ns
Analog Output Delay	17			30			30	ns
Analog Output Rise/Fall Time	18		3			3		ns
Analog Output Settling Time (Note 1)	19		13			13		ns
Clock and Data Feedthrough (Note 1)			–30			–30		dB
Glitch Impulse (Note 1)			150			150		pV - sec
DAC-to-DAC Crosstalk			–23			–23		dB
Analog Output Skew			0	2		0	2	ns
Pipeline Delay		4	4	4	4	4	4	Clocks
VAA Supply Current (Note 2)	IAA		180	220		180	220	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with external voltage reference, RSET = 143 Ω, and VREF = 1.235 V. TTL input values are 0–3 V with input rise/fall times ≤ 4 ns, measured between the 10-percent and 90-percent points. Timing reference points at 50 percent for inputs and outputs. Analog output load ≤ 10 pF and D0–D7 output load ≤ 75 pF. See timing notes in Figure 9. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5V.

Note 1: Clock and data feedthrough is a function of the number of edge rates, and the amount of overshoot and undershoot on the digital inputs. For this test, the digital inputs have a 1 kΩ resistor to ground and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, and –3 dB test bandwidth = 2x clock rate.

Note 2: At Fmax. IAA (typ) at VAA = 5.0 V. IAA (max) at VAA (max).

Timing Waveforms

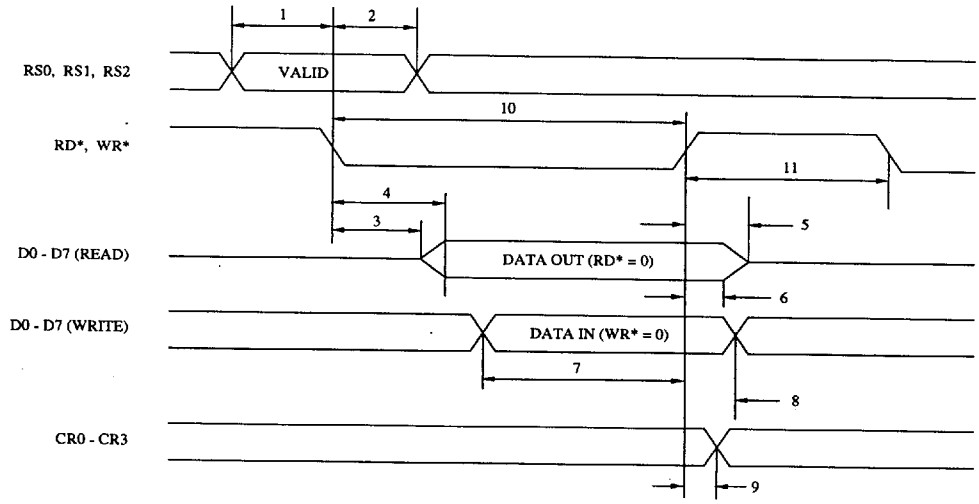
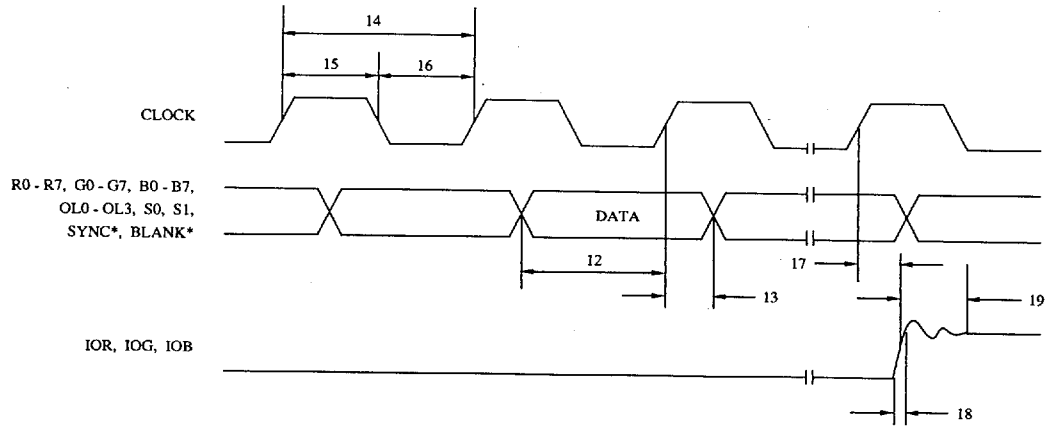


Figure 8. MPU Read/Write Timing Dimensions.



Note 1: Output delay is measured from the 50-percent point of the rising edge of CLOCK to the 50-percent point of full-scale transition.

Note 2: Settling time is measured from the 50-percent point of full-scale transition to the output remaining within ±1 LSB.

Note 3: Output rise/fall time is measured between the 10-percent and 90-percent points of full-scale transition.

Figure 9. Video Input/Output Timing.

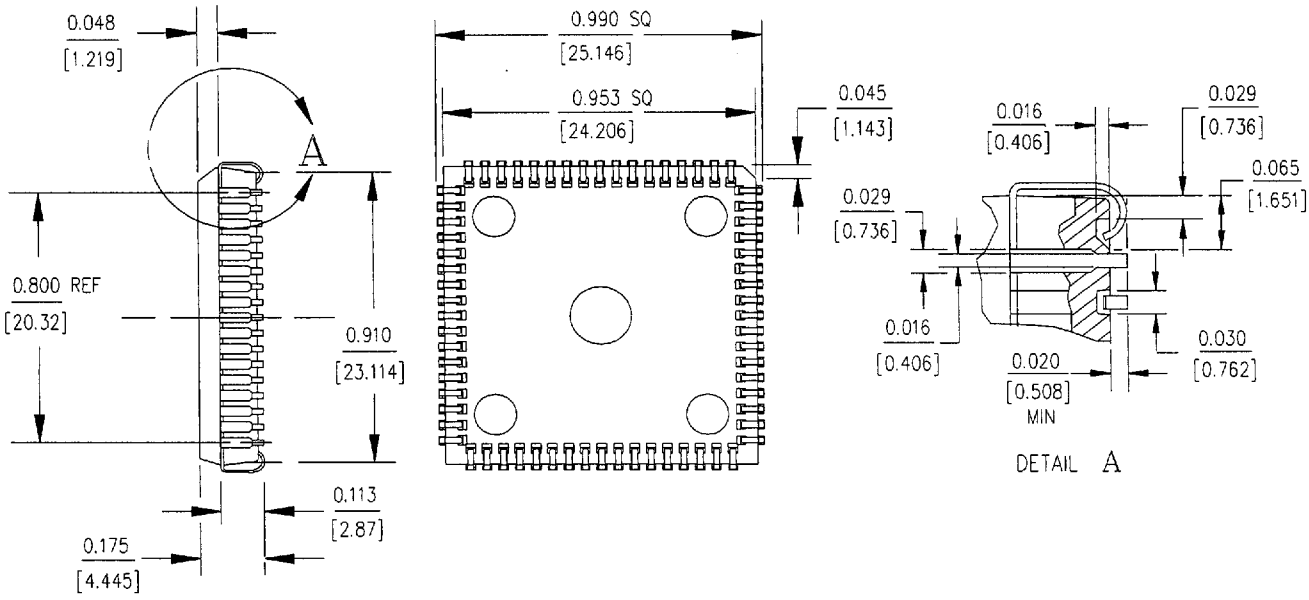
Ordering Information

Model Number	Speed	Package	Ambient Temperature Range
Bt473KPJ110	110 MHz	68-pin Plastic J-Lead	0° to +70° C
Bt473KPJ80	80 MHz	68-pin Plastic J-Lead	0° to +70° C
Bt473KPJ66	66 MHz	68-pin Plastic J-Lead	0° to +70° C
Bt473KPJ50	50 MHz	68-pin Plastic J-Lead	0° to +70° C
Bt473KPJ35	35 MHz	68-pin Plastic J-Lead	0° to +70° C

Revision History

Datasheet Revision	Change from Previous Revision
F	AC parameters: RD* asserted to data bus driven time changed from 5 ns to 3 ns; maximum VAA supply current changed from 220 mA to 250 mA for 80 and 66 MHz devices.
G	Expanded PC Board Layout section.
H	Modified PC Board Layout recommendations. Modified Sync.
I	Added 110 MHz Speed Grade, modified RD*, WR* Pulse Width High and added 471* pin description.

Package Drawing—68–pin Plastic J-Lead (PLCC)



Notes: Unless otherwise specified:

1. Dimensions are in inches [millimeters].
2. Tolerances are: .xxx ± 0.005 [0.127].
3. PLCC packages are intended for surface mounting on solder lands on 0.050 [1.27] centers.