1k, 2k, 4k, bit EEPROMs for direct connection to serial ports

BR9010-W / BR9010F-W / BR9010FV-W / BR9010RFV-W / BR9010RFVM-W
BR9020-W / BR9020F-W / BR9020FV-W / BR9020RFV-W / BR9020RFVM-W
BR9040-W / BR9040F-W / BR9040FV-W / BR9040RFV-W / BR9040RFVM-W

The BR90XX series are serial EEPROMs that can be connected directly to a serial port and can be erased and written electrically. Writing and reading is perfomed in word units, using four types of operation commands. Communication occurs through $\overline{CS}$, $\overline{SK}$, DI, and DO pins, $\overline{WC}$ pin control is used to initiate a write disabled state, enabling these EEPROMs to be used as one-time ROMs. During writing operation is checked via the internal status check.

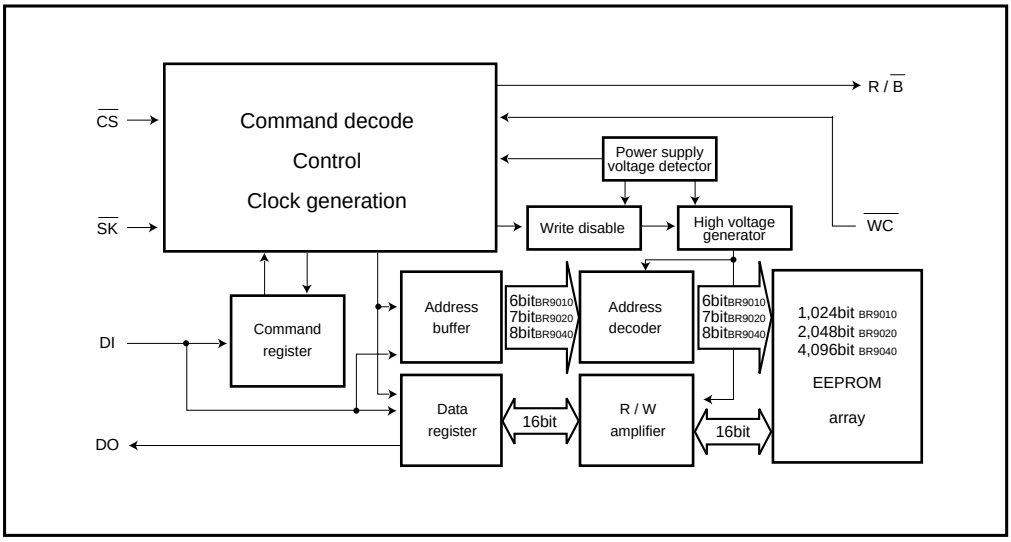
●Application

General-Purpose

●Features

1) BR9010-W / F-W / FV-W / RFV-W / RFVM-W (1k bit) : 64 words×16bit
   BR9020-W / F-W / FV-W / RFV-W / RFVM-W (2k bit) : 128words×16bit
   BR9040-W / F-W / FV-W / RFV-W / RFVM-W (4k bit) : 256words×16bit
2) Single power supply.
3) Serial data I/O.
4) Self-timed programming cycle with auto-erase.
5) Low supply current.
   Active (5V) : 2mA (max.)
   Standby (5V) : 3μA (max.) (CMOS INPUT)
6) Noise filter on the $\overline{SK}$ pin. Write protection when the supply is low.
7) Write protection by $\overline{WC}$ pin.
8) Space Saving DIP8/SOP8/SSOP-B8/MSOP8pin Packages.
9) 100,000 erase/ write cycles endurance.
10) Provide 10 years of date retention.
11) Easy connection to serial port.
12) “FFFFh” stored in all address on shipped.

●**Block diagram**



●**Terminal Function**

Pin No.		Pin name	Function
BR90xx-W/RFV-W/RFVM-W	BR90xxF-W/FV-W		
1	3	$\overline{CS}$	Chip Select Input
2	4	$\overline{SK}$	Serial Date Clock Input
3	5	DI	Serial Date Input (Op code, address)
4	6	DO	Serial Date Output
5	7	GND	Ground (0V)
6	8	$\overline{WC}$	Write Control Input
7	1	R / $\overline{B}$	READY/ $\overline{BUSY}$ Status Output
8	2	V_{CC}	Power Supply

● **Absolute Maximum Ratings** (Ta=25°C)

Parameter		Symbol	Limits		Unit
Supply Voltage		V_{CC}	–0.3~+7.0		V
Power dissipation	BR9010-W, BR9020-W, BR9040-W	Pd	DIP8	800*1	mW
	BR9010F-W, BR9020F-W, BR9040F-W		SOP8	450*2	
	BR9010FV-W, BR9010RFV-W, BR9020FV-W, BR9020RFV-W, BR9040FV-W, BR9040RFV-W		SSOP-B8	300*3	
	BR9010RFVM-W, BR9020RFVM-W, BR9040RFVM-W		MSOP8	310*4	
Storage Temperature		Tstg	–65~+125		°C
Operating Temperature		Topr	–40~+85		°C
Terminal Voltage		–	–0.3~V_{CC}+0.3		V

∗1 Degradation is done at 8.0mW/˚C for operation above Ta=25˚C
∗2 Degradation is done at 4.5mW/˚C for operation above Ta=25˚C
∗3 Degradation is done at 3.0mW/˚C for operation above Ta=25˚C
∗4 Degradation is done at 3.1mW/˚C for operation above Ta=25˚C

● **Recommended Operating Condition** (Ta=25°C)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Write	V_{CC}	2.7	–	5.5	V
	Read		2.0	–	5.5	V
Input voltage		V_{IN}	0	–	V_{CC}	V

●**Electrical Characteristics**

Unless otherwise specified (Ta=–40~+85°C, V_{CC}=2.7V~5.5V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input LOW Voltage 1	V_{IL1}	–	–	0.3×V_{CC}	V	DI pin
Input HIGH Voltage 1	V_{IH1}	0.7×V_{CC}	–	–	V	DI pin
Input LOW Voltage 2	V_{IL2}	–	–	0.2×V_{CC}	V	$\overline{CS}$, $\overline{SK}$, $\overline{WC}$ pin
Input HIGH Voltage 2	V_{IH2}	0.8×V_{CC}	–	–	V	$\overline{CS}$, $\overline{SK}$, $\overline{WC}$ pin
Output LOW Voltage	V_{OL}	0	–	0.4	V	I_{OL}=2.1mA
Output HIGH Voltage	V_{OH}	V_{CC}–0.4	–	V_{CC}	V	I_{OH}=–0.4mA
Input Leakage Current	I_{LI}	–1	–	1	µA	V_{IN}=0V~V_{CC}
Output Leakage Current	I_{LO}	–1	–	1	µA	V_{OUT}=0V~V_{CC}, $\overline{CS}$=V_{CC}
Operating Current	I_{CC1}	–	–	2	mA	f_{SK}=2MHz, tE / W=10ms (WRITE)
	I_{CC2}	–	–	1	mA	f_{SK}=2MHz (READ)
Standby Current	I_{SB}	–	–	3	µA	$\overline{CS}$, $\overline{SK}$, DI, $\overline{WC}$=V_{CC}, DO, R / $\overline{B}$=OPEN
Clock Frequency	f_{SK}	–	–	2	MHz	–

Unless otherwise specified (Ta=–40~+85°C, V_{CC}=2.7V~3.3V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input LOW Voltage 1	V_{IL1}	–	–	0.3×V_{CC}	V	DI pin
Input HIGH Voltage 1	V_{IH1}	0.7×V_{CC}	–	–	V	DI pin
Input LOW Voltage 2	V_{IL2}	–	–	0.2×V_{CC}	V	$\overline{CS}$, $\overline{SK}$, $\overline{WC}$ pin
Input HIGH Voltage 2	V_{IH2}	0.8×V_{CC}	–	–	V	$\overline{CS}$, $\overline{SK}$, $\overline{WC}$ pin
Output LOW Voltage	V_{OL}	0	–	0.4	V	I_{OL}=100µA
Output HIGH Voltage	V_{OH}	V_{CC}–0.4	–	V_{CC}	V	I_{OH}=–100µA
Input Leakage Current	I_{LI}	–1	–	1	µA	V_{IN}=0V~V_{CC}
Output Leakage Current	I_{LO}	–1	–	1	µA	V_{OUT}=0V~V_{CC}, $\overline{CS}$=V_{CC}
Operating Current	I_{CC1}	–	–	1.5	mA	f_{SK}=2MHz, tE / W=10ms (WRITE)
	I_{CC2}	–	–	0.5	mA	f_{SK}=2MHz (READ)
Standby Current	I_{SB}	–	–	2	µA	$\overline{CS}$, $\overline{SK}$, DI, $\overline{WC}$=V_{CC}, DO, R / $\overline{B}$=OPEN
Clock Frequency	f_{SK}	–	–	2	MHz	–

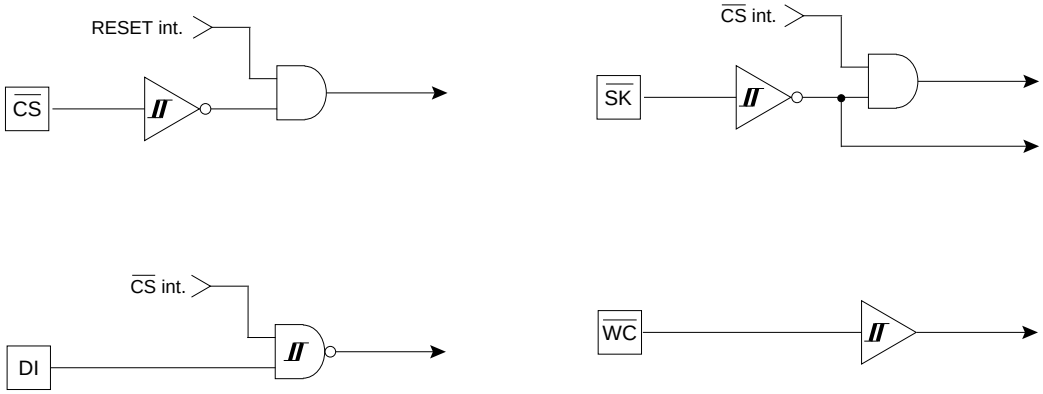
● **AC Operation Characteristics**

(Ta=−40~+85°C, Vcc=2.7~5.5V)

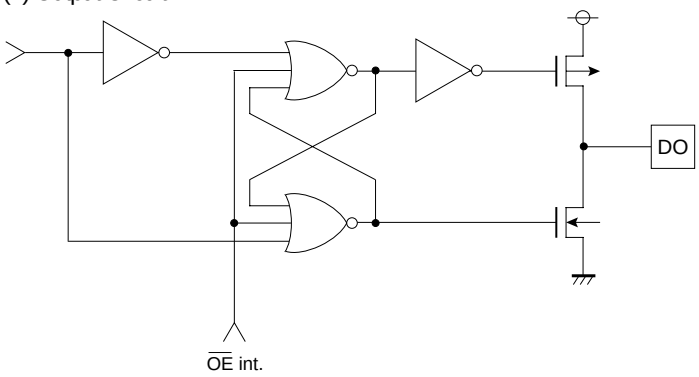
Parameter	Symbol	Min.	Typ.	Max.	Unit
Chip Select Setup Time	t_{CSS}	100	–	–	ns
Chip Select Hold Time	t_{CSH}	100	–	–	ns
Data In Setup Time	t_{DIS}	100	–	–	ns
Data In Hold Time	t_{DIH}	100	–	–	ns
Delay to Output High	t_{PD1}	–	–	150	ns
Delay to Output Low	t_{PD0}	–	–	150	ns
Self-Timed Program Cycle	$t_{E/W}$	–	–	10	ms
Minimum Chip Select High Time	t_{CS}	250	–	–	ns
Data Output Disable Time(From $\overline{CS}$)	t_{OH}	0	–	150	ns
Clock High Time	t_{WH}	230	–	–	ns
Clock Low Time	t_{WL}	230	–	–	ns
Write Control Setup Time	t_{WCS}	0	–	–	ns
Write Control Hold Time	t_{WCH}	0	–	–	ns
Clock High to Output READY/$\overline{BUSY}$ Status	t_{SV}	–	–	150	ns

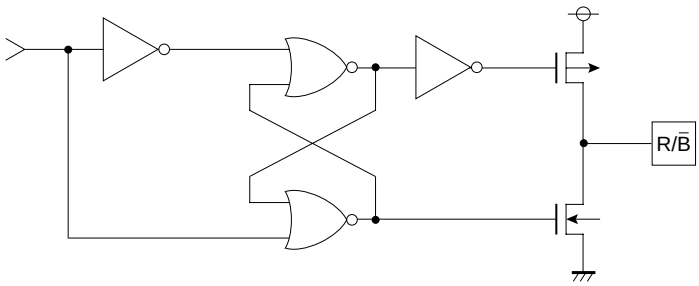
● **I / O Circuit**

(1) Input Circuit



(2) Output Circuit





●Operating

(1) Instruction Code

Instruction	Start Bit	Op Code	Address	Data
READ	1010	1000	A0 A1 A2 A3 A4 A5 (A6)*2 (A7)*1	D0 D1–D14 D15 (READ DATA)
WRITE	1010	0100	A0 A1 A2 A3 A4 A5 (A6)*2 (A7)*1	D0 D1–D14 D15 (WRITE DATA)
Write Enable (WEN)	1010	0011	* * * * * * * *	
Write Disable (WDS)	1010	0000	* * * * * * * *	

Address and data must be transferred from LSB.
* Means either V_{IH} or V_{IL}
BR9020-W/F-W/FV-W/RFV-W/RFVM-W *1= "0"
BR9010-W/F-W/FV-W/RFV-W/RFVM-W *1, 2= "0"

Synchronous Data Input Output Timing

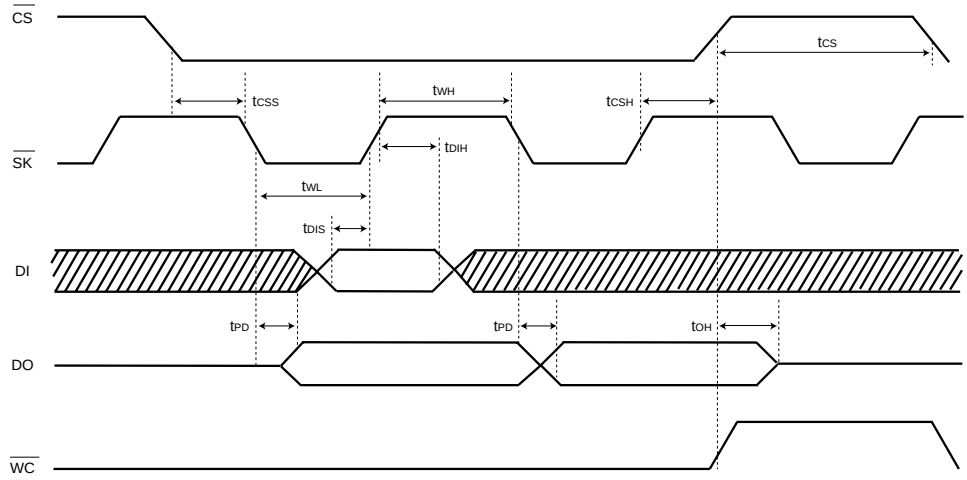


Fig.1

- Input Data is clocked into the DI pin on the rising edge of the clock SK
- Output data is clocked out on the falling edge of the SK clock.
- The WC pin does not have any affect on the READ, WEN and WDS operations.
- Between instructions, CS must be brought High for greater than the minimum of tCS. If CS is maintained Low, the next instruction isn't detected.

(2) WRITE Enable / Disable

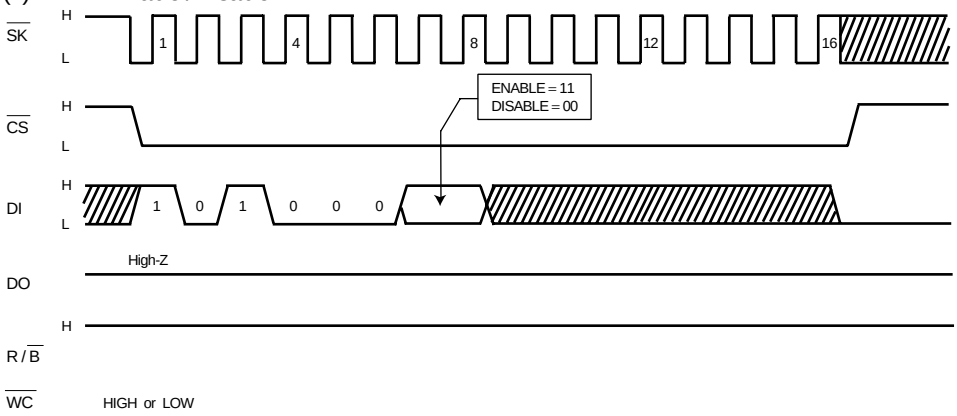


Fig.2

1) When power is first applied, the device has been held in a reset status, with respect to the write enable, in the same way the write disable (WDS) instruction is executed. Before the write instruction is executed, the device must be received the write enable (WEN) instruction. Once the device is done, the device remains programmable until the write disable (WDS) instruction is executed or the supply is removed from the device.
2) It is unnecessary to add the clock after 16 th clock. If the device is recieved the clock, the device ignores the clock.
3) As both of the enable and disable instructions don't depend on the status of the $\overline{WC}$ pin, the state of $\overline{WC}$ isn't cared during the instruction.
4) The instruction is recognized after the rising edge of 8 th clock for the address following 8 clocks for the opcode, but the specified address isn't cared during the instructions.

(3) Read Cycle

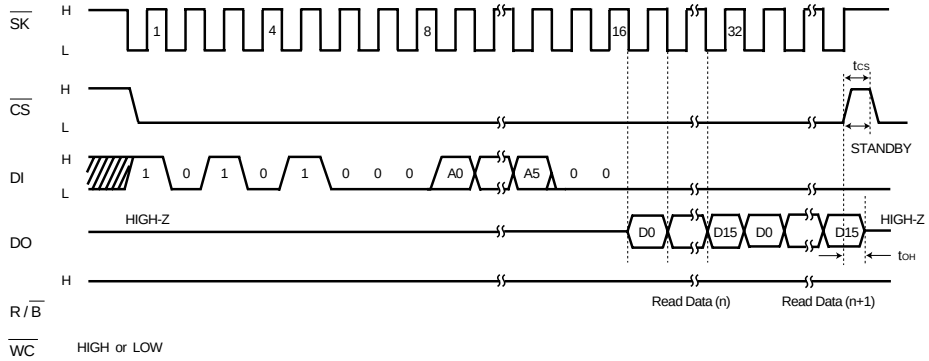


Fig.3 BR9010-W / F--W / FV-W / RFV-W / RFVM-W

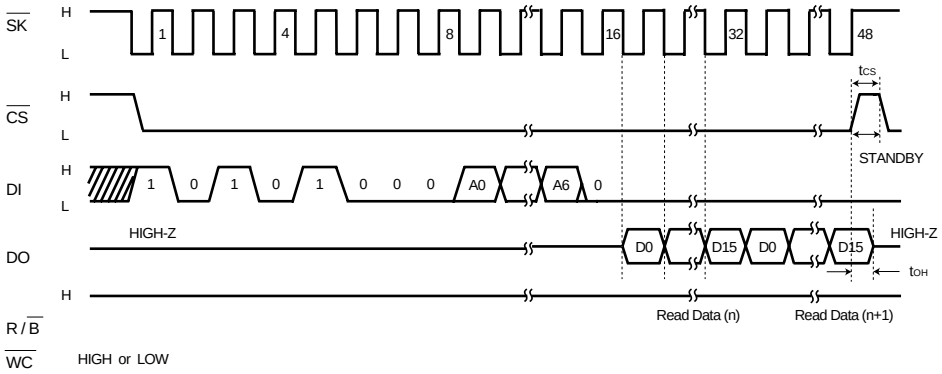


Fig.4 BR9020-W / F-W / FV-W / RFV-W / RFVM-W

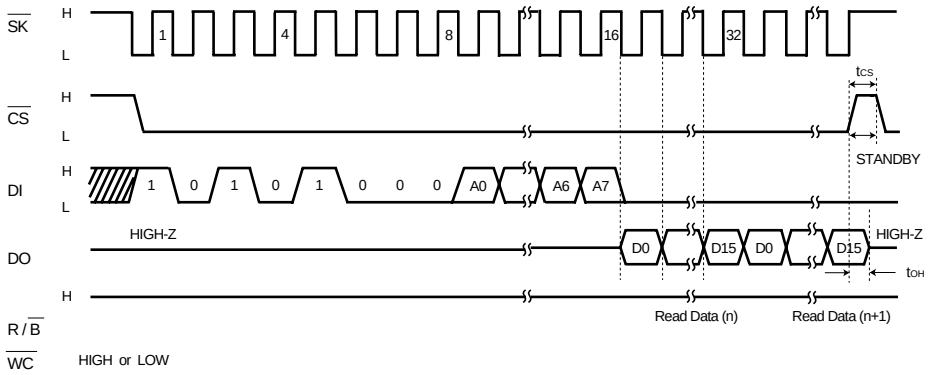


Fig.5 BR9040-W / F-W / FV-W / RFV-W / RFVM-W

1) On the falling edge of 16 th clock, the data stored in the specified address (n) is clocked out of the DO pin.
The Output DO is toggled after the internal propagation t_{PDO} or t_{PD1} on the falling edge of $\overline{SK}$. During t_{PD0} or t_{PD1}, the data is the previous data or unstable, and to take in the data, t_{PD} is needed. (Refer to Fig.1 Synchronous data input output timing.)
2) The data stored in the next address is clocked out of the device on the falling edge of 32nd clock. The data stored in the upper address every 16 clocks is output sequentially by the continual $\overline{SK}$ input. Also the read operation is reset by $\overline{CS}$ High.

(4) Write Cycle

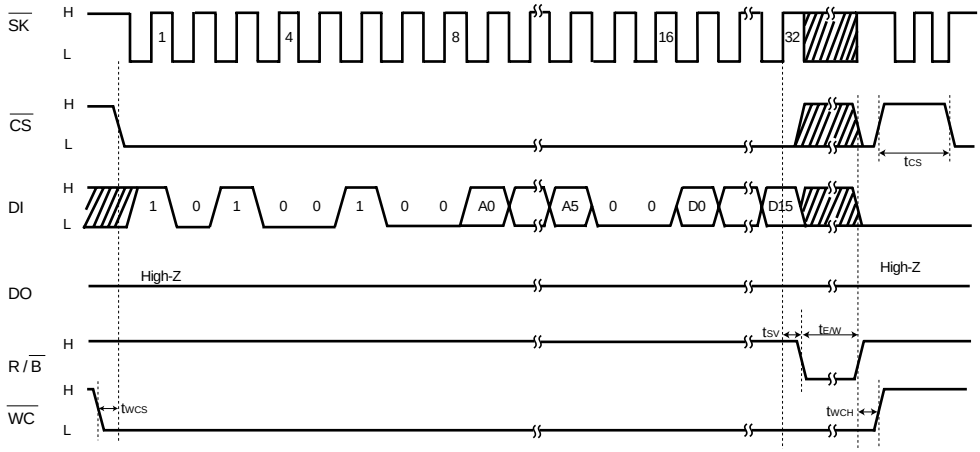


Fig.6 BR9010-W / F-W / FV-W / RFV-W / RFVM-W

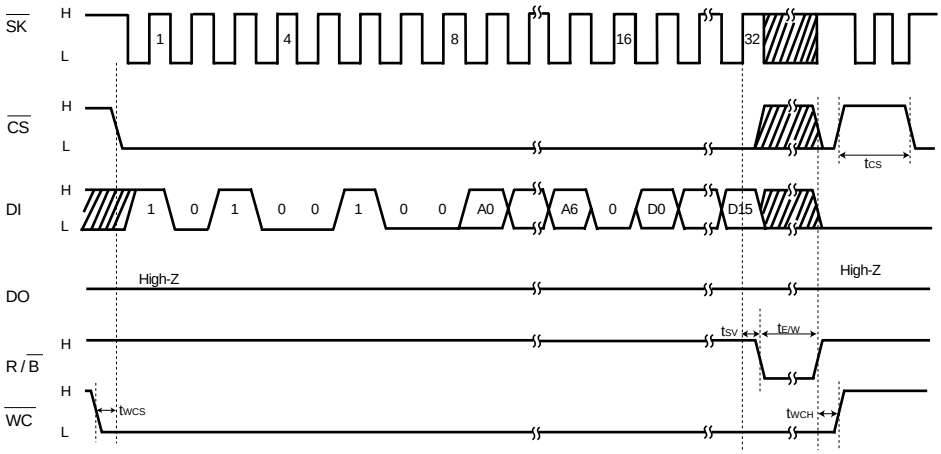


Fig.7 BR9020-W / F-W / FV-W / RFV-W / RFVM-W

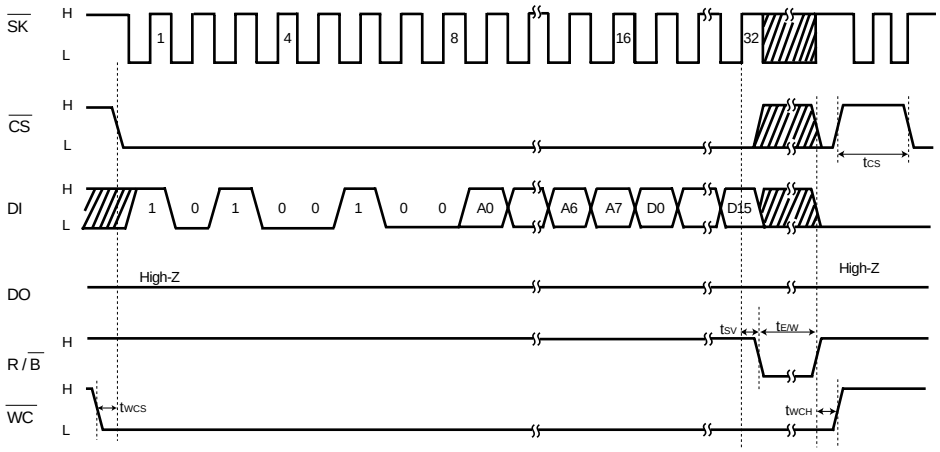


Fig.8 BR9040-W / F-W / FV-W / RFV-W / RFVM-W

1) During the write instruction , $\overline{CS}$ must be brought Low. However once the write operation started, $\overline{CS}$ may be either High or Low. But in the case of connecting the $\overline{WC}$ pin to the $\overline{CS}$ pin. $\overline{CS}$ and $\overline{WC}$ must be brought Low during programming cycle.(If the $\overline{WC}$ pin is brought High during the write cycle, the write operation is halted. In that case, the data of the specified address is not guaranteed. It is necessary to rewrite it.)
2) After the R / $\overline{B}$ pin changed Busy to Ready, once $\overline{CS}$ is brought High, then $\overline{CS}$ keep Low ,which means the status of being able to accept an instruction. The device can take in the input from $\overline{SK}$ and DI, but in the case of keeping $\overline{CS}$ Low without being brought High once, the input is canceled until being $\overline{CS}$ High once.
3) At the rising edge of 32 nd clock, the R / $\overline{B}$ pin will be driven Low after the specified time delay (tSV).
4) During programming, R / $\overline{B}$ is tied to Low by the device (On the rising edge of $\overline{SK}$ taken in the last data (D15), internal timer starts and automatically finished after the data of memory cell is written spending tE / W. $\overline{SK}$ could be either High or Low at the time.
5) After input write instruction, also the DO pin will be able to show the status of R / $\overline{B}$, in the case that $\overline{CS}$ is falling from High to Low while $\overline{SK}$ is tied to Low. (Refer to READY / $\overline{BUSY}$ STATUS in the next page.)

(5) READY / $\overline{BUSY}$ STATUS (on the R / $\overline{B}$ pin, the DO pin)

1)The DO pin outputs the READY / $\overline{BUSY}$ status of the internal part, which shows whether the device is ready to receive the next instruction or not. (High or Low)
After the write instruction is completed, if $\overline{CS}$ is brought from high to low while $\overline{SK}$ is Low, the DO pin outputs the internal status. (The R / $\overline{B}$ pin may be no connection.
2) When written to the memory cell, R / $\overline{B}$ status is output after tSV spent from the rising edge of 32 th clock on $\overline{SK}$.

R / $\overline{B}$ =Low : under writing
After spending tE / W operating the internal timer, the device automatically finishes writing.
During tE / W, the memory array is accessed and any instruction is not received.

R / $\overline{B}$=High : ready
Auto programming has been completed. The device is ready to receive the next Instruction.

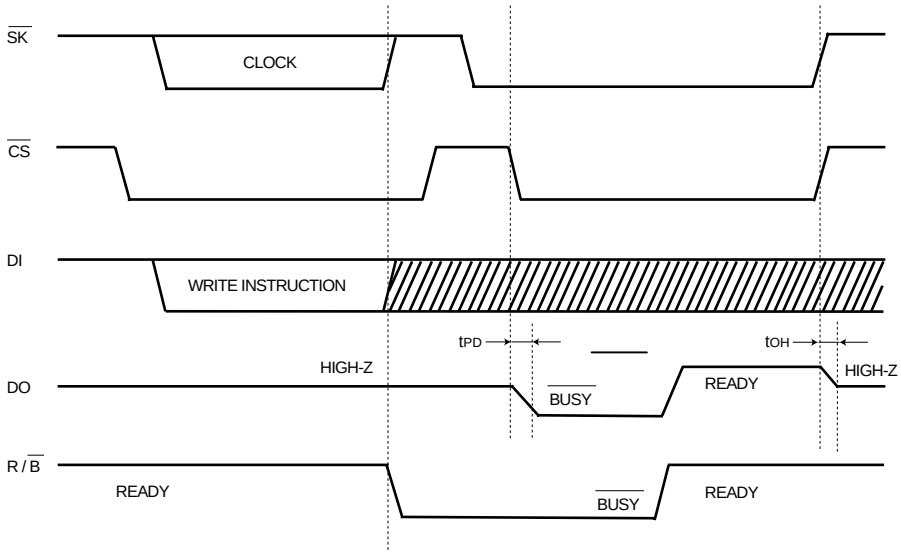


Fig.9 R / $\overline{B}$ Status Output Timing

(6) About the direct connection between the DI and DO pins

The device can be used with the DI pin connected to the DO pin directly.

But when the READY / BUSY status is output, be careful about the bus conflict on the port of the controller.

●Attention to Use

(1) Power ON / OFF

1) The $\overline{CS}$ is brought High during power–up and power–down.
2) This device is in active state while $\overline{CS}$ is Low.
3) The extraordinary function or data collapse may occur in that condition because of noise etc, if power–up and power–down is done with $\overline{CS}$ brought Low.
   In order to prevent above errors from happening, keep $\overline{CS}$ High during power-up and power-down.

(Good example) $\overline{CS}$ is brought High during power–up and power-down.
Please take more than 10ms between power–up and power-off, or the internal circuit is not always reset.

(Bad example) $\overline{CS}$ is brought Low during power–up and power-down.
The $\overline{CS}$ pin is always Low in this case, the noise may force the device to make malfunction or inadvertent write.
It sometimes occurs in the case that the $\overline{CS}$ pin is Hi-Z.

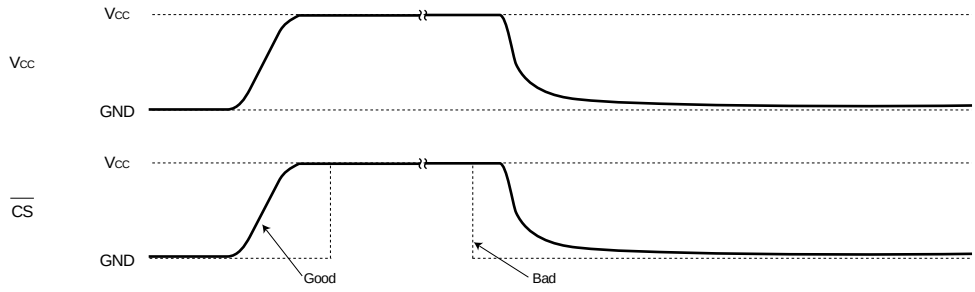


Fig.10

(2) Noise Rejection

1) $\overline{SK}$ NOISE
   If $\overline{SK}$ line has a lot of noise for rising time of $\overline{SK}$, the device may recognize the noise as a clock and then clock will be shifted.
2) $\overline{WC}$ NOISE
   If $\overline{WC}$ line has noise during write cycle (tE / W), there may be a chance to deny the programming.
3) VCC NOISE
   It recommended that capacitor is put between VCC and GND to prevent these case, since it is possible to occur malfunction by the effect of noise or surge on power line.

(3) Instruction Mode Cancel

1) Read instruction

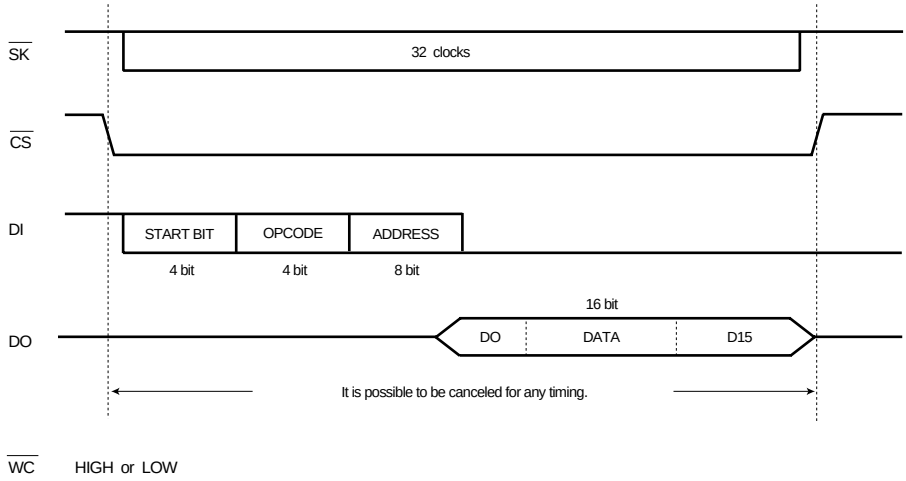


Fig.11

How to cancel : $\overline{CS}$ is brought High.

2) Write instruction

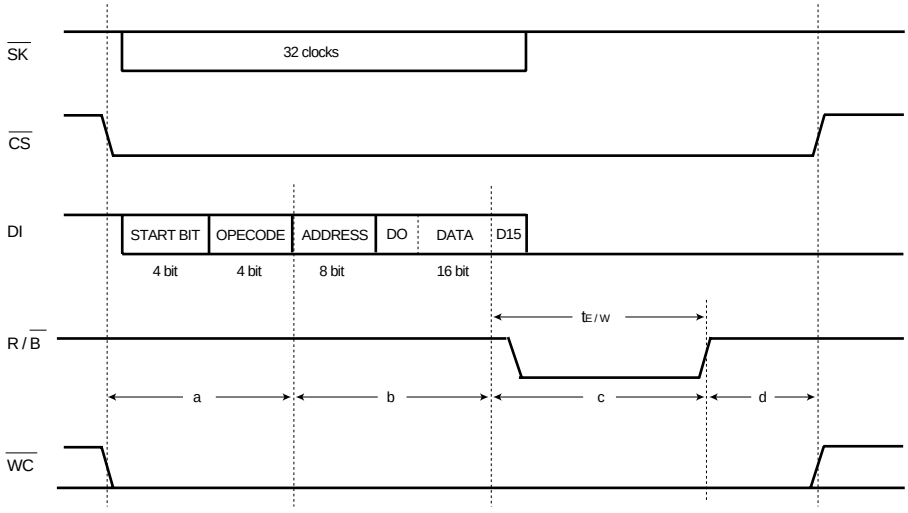


Fig.12

How to cancel

a : $\overline{CS}$ is brought High to cancel the instruction, and $\overline{WC}$ may be either High or Low.

b : In case that $\overline{WC}$ is brought High for a moment, or $\overline{CS}$ is brought High, the write instruction is canceled, the data of the specified address is not changed.

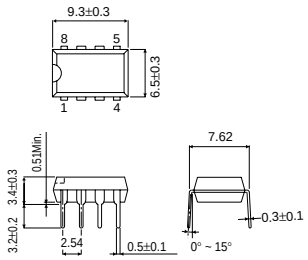
c : When $\overline{WC}$ is brought High, or the device is powered down (But the latter way is not recommended), the instruction is canceled but the specified data is not guaranteed. Send the instruction again.

d : When $\overline{CS}$ is brought High during R/$\overline{B}$ High, the device is reset and ready to receive a next instruction.

NOTE : The document may be strategic technical data subject to COCOM regulations.

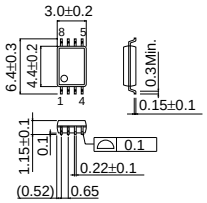
●**External dimensions** (Units : mm)

BR9010-W, BR9020-W, BR9040-W



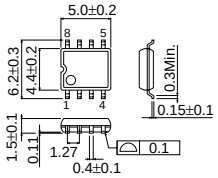
DIP8

BR9010FV-W, BR9010RFV-W
BR9020FV-W, BR9020RFV-W
BR9040FV-W, BR9040RFV-W



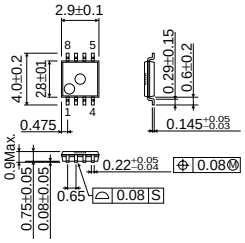
SSOP-B8

BR9010F-W, BR9020F-W, BR9040F-W



SOP8

BR9010RFVM-W, BR9020RFVM-W, BR9040RFVM-W



MSOP8