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2 GENERAL DESCRIPTION

The PCF21xxC family are single-chip, silicon gate CMOS LCD driver circuits. A 3-line bus (CBUS) structure enables serial data transfer with microcontrollers. All inputs are CMOS/NMOS compatible.

The devices have the same function and performance as those of the PCF21xx family, which they supersede. The maximum operating voltage required is reduced from 6.5 to 6.0 V.

3 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		2.25	–	6.0	V
I_{DD1}	supply current 1	outputs open; CBUS inactive	–	20	50	μA
I_{DD2}	supply current 2	outputs open; CBUS inactive; T_{amb} = 25 °C	–	20	30	μA
P_O	power dissipation per output		–	–	100	mW
T_{amb}	operating ambient temperature		–40	–	+85	°C
T_{stg}	storage temperature		–65	–	+150	°C

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF2100CP	DIP28	plastic dual in-line package; 28 leads (600 mil)	SOT117-1
PCF2100CT	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
PCF2111CP	DIP40	plastic dual in-line package; 40 leads (600 mil)	SOT129-1
PCF2111CT	VSO40	plastic very small outline package; 40 leads	SOT158-1
PCF2112CP	DIP40	plastic dual in-line package; 40 leads (600 mil)	SOT129-1
PCF2112CT	VSO40	plastic very small outline package; 40 leads	SOT158-1

5 BLOCK DIAGRAMS

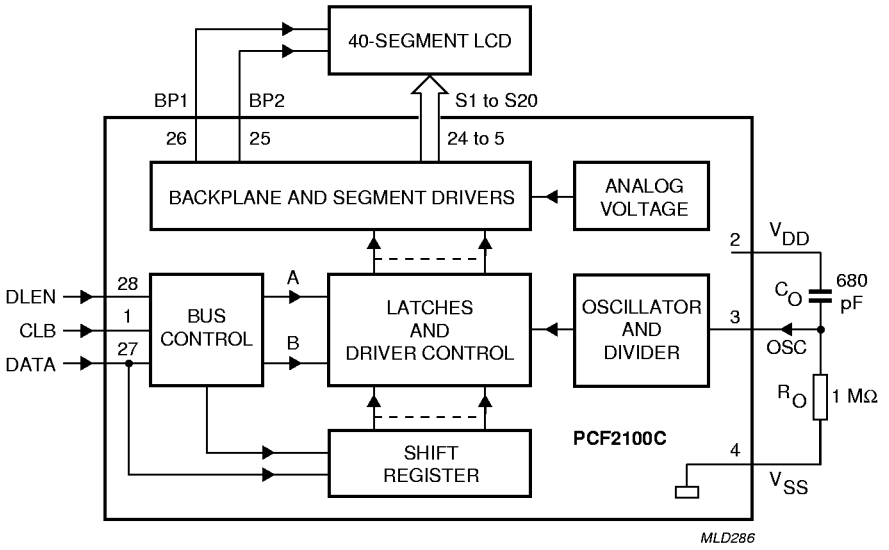


Fig.1 Block diagram; PCF2100C.

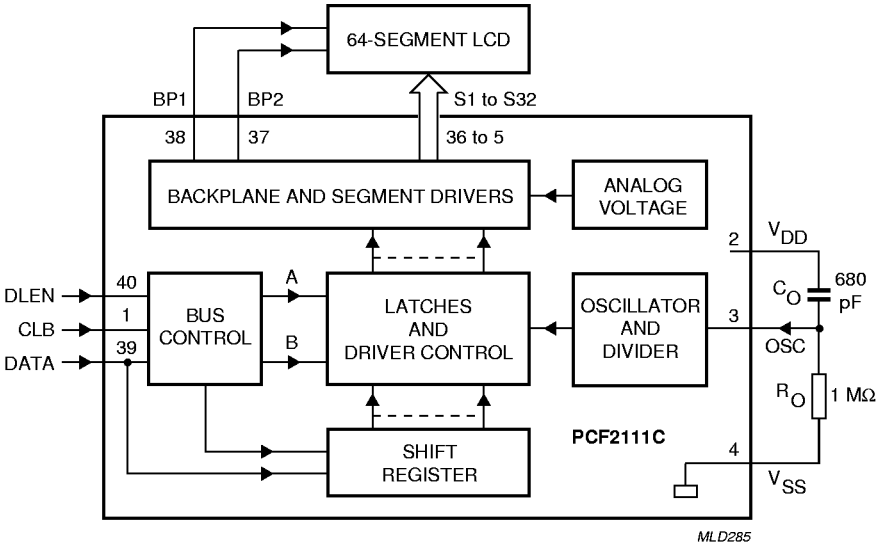


Fig.2 Block diagram; PCF2111C.

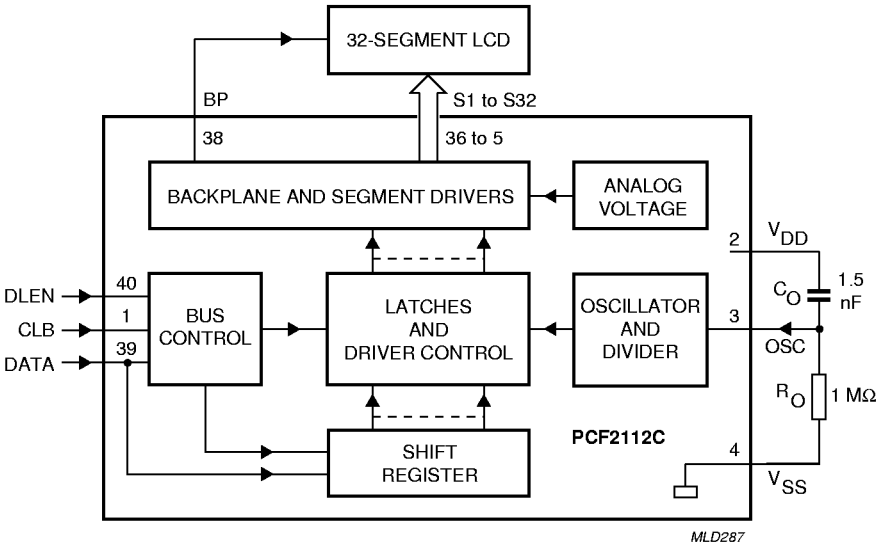


Fig.3 Block diagram; PCF2112C.

6 PINNING

6.1 PCF2100C

SYMBOL	PIN	DESCRIPTION
CLB	1	clock burst input (CBUS)
V_{DD}	2	supply voltage
OSC	3	oscillator input
V_{SS}	4	supply voltage ground
S20	5	LCD driver output 20
S19	6	LCD driver output 19
S18	7	LCD driver output 18
S17	8	LCD driver output 17
S16	9	LCD driver output 16
S15	10	LCD driver output 15
S14	11	LCD driver output 14
S13	12	LCD driver output 13
S12	13	LCD driver output 12
S11	14	LCD driver output 11
S10	15	LCD driver output 10
S9	16	LCD driver output 9
S8	17	LCD driver output 8
S7	18	LCD driver output 7
S6	19	LCD driver output 6
S5	20	LCD driver output 5
S4	21	LCD driver output 4
S3	22	LCD driver output 3
S2	23	LCD driver output 2
S1	24	LCD driver output 1
BP2	25	backplane driver output 2
BP1	26	backplane driver output 1
DATA	27	data input line (CBUS)
DLEN	28	data input line enable (CBUS)

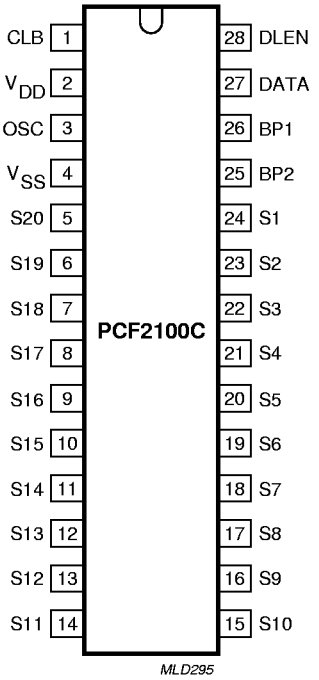


Fig.4 Pin configuration; SOT117-1 and SOT136-1.

6.2 PCF2111C

SYMBOL	PIN	DESCRIPTION
CLB	1	clock burst input (CBUS)
V_{DD}	2	supply voltage
OSC	3	oscillator input
V_{SS}	4	supply voltage ground
S32	5	LCD driver output 32
S31	6	LCD driver output 31
S30	7	LCD driver output 30
S29	8	LCD driver output 29
S28	9	LCD driver output 28
S27	10	LCD driver output 27
S26	11	LCD driver output 26
S25	12	LCD driver output 25
S24	13	LCD driver output 24
S23	14	LCD driver output 23
S22	15	LCD driver output 22
S21	16	LCD driver output 21
S20	17	LCD driver output 20
S19	18	LCD driver output 19
S18	19	LCD driver output 18
S17	20	LCD driver output 17
S16	21	LCD driver output 16
S15	22	LCD driver output 15
S14	23	LCD driver output 14
S13	24	LCD driver output 13
S12	25	LCD driver output 12
S11	26	LCD driver output 11
S10	27	LCD driver output 10
S9	28	LCD driver output 9
S8	29	LCD driver output 8
S7	30	LCD driver output 7
S6	31	LCD driver output 6
S5	32	LCD driver output 5
S4	33	LCD driver output 4
S3	34	LCD driver output 3
S2	35	LCD driver output 2
S1	36	LCD driver output 1
BP2	37	backplane driver output 2
BP1	38	backplane driver output 1
DATA	39	data input line (CBUS)
DLEN	40	data input line enable (CBUS)

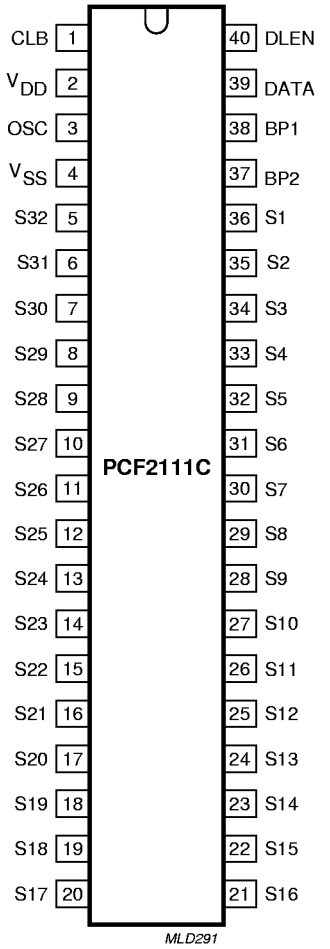


Fig.5 Pin configuration; SOT129-1 and SOT158-1.

6.3 PCF2112C

SYMBOL	PIN	DESCRIPTION
CLB	1	clock burst input (CBUS)
V_{DD}	2	supply voltage
OSC	3	oscillator input
V_{SS}	4	supply voltage ground
S32	5	LCD driver output 32
S31	6	LCD driver output 31
S30	7	LCD driver output 30
S29	8	LCD driver output 29
S28	9	LCD driver output 28
S27	10	LCD driver output 27
S26	11	LCD driver output 26
S25	12	LCD driver output 25
S24	13	LCD driver output 24
S23	14	LCD driver output 23
S22	15	LCD driver output 22
S21	16	LCD driver output 21
S20	17	LCD driver output 20
S19	18	LCD driver output 19
S18	19	LCD driver output 18
S17	20	LCD driver output 17
S16	21	LCD driver output 16
S15	22	LCD driver output 15
S14	23	LCD driver output 14
S13	24	LCD driver output 13
S12	25	LCD driver output 12
S11	26	LCD driver output 11
S10	27	LCD driver output 10
S9	28	LCD driver output 9
S8	29	LCD driver output 8
S7	30	LCD driver output 7
S6	31	LCD driver output 6
S5	32	LCD driver output 5
S4	33	LCD driver output 4
S3	34	LCD driver output 3
S2	35	LCD driver output 2
S1	36	LCD driver output 1
n.c.	37	not connected
BP	38	backplane driver output
DATA	39	data input line (CBUS)
DLEN	40	data input line enable (CBUS)

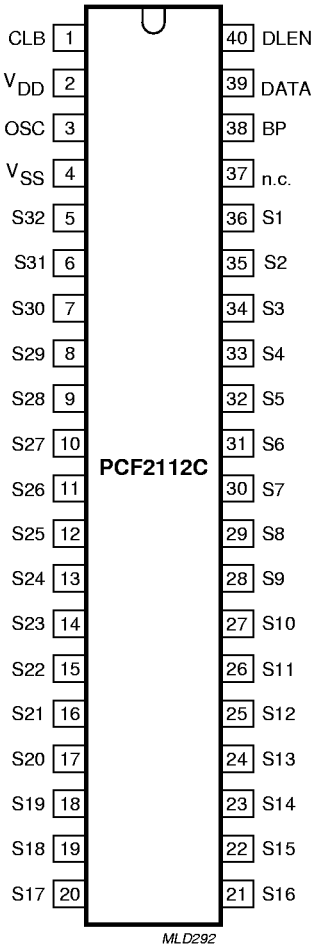


Fig.6 Pin configuration; SOT129-1 and SOT158-1.

7 FUNCTIONAL DESCRIPTION

An LCD segment or LED output is activated when the corresponding DATA bit is HIGH.

7.1 PCF2100C

When DATA bit 21 is HIGH, the A-latches (BP1) are loaded. With DATA bit 21 LOW, the B-latches (BP2) are loaded. CLB pulse 23 transfers data from the shift register to the selected latches.

7.2 PCF2111C

When DATA bit 33 is HIGH, the A-latches (BP1) are loaded. With DATA bit 33 LOW, the B-latches (BP2) are loaded. CLB pulse 35 transfers data from the shift register to the selected latches.

7.3 PCF2112C

When DATA bit 33 is HIGH, the latches are loaded. CLB pulse 35 transfers data from the shift register to the selected latches.

7.4 Bus control logic

The following tests are carried out by the bus control logic:

1. Test on leading zero
2. Test on number of DATA bits
3. Test of disturbed DLEN and DATA signals during transmission.

If one of the test conditions is not fulfilled, no action follows the load condition (load pulse with DLEN LOW) and the driver is ready to receive new data.

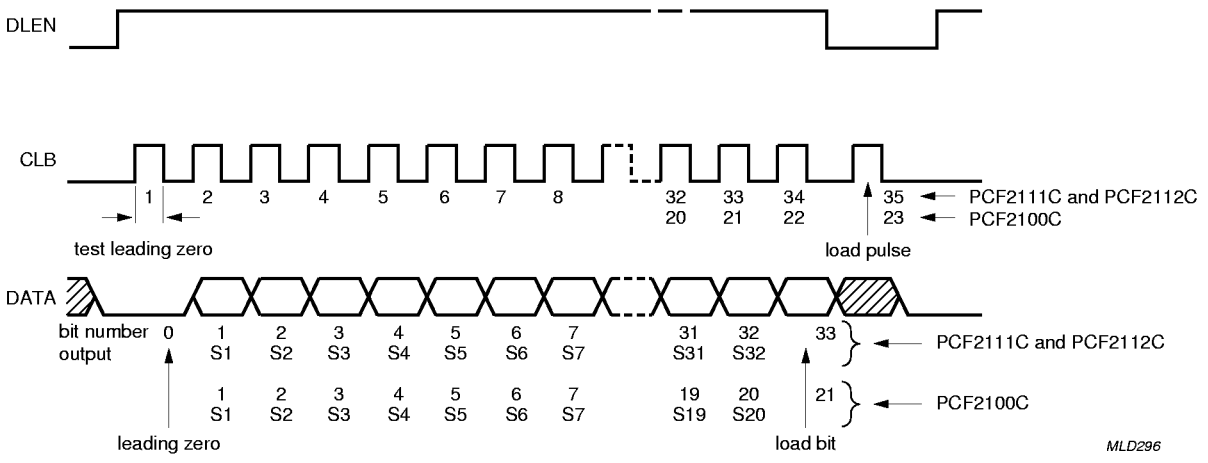


Fig.7 CBUS data format.

7.5 Timing

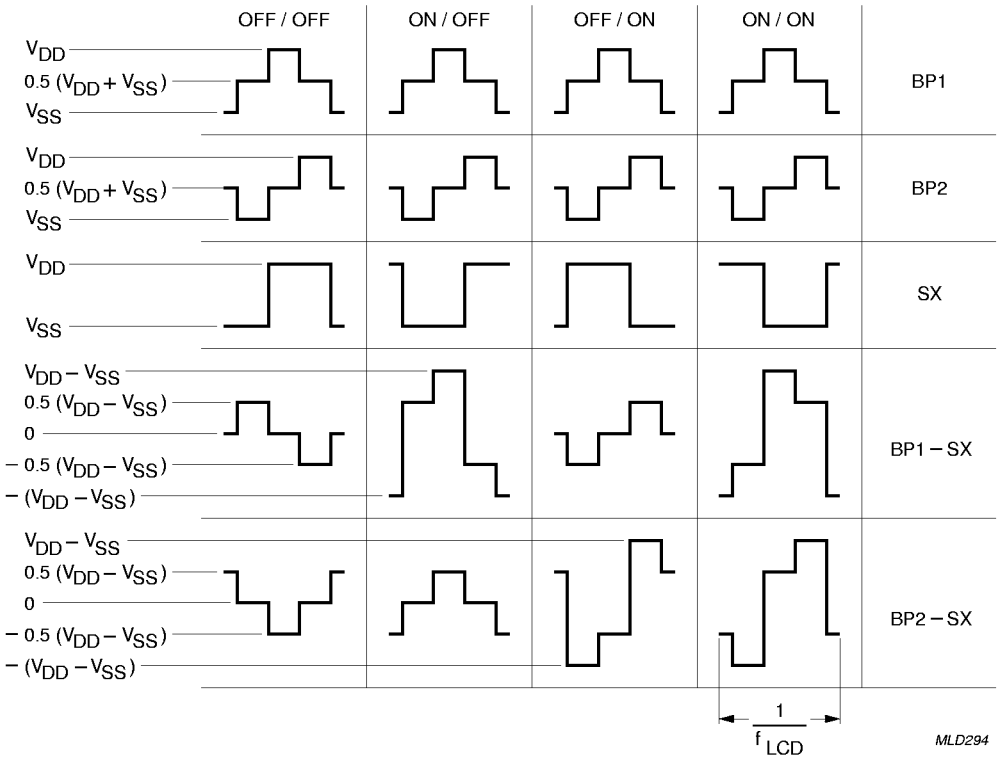


Fig.8 Timing diagram for PCF2100C and PCF2111C.

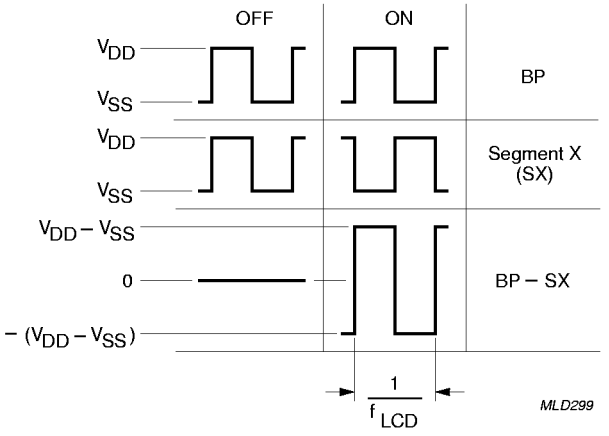
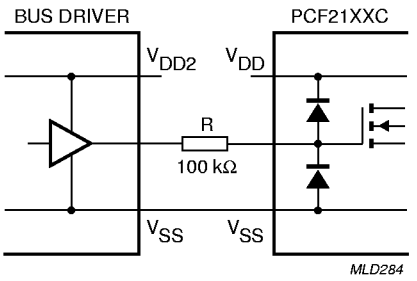


Fig.9 Timing diagram for PCF2112C.

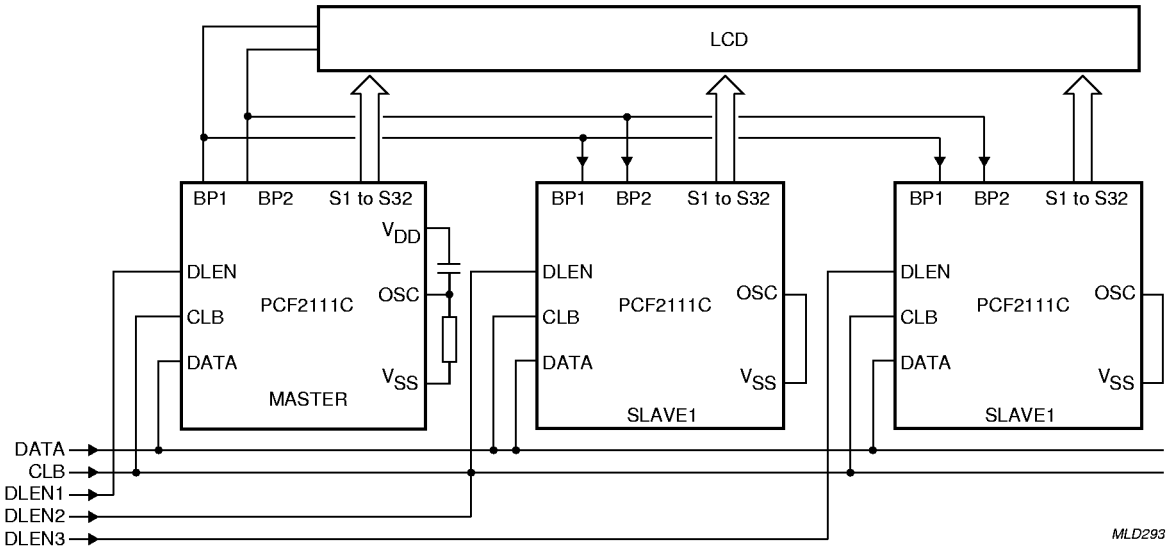
7.6 Input circuitry



V_{SS} line is common. In systems where it is expected that $V_{DD2} > V_{DD1} + 0.5$ V, a resistor should be inserted to reduce the current flowing through the input protection. Maximum input current ≤40 μA.

Fig.10 Input circuitry.

7.7 Expansion



By connecting OSC to V_{SS} the BP pins become inputs and generate signals synchronized to the single oscillator frequency, thus allowing expansion of several members of the PCF21xxC family up to the BP drive capability of the master. The PCF2112C can only function as a master for other PCF2112Cs.

Fig.11 Expansion possibility (using PCF2111C).

8 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		–0.5	+8.0	V
V_I	input voltage DLEN, CLB, DATA and OSC		V_{SS} – 0.5	V_{DD} + 0.5	V
V_O	output voltage BP1, BP2 and S1 to S32		V_{SS} – 0.5	V_{DD} + 0.5	V
I_{DD}, I_{SS}	supply current		–50	+50	mA
I_I	DC input current		–20	+20	mA
I_O	DC output current		–25	+25	mA
P_{tot}	total power dissipation per package	note 1	–	500	mW
P_O	power dissipation per output		–	100	mW
T_{stg}	storage temperature		–65	+150	°C

Note

1. Derate by 7.7 mW/K when T_{amb} > 60 °C.

9 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices. See *"Handling MOS devices"*.

ESD in accordance with *"MIL STD 883C, Method 3015"*.

10 DC CHARACTERISTICS

V_{DD} = 2.25 to 6.0 V; V_{SS} = 0 V; T_{amb} = –40 to +80 °C; R_O = 1 MΩ; C_O = 680 pF; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		2.25	–	6.0	V
I_{DD}	supply current	note 1; see Fig.13	–	20	50	µA
		note 1; T_{amb} = 25 °C; see Fig.13	–	20	30	µA
V_{POR}	power-on reset voltage level	note 2	–	1.0	1.6	V
Inputs CLB, DATA and DLEN						
V_{IL}	LOW level input voltage		–	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	–	V
I_{LI}	input leakage current	$V_I = V_{SS}$ or V_{DD}	–	–	±1	µA
C_i	input capacitance	note 3	–	–	10	pF
Input OSC						
I_{osc}	oscillator start-up current	$V_I = V_{SS}$	0.5	1.2	5.0	µA
LCD outputs						
V_{BP}	DC voltage of backplane drivers		–	±20	–	mV
$Z_{O(BP)}$	backplane driver output impedance	note 4; V_{DD} = 5 V	–	0.5	5.0	kΩ
$Z_{O(S)}$	segment driver output impedance	note 4; V_{DD} = 5 V	–	1	7	kΩ

Notes

1. Outputs open; CBUS inactive.
2. Resets all logic, when $V_{DD} < V_{POR}$.
3. Periodically sampled (not 100% tested).
4. Outputs measured one at a time.

11 AC CHARACTERISTICS

V_{DD} = 2.25 to 6.0 V; V_{SS} = 0 V; T_{amb} = –40 to +80 °C; R_O = 1 MΩ; C_O = 680 pF; all timing values are referenced to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Inputs CLB, DATA and DLEN (see Fig.12)						
t_{SUDA}	data set-up time		3	–	–	µs
t_{HDDA}	data hold time		3	–	–	µs
t_{SUEN}	enable set-up time		1	–	–	µs
t_{SUDI}	disable set-up time		2	–	–	µs
t_{SULD}	load pulse set-up time		2.5	–	–	µs
t_{BUSY}	busy time		3	–	–	µs
t_{WH}	CLB HIGH time		1	–	–	µs
t_{WL}	CLB LOW time		5	–	–	µs
t_{CLB}	CLB cycle time		10	–	–	µs
t_r	rise time		–	–	10	µs
t_f	fall time		–	–	10	µs
LCD timing (see Figs. 12, 14, 15, 16 and 17)						
f_{LCD}	LCD frame frequency					
	PCF2100C, PCF2111C		60	75	100	Hz
	PCF2112C	C_O = 1.5 nF	30	35	50	Hz
t_{BS}	transfer time with test loads	V_{DD} = 5 V	–	20	100	µs
t_{PLCD}	driver delay time with test loads	V_{DD} = 5 V	–	20	100	µs

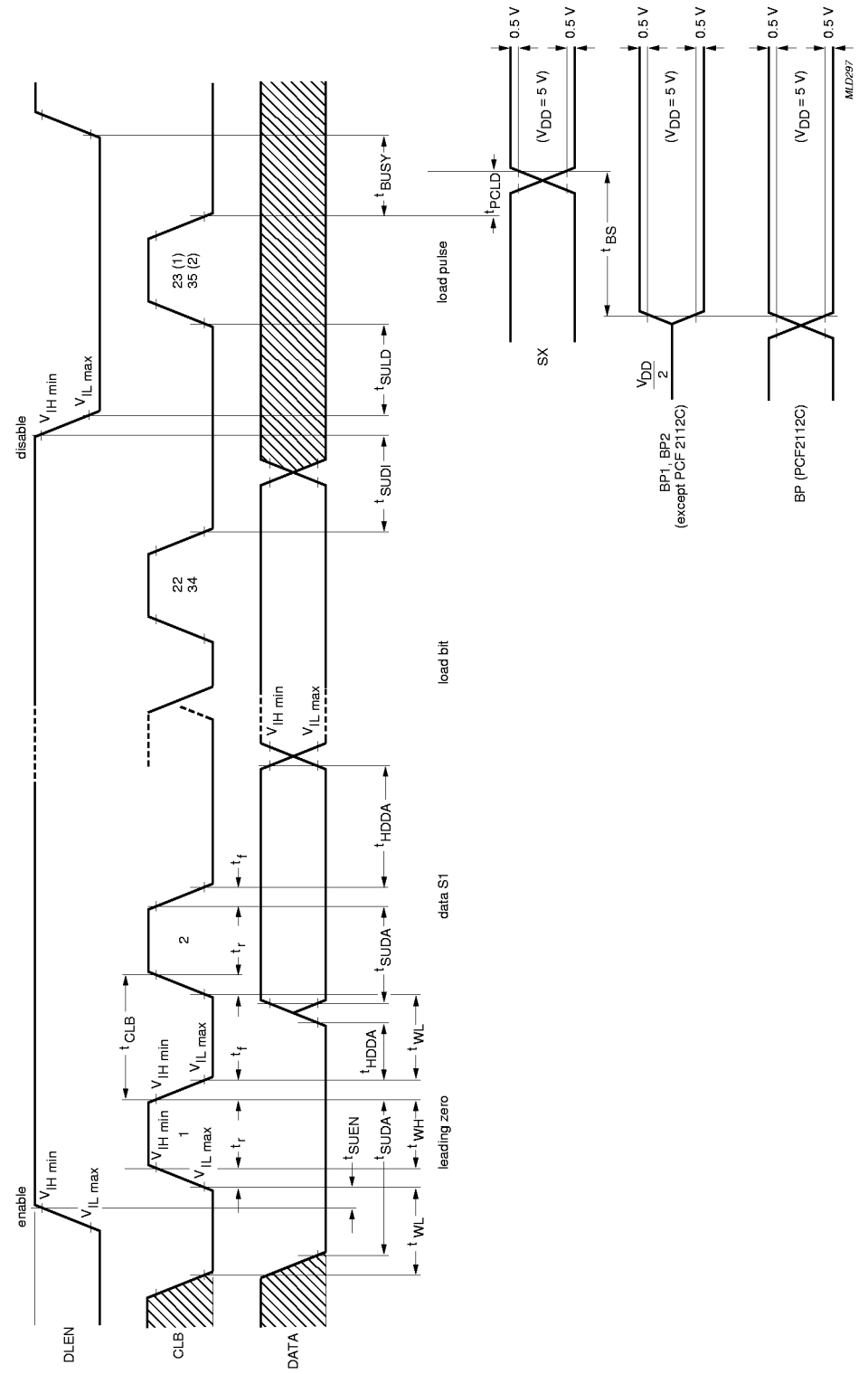
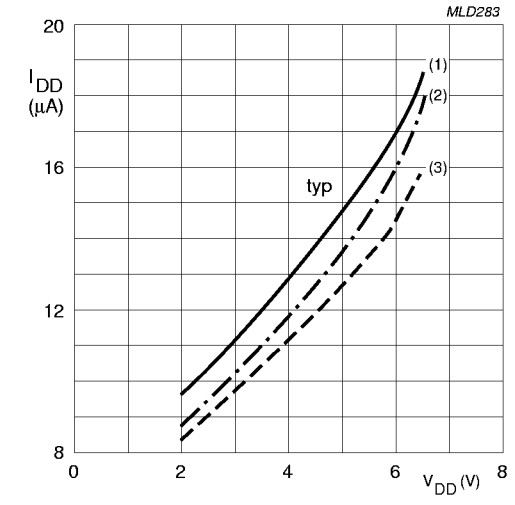


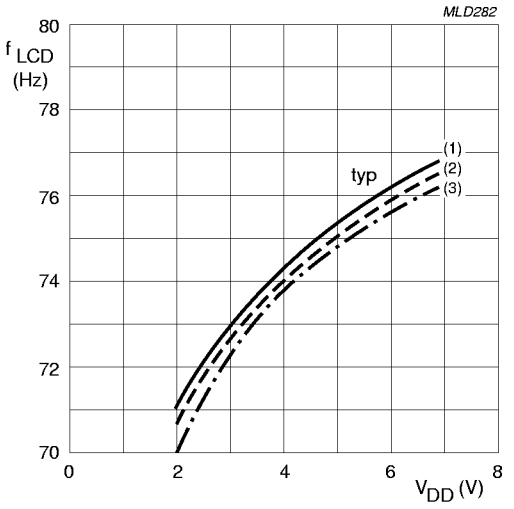
Fig.12 CBUS timing.

(1) Load pulse 23 for PCF2100C (see Fig.7).
(2) Load pulse 35 for PCF2111C and PCF2112C (see Fig.7).



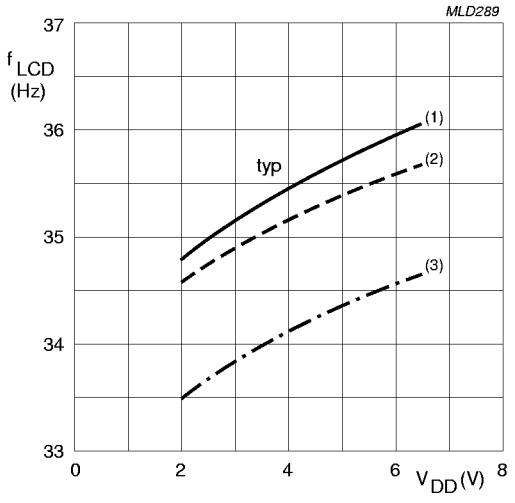
(1) T_{amb} = −40 °C.
(2) T_{amb} = +85 °C.
(3) T_{amb} = +25 °C.

Fig.13 Supply current as a function of supply voltage.



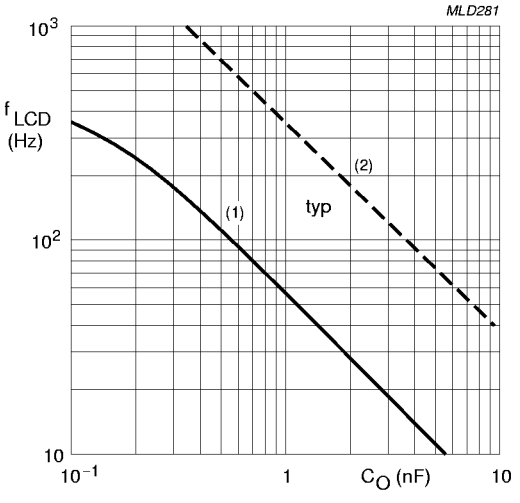
(1) T_{amb} = −40 °C.
(2) T_{amb} = +25 °C.
(3) T_{amb} = +85 °C.

Fig.14 Display frequency as a function of supply voltage; C_O = 680 pF (except PCF2112C).



(1) T_{amb} = −40 °C.
(2) T_{amb} = +25 °C.
(3) T_{amb} = +85 °C.

Fig.15 Display frequency as a function of supply voltage; C_O = 1.5 nF (only PCF2112C).



(1) R_O = 1 MΩ.
(2) R_O = 100 kΩ.

Fig.16 Display frequency as a function of R_O and C_O; T_{amb} = 25 °C; V_{DD} = 5 V.

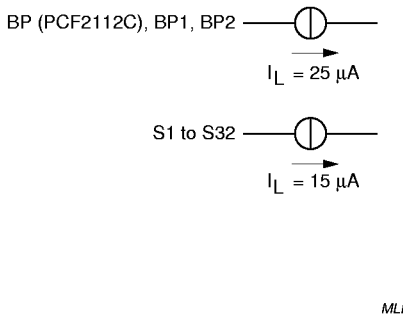
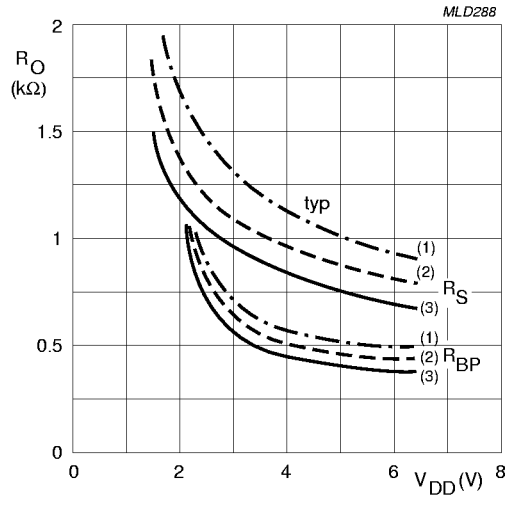
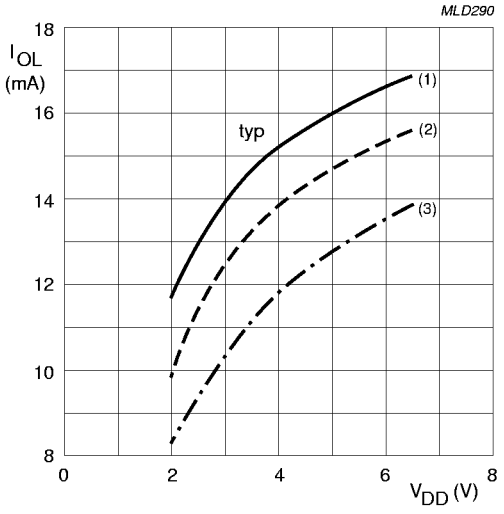


Fig.17 Test loads.



(1) T_{amb} = +85 °C.
(2) T_{amb} = +25 °C.
(3) T_{amb} = −40 °C.

Fig.18 Output resistance of backplane and segments.

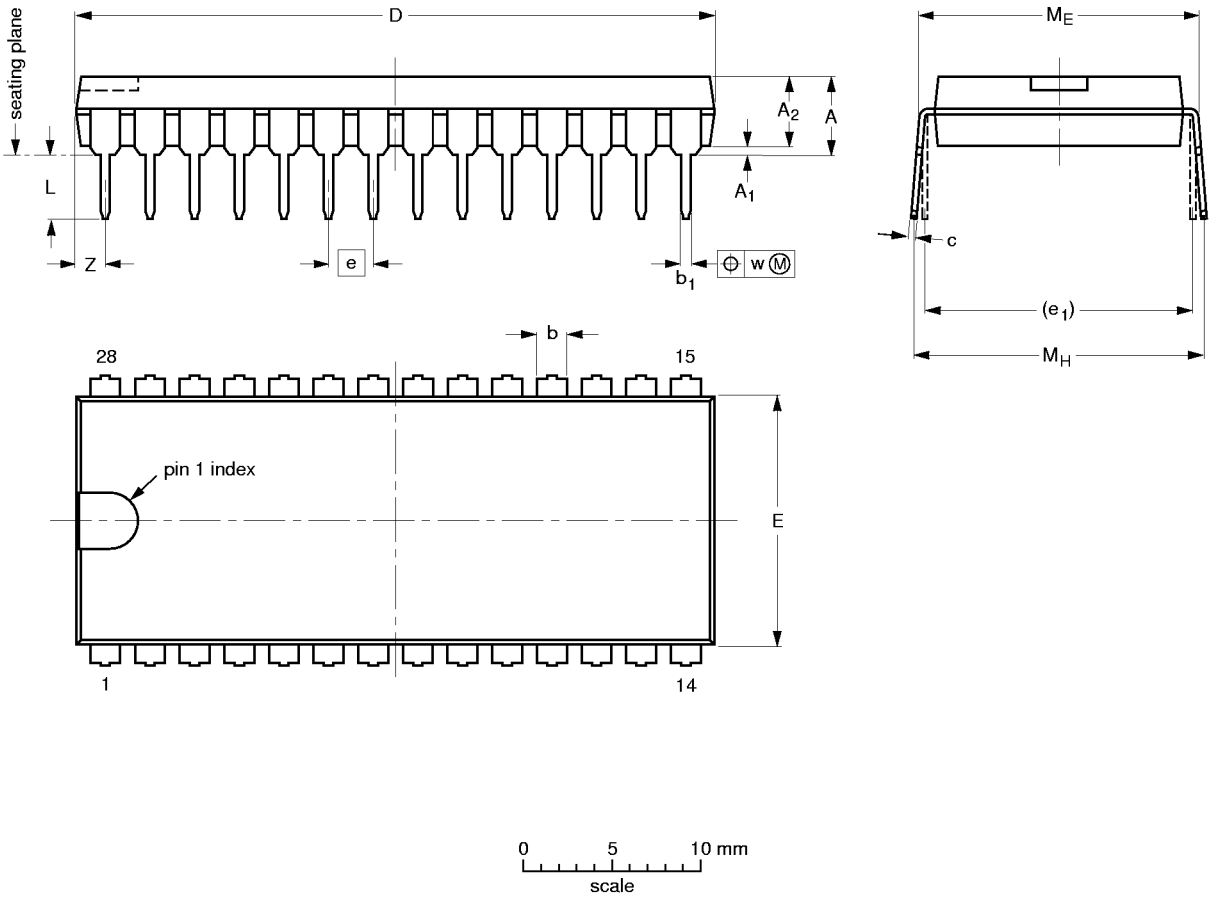


(1) T_{amb} = −40 °C.
(2) T_{amb} = +25 °C.
(3) T_{amb} = +85 °C.

Fig.19 LOW level output current as a function of supply voltage (only PCF2112C).

12 PACKAGE OUTLINES

DIP28: plastic dual in-line package; 28 leads (600 mil) **SOT117-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

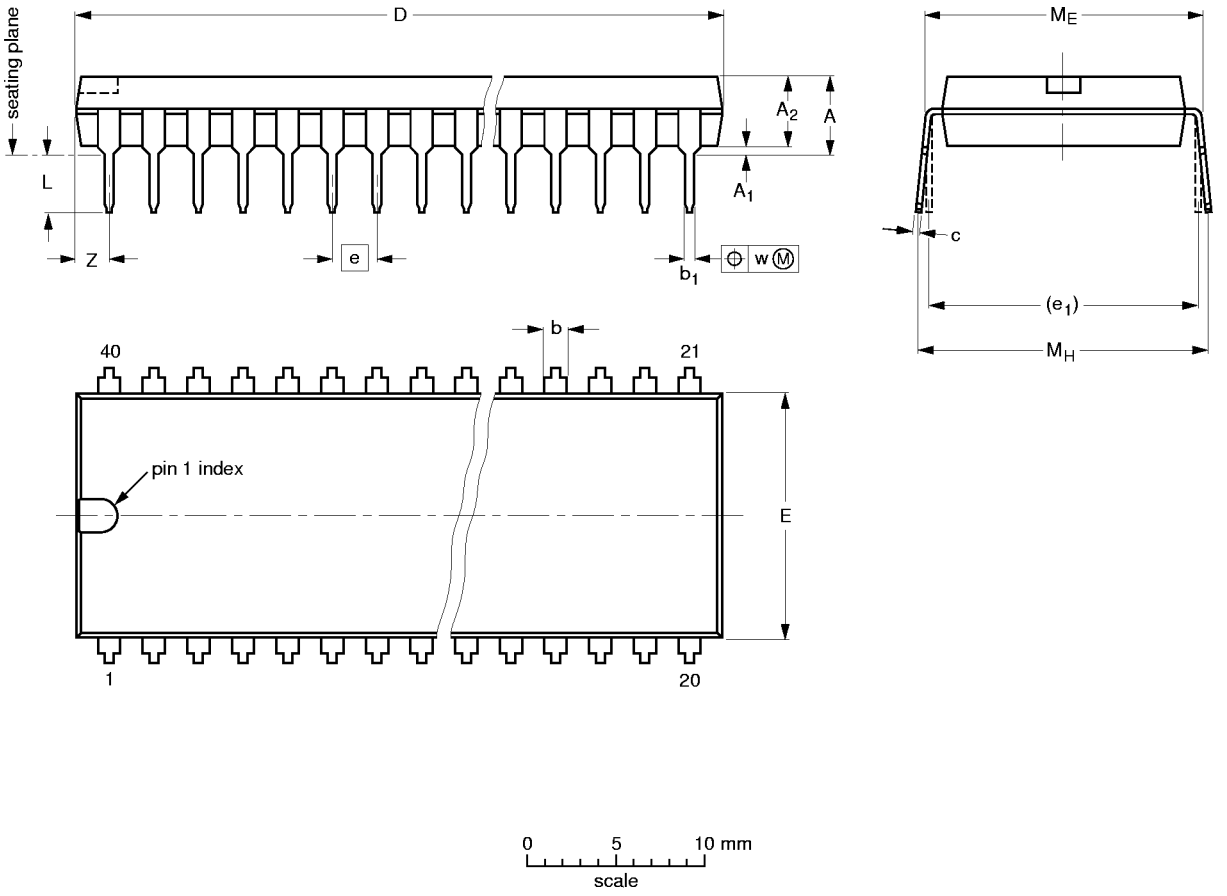
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.1	0.51	4.0	1.7 1.3	0.53 0.38	0.32 0.23	36.0 35.0	14.1 13.7	2.54	15.24	3.9 3.4	15.80 15.24	17.15 15.90	0.25	1.7
inches	0.20	0.020	0.16	0.066 0.051	0.020 0.014	0.013 0.009	1.41 1.34	0.56 0.54	0.10	0.60	0.15 0.13	0.62 0.60	0.68 0.63	0.01	0.067

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT117-1	051G05	MO-015AH				~~92-11-17~~ 95-01-14

DIP40: plastic dual in-line package; 40 leads (600 mil) **SOT129-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

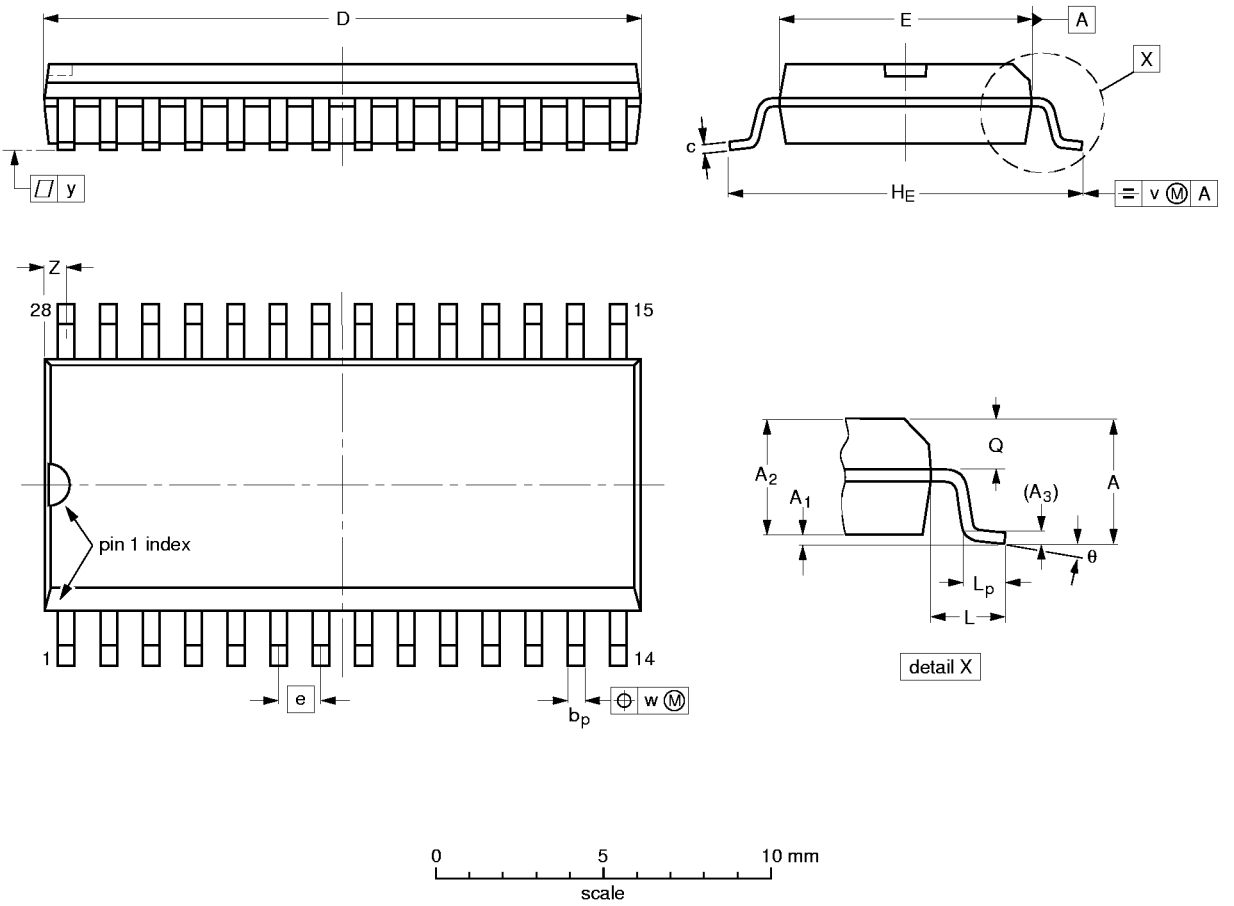
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	$D^{(1)}$	$E^{(1)}$	e	e_1	L	M_E	M_H	w	$Z^{(1)}$ max.
mm	4.7	0.51	4.0	1.70 1.14	0.53 0.38	0.36 0.23	52.50 51.50	14.1 13.7	2.54	15.24	3.60 3.05	15.80 15.24	17.42 15.90	0.254	2.25
inches	0.19	0.020	0.16	0.067 0.045	0.021 0.015	0.014 0.009	2.067 2.028	0.56 0.54	0.10	0.60	0.14 0.12	0.62 0.60	0.69 0.63	0.01	0.089

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT129-1	051G08	MO-015AJ				~~92-11-17~~ 95-01-14

SO28: plastic small outline package; 28 leads; body width 7.5 mm **SOT136-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

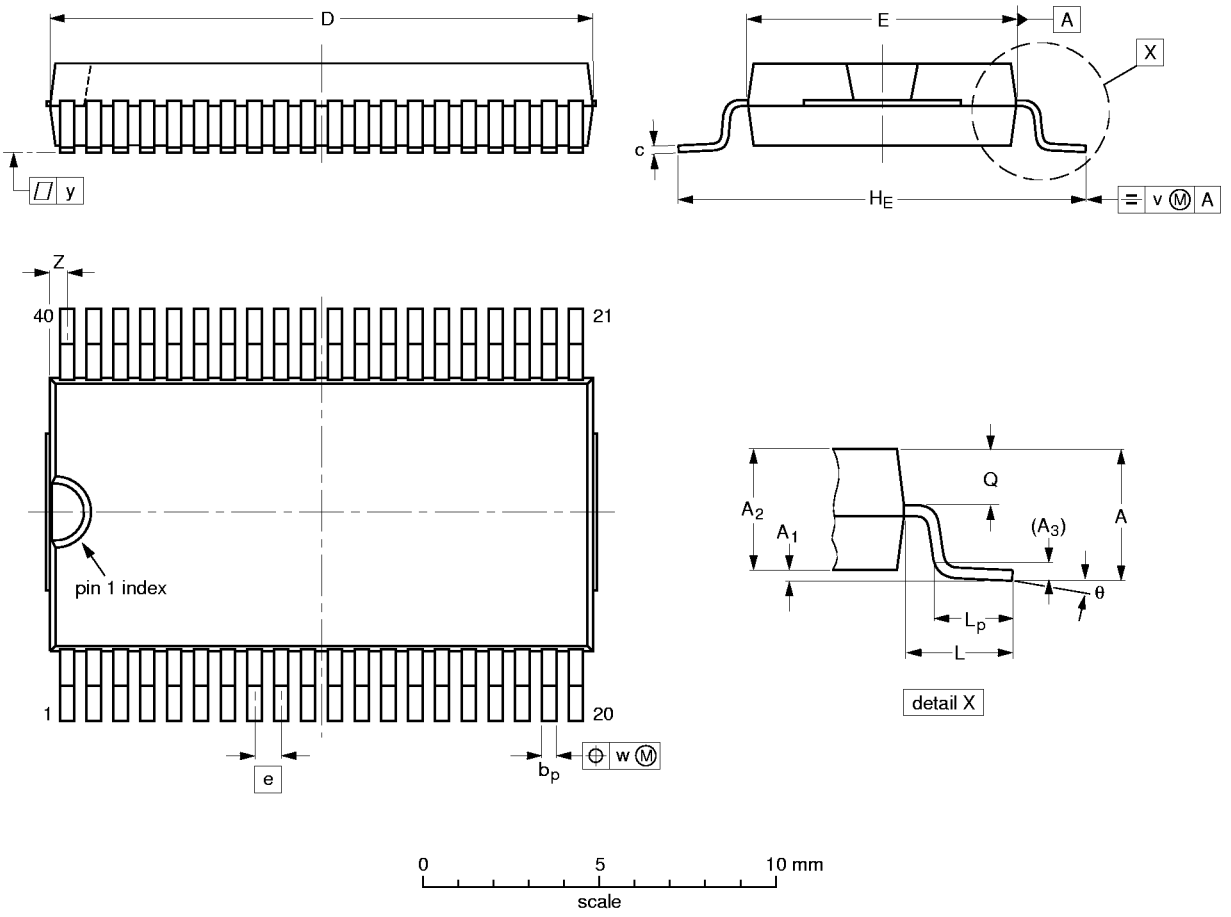
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	18.1 17.7	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.71 0.69	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT136-1	075E06	MS-013AE				~~91-08-13~~ 95-01-24

VSO40: plastic very small outline package; 40 leads **SOT158-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.70	0.3 0.1	2.45 2.25	0.25	0.42 0.30	0.22 0.14	15.6 15.2	7.6 7.5	0.762	12.3 11.8	2.25	1.7 1.5	1.15 1.05	0.2	0.1	0.1	0.6 0.3	7° 0°
inches	0.11	0.012 0.004	0.096 0.089	0.010	0.017 0.012	0.0087 0.0055	0.61 0.60	0.30 0.29	0.03	0.48 0.46	0.089	0.067 0.059	0.045 0.041	0.008	0.004	0.004	0.024 0.012	

Notes

1. Plastic or metal protrusions of 0.4 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT158-1						~~92-11-17~~ 95-01-24

13 SOLDERING

13.1 Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

13.2 DIP

13.2.1 SOLDERING BY DIPPING OR BY WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

13.2.2 REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

13.3 SO and VSO

13.3.1 REFLOW SOLDERING

Reflow soldering techniques are suitable for all SO and VSO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

13.3.2 WAVE SOLDERING

Wave soldering techniques can be used for all SO and VSO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

13.3.3 REPAIRING SOLDERED JOINTS

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.