**Preferred Device** 

#### **Triacs**

### **Silicon Bidirectional Thyristors**

Designed for high volume, low cost, industrial and consumer applications such as motor control; process control; temperature, light and speed control.

#### **Features**

- Small Size Surface Mount DPAK Package
- Passivated Die for Reliability and Uniformity
- Blocking Voltage to 800 V
- On-State Current Rating of 4.0 A RMS at 108°C
- High Immunity to dv/dt 500 V/µs at 125°C
- High Immunity to di/dt 6.0 A/ms at 125°C
- Epoxy Meets UL 94 V-0 @ 0.125 in
- ESD Ratings: Human Body Model, 3B > 8000 V Machine Model, C > 400 V
- Pb-Free Packages are Available

#### MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Repetitive Off–State Voltage (Note 1) (T <sub>J</sub> = -40 to 125°C, Sine Wave, 50 to 60 Hz, Gate Open)	$V_{ m DRM,} \ V_{ m RRM}$		V
MAC4DCM MAC4DCN		600 800	
On–State RMS Current (Full Cycle Sine Wave, 60 Hz, T <sub>C</sub> = 108°C)	I <sub>T(RMS)</sub>	4.0	A
Peak Non-Repetitive Surge Current (One Full Cycle Sine Wave, 60 Hz, T <sub>J</sub> = 125°C)	I <sub>TSM</sub>	40	A
Circuit Fusing Consideration (t = 8.3 msec)	l <sup>2</sup> t	6.6	A <sup>2</sup> sec
Peak Gate Power (Pulse Width ≤ 10 μsec, T <sub>C</sub> = 108°C)	P <sub>GM</sub>	0.5	W
Average Gate Power (t = 8.3 msec, T <sub>C</sub> = 108°C)	$P_{G(AV)}$	0.1	W
Peak Gate Current (Pulse Width ≤ 10 μsec, T <sub>C</sub> = 108°C)	I <sub>GM</sub>	0.5	Α
Peak Gate Voltage (Pulse Width ≤ 10 μsec, T <sub>C</sub> = 108°C)	$V_{GM}$	5.0	V
Operating Junction Temperature Range	$T_J$	-40 to 125	°C
Storage Temperature Range	T <sub>stg</sub>	-40 to 150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

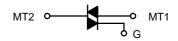
 V<sub>DRM</sub> and V<sub>RRM</sub> for all types can be applied on a continuous basis. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the device are exceeded.



#### ON Semiconductor®

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# TRIACS 4.0 AMPERES RMS 600 – 800 VOLTS



#### MARKING DIAGRAMS

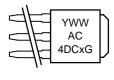


DPAK CASE 369C STYLE 6





DPAK-3 CASE 369D STYLE 6



PIN ASSIGNMENT			
1	Main Terminal 1		
2	Main Terminal 2		
3	Gate		
4	Main Terminal 2		

#### **ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

**Preferred** devices are recommended choices for future use and best overall value.

#### THERMAL CHARACTERISTICS

Characteristic		Max	Unit
Thermal Resistance, - Junction-to-Case - Junction-to-Ambient - Junction-to-Ambient (Note 2)	$egin{array}{c} R_{ heta JC} \ R_{ heta JA} \ R_{ heta JA} \end{array}$	3.5 88 80	°C/W
Maximum Lead Temperature for Soldering Purposes (Note 3)	TL	260	°C

Characteristic	Symbol	Min	Тур	Max	Unit
OFF CHARACTERISTICS	•				
Peak Repetitive Blocking Current $(V_D = Rated \ V_{DRM}, \ V_{RRM}; \ Gate \ Open) \\ T_J = 25^{\circ}C \\ T_J = 125^{\circ}C$	I <sub>DRM,</sub> I <sub>RRM</sub>	- -	- -	0.01 2.0	mA
ON CHARACTERISTICS					
Peak On–State Voltage (Note 4) ( $I_{TM} = \pm 6.0 \text{ A}$ )	$V_{TM}$	_	1.3	1.6	V
Gate Trigger Current (Continuous dc) ( $V_D$ = 12 $V$ , $R_L$ = 100 $\Omega$ ) MT2(+), G(+) MT2(+), G(-) MT2(-), G(-)	I <sub>GT</sub>	8.0 8.0 8.0	12 18 22	35 35 35	mA
Gate Trigger Voltage (Continuous dc) ( $V_D$ = 12 V, $R_L$ = 100 $\Omega$ ) MT2(+), G(+) MT2(+), G(-) MT2(-), G(-)	V <sub>GT</sub>	0.5 0.5 0.5	0.8 0.8 0.8	1.3 1.3 1.3	V
Gate Non–Trigger Voltage (Continuous dc) (V <sub>D</sub> = 12 V, R <sub>L</sub> = 100 $\Omega$ ) MT2(+), G(+); MT2(+), G(-); MT2(-), G(-) T <sub>J</sub> = 125 $^{\circ}$ C	$V_{\sf GD}$	0.2	0.4	-	V
Holding Current (V <sub>D</sub> = 12 V, Gate Open, Initiating Current = ±200 mA)	I <sub>H</sub>	6.0	22	35	mA
Latching Current ( $V_D = 12 \text{ V}, I_G = 35 \text{ mA}$ ) MT2(+), G(+) MT2(+), G(-) MT2(-), G(-)	ΙL	- - -	30 50 20	60 80 60	mA
DYNAMIC CHARACTERISTICS					
Rate of Change of Commutating Current ( $V_D = 400~V$ , $I_{TM} = 4.0~A$ , Commutating dv/dt = 18 V/ $\mu$ sec, Gate Open, $T_J = 125^{\circ}$ C, $f = 250~Hz$ , $CL = 5.0~\mu$ F, $LL = 20~m$ H, No Snubber) (See Figure 16)	di/dt(c)	6.0	8.4	-	A/ms
Critical Rate of Rise of Off–State Voltage $(V_D = 0.67 \text{ X Rated } V_{DRM}, \text{ Exponential Waveform, Gate Open, } T_J = 125^{\circ}C)$	dv/dt	500	1700	-	V/μs

- These ratings are applicable wl
   1/8" from case for 10 seconds. These ratings are applicable when surface mounted on the minimum pad sizes recommended.
- 4. Pulse Test: Pulse Width ≤ 2.0 msec, Duty Cycle ≤ 2%.

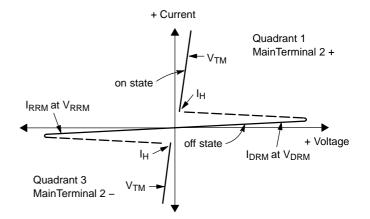
#### **ORDERING INFORMATION**

Device	Package Type	Package	Shipping <sup>†</sup>
MAC4DCM-001	DPAK-3	369D	75 Units / Rail
MAC4DCM-1G	DPAK-3 (Pb-Free)	369D	75 Units / Rail
MAC4DCMT4	DPAK	369C	2500 / Tape & Reel
MAC4DCMT4G	DPAK (Pb-Free)	369C	2500 / Tape & Reel
MAC4DCN-001	DPAK-3	369D	75 Units / Rail
MAC4DCN-1G	DPAK-3 (Pb-Free)	369D	75 Units / Rail
MAC4DCNT4	DPAK	369C	2500 / Tape & Reel
MAC4DCNT4G	DPAK (Pb-Free)	369C	2500 / Tape & Reel

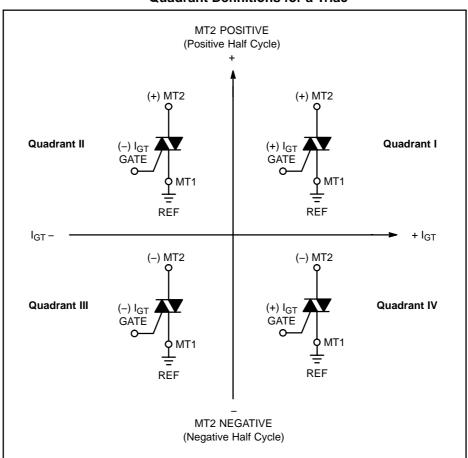
<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# Voltage Current Characteristic of Triacs (Bidirectional Device)

Symbol	Parameter
$V_{DRM}$	Peak Repetitive Forward Off–State Voltage
I <sub>DRM</sub>	Peak Forward Blocking Current
$V_{RRM}$	Peak Repetitive Reverse Off–State Voltage
I <sub>RRM</sub>	Peak Reverse Blocking Current
V <sub>TM</sub>	Maximum On-State Voltage
I <sub>H</sub>	Holding Current



#### **Quadrant Definitions for a Triac**



All polarities are referenced to MT1.

With in-phase signals (using standard AC lines) quadrants I and III are used.

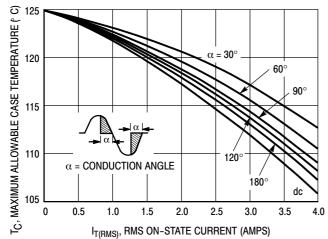


Figure 1. RMS Current Derating

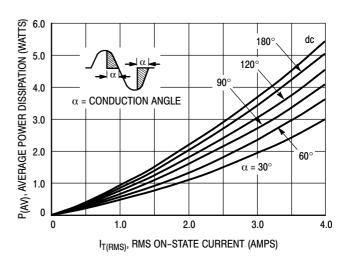


Figure 2. On-State Power Dissipation

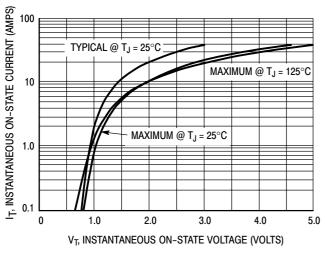
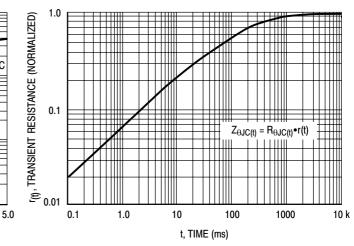


Figure 3. On-State Characteristics



**Figure 4. Transient Thermal Response** 

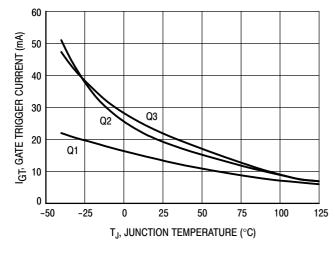


Figure 5. Typical Gate Trigger Current versus Junction Temperature

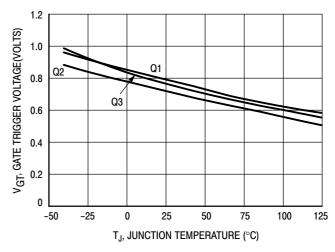
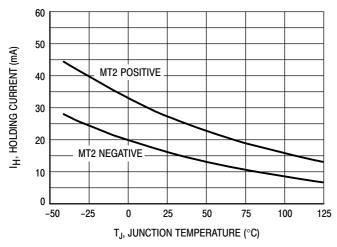


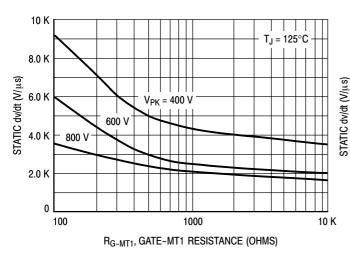
Figure 6. Typical Gate Trigger Voltage versus
Junction Temperature



120 100 IL, LATCHING CURRENT (mA) Q2 Q1 40 Q3 20 0 25 -25 50 100 -50 125 T<sub>J</sub>, JUNCTION TEMPERATURE (°C)

Figure 7. Typical Holding Current versus Junction Temperature

Figure 8. Typical Latching Current versus Junction Temperature



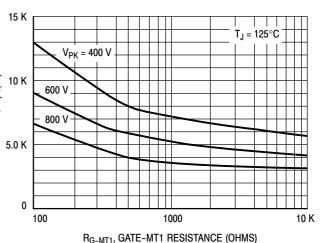
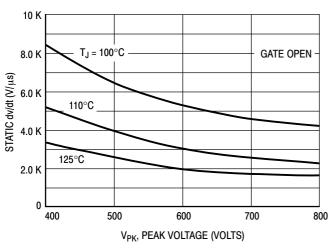


Figure 9. Exponential Static dv/dt versus Gate-MT1 Resistance, MT2(+)

Figure 10. Exponential Static dv/dt versus Gate-MT1 Resistance, MT2(-)



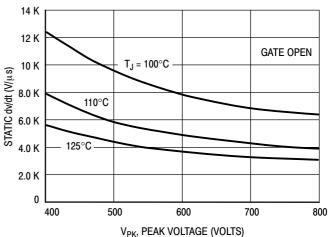


Figure 11. Exponential Static dv/dt versus Peak Voltage, MT2(+)

Figure 12. Exponential Static dv/dt versus Peak Voltage, MT2(-)

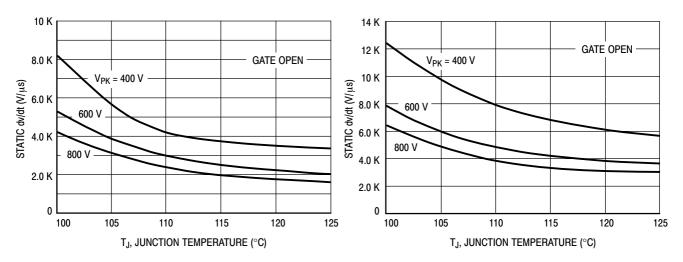


Figure 13. Typical Exponential Static dv/dt versus Junction Temperature, MT2(+)

Figure 14. Typical Exponential Static dv/dt versus Junction Temperature, MT2(-)

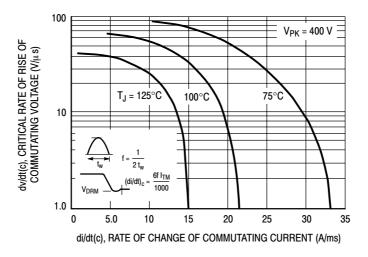
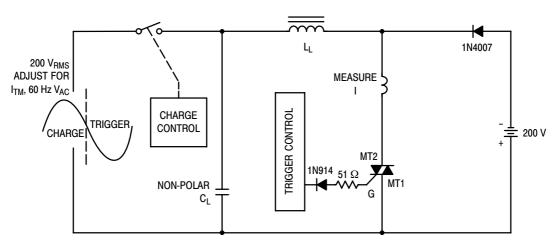


Figure 15. Critical Rate of Rise of Commutating Voltage

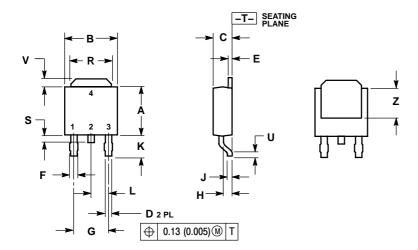


Note: Component values are for verification of rated (di/dt)<sub>c</sub>. See AN1048 for additional information.

Figure 16. Simplified Test Circuit to Measure the Critical Rate of Rise of Commutating Current (di/dt)<sub>c</sub>

#### **PACKAGE DIMENSIONS**

#### **DPAK** CASE 369C ISSUE O

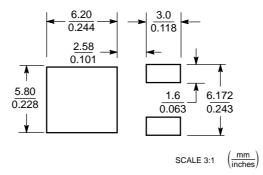


- NOTES: 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. 2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIN	METERS	
DIM	MIN	MAX	MIN	MAX	
Α	0.235	0.245	5.97	6.22	
В	0.250	0.265	6.35	6.73	
С	0.086	0.094	2.19	2.38	
D	0.027	0.035	0.69	0.88	
E	0.018	0.023	0.46	0.58	
F	0.037	0.045	0.94	1.14	
G	0.180 BSC		4.58	BSC	
Н	0.034	0.040	0.87	1.01	
J	0.018	0.023	0.46	0.58	
K	0.102	0.114	2.60	2.89	
L	0.090	BSC	2.29 BSC		
R	0.180	0.215	4.57	5.45	
S	0.025	0.040	0.63	1.01	
U	0.020		0.51		
٧	0.035	0.050	0.89	1.27	
Z	0.155		3.93		

STYLE 6: PIN 1. MT1 2. MT2 3. GATE 4. MT2

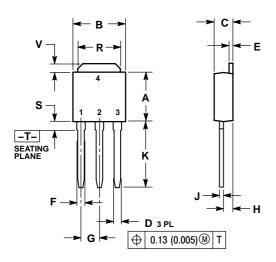
#### **SOLDERING FOOTPRINT\***

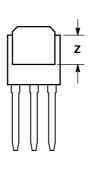


<sup>\*</sup>For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

#### PACKAGE DIMENSIONS

DPAK-3 CASE 369D-01 **ISSUE B** 





#### NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
   CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
Α	0.235	0.245	5.97	6.35
В	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
Е	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090 BSC		2.29 BSC	
Н	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
٧	0.035	0.050	0.89	1.27
Z	0.155		3.93	

## STYLE 6: PIN 1.

- MT1
- 2. 3. MT2
- GATE

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