Am29C821/Am29C823
Am29C921/Am29C923

High-Performance CMOS Bus Interface Registers

DISTINCTIVE CHARACTERISTICS

- High-speed parallel positive edge-triggered registers with D-type flip-flops
  - CP-Y propagation delay = 8 ns typical
- Low standby power
- JEDEC FCT-compatible specs
- I_{OL} = 24 mA, Commercial and Military
- Extra-wide (9- and 10-bit) data paths
- Am29C900 DIP pinout option reduces lead inductance on V_{CC} and GND pins

GENERAL DESCRIPTION

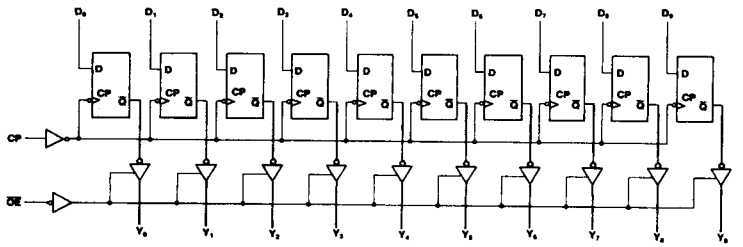
The Am29C821 and Am29C823 CMOS Bus Interface Registers are designed to eliminate the extra devices required to buffer stand alone registers and to provide extra data width for wider address/data paths or buses carrying parity. The Am29C800 registers are produced with AMD's exclusive CS-11 CMOS process, and feature typical propagation delays of 8 ns, as well as an output current drive of 24 mA.

The Am29C821 is a buffered, 10-bit version of the popular '374/'534 function. The Am29C823 is a 9-bit buffered register with Clock Enable ($\overline{EN}$) and Clear ($\overline{CLR}$) — ideal for parity bus interfacing in high-performance microprogrammed systems.

The Am29C821 and Am29C823 are available in the standard package options: DIPs, PLCCs, LCCs, SOICs, and Flatpacks. In addition, a DIP pinout option, featuring center V_{CC} and GND pins, reduces the lead inductance of the V_{CC} and GND pins. The ordering part numbers for CMOS registers with this pinout are the Am29C921 and Am29C923; their pinouts are shown later in this data sheet.

BLOCK DIAGRAMS

Am29C821



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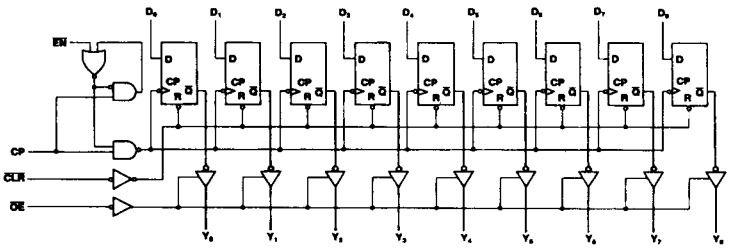
Am29C823



BD005481

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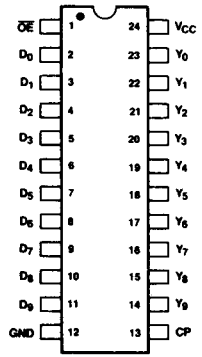
Issue Date: January 1988

CONNECTION DIAGRAMS
Top View

Am29C821

DIPs*



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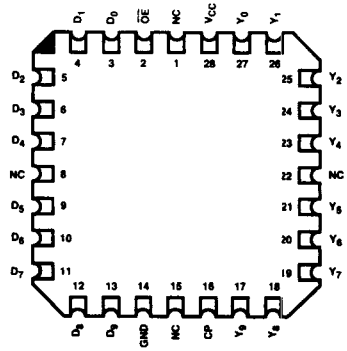

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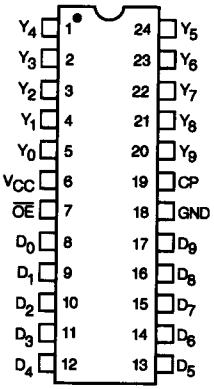
Am29C921

DIPs



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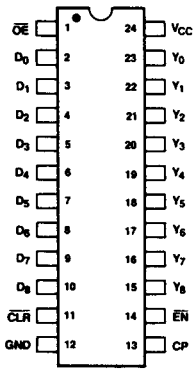
Am29C823

DIPs*



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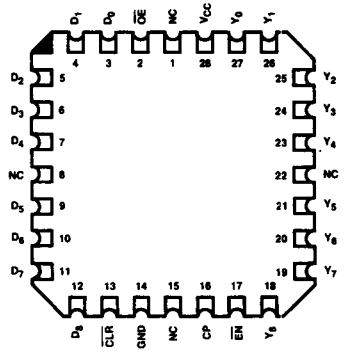
LCC**



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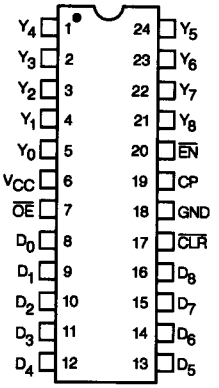
*Also available in 24-Pin Flatpack and Small Outline packages; pinout identical to DIPs.
**Also available in 28-Pin PLCC; pinout identical to LCC.

Am29C923

DIPs



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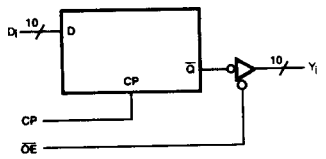
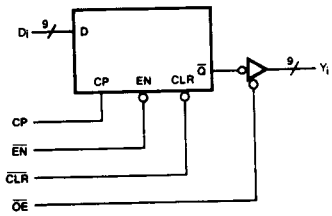
LOGIC SYMBOLS

Am29C821



LS000452

Am29C823



LS000432

FUNCTION TABLES

Am29C821

Inputs			Internal	Outputs	
$\overline{OE}$	D_I	CP	$\overline{Q_I}$	Y_I	Function
H	L	↑	H	Z	Hi-Z
H	H	↑	L	Z	
L	L	↑	H	L	Load
L	H	↑	L	H	

Am29C823

Inputs					Internal	Outputs	
$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	D_I	CP	$\overline{Q_I}$	Y_I	Function
H	H	L	L	↑	H	Z	Hi-Z
H	H	L	H	↑	L	Z	
H	L	X	X	X	H	Z	Clear
L	L	X	X	X	H	L	
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	
H	H	L	L	↑	H	Z	Load
H	H	L	H	↑	L	Z	
L	H	L	L	↑	H	L	
L	H	L	H	↑	L	H	

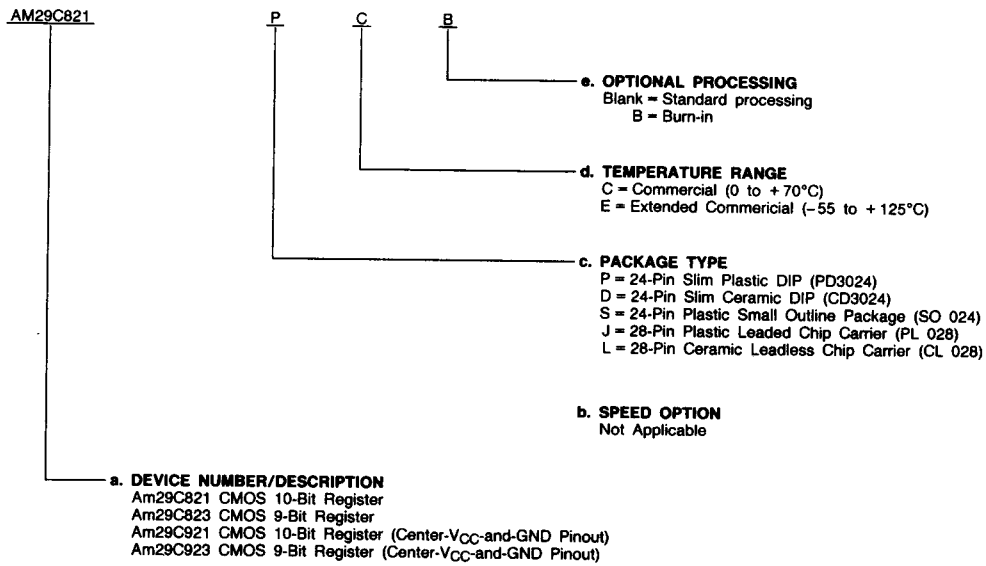
H = HIGH
L = LOW
X = Don't Care

NC = No Change
↑ = LOW-to-HIGH Transition
Z = High Impedance

ORDERING INFORMATION
Standard Products

AMD products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM29C821	PC, PCB, DC, DCB, DE, SC, JC, LC
AM29C823	
AM29C921	PC, PCB, DC, DCB, DE
AM29C923	

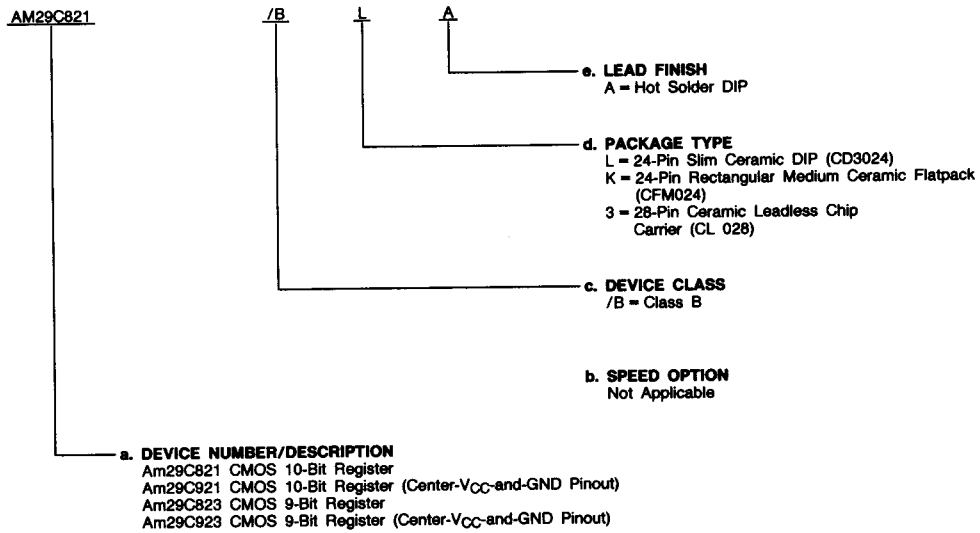
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION (Cont'd.)

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
AM29C821	/BLA, /BKA, /B3A
AM29C823	
AM29C921	/BLA
AM29C923	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups
1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

Am29C821/Am29C823

D_i Data Input (Input)
D_i are the register data inputs.

CP Clock Pulse (Input, LOW-to-HIGH Transition)
Clock Pulse is the clock input for the registers. Data is entered into the registers on the LOW-to-HIGH transitions.

Y_i Data Outputs (Output)
Y_i are the three-state outputs.

$\overline{OE}$ Output Enable (Input, Active LOW)
When the $\overline{OE}$ input is HIGH, the Y_i outputs are in the high-impedance state. When $\overline{OE}$ is LOW, the register data is present at the Y_i outputs.

Am29C823 only:

$\overline{EN}$ Clock Enable (Input, Active LOW)
When $\overline{EN}$ is LOW, data on the D_i inputs are transferred to the $\overline{Q}_i$ outputs on the LOW-to-HIGH clock transition. When $\overline{EN}$ is HIGH, the $\overline{Q}_i$ outputs do not change state, regardless of the data or clock input transitions.

$\overline{CLR}$ Clear (Input, Active LOW)
When $\overline{CLR}$ is LOW, the internal register is cleared. When $\overline{CLR}$ is LOW and $\overline{OE}$ is LOW, the $\overline{Q}_i$ outputs are HIGH. When $\overline{CLR}$ is HIGH, data can be entered into the register.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Supply Voltage to Ground Potential
Continuous ..... −0.5 V to +7.0 V
DC Output Voltage ..... −0.5 V to V_{CC} + 0.5 V
DC Input Voltage ..... −0.5 V to V_{CC} + 0.5 V
DC Output Diode Current: Into Output ..... +50 mA
Out of Output ..... −50 mA
DC Input Diode Current: Into Input ..... +20 mA
Out of Input ..... −20 mA
DC Output Current per Pin: I_{Sink} ..... +48 mA (2 x I_{OL})
I_{Source} ..... −30 mA (2 x I_{OH})
Total DC Ground Current .($n \times I_{OL} + m \times I_{CCT}$) mA (Note 1)
Total DC V_{CC} Current .... ($n \times I_{OH} + m \times I_{CCT}$) mA (Note 1)

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_A) ..... 0 to +70°C
Supply Voltage (V_{CC}) ..... +4.5 V to +5.5 V

Military (M) and Extended Commercial (E) Devices
Temperature (T_A) ..... −55 to +125°C
Supply Voltage (V_{CC}) ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions			Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = 4.5 V, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −15 mA		2.4		Volts
V_{OL}	Output LOW Voltage	V_{CC} = 4.5 V, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24 mA			0.5	Volts
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for All Inputs (Note 2)			2.0		Volts
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for All Inputs (Note 2)				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = 4.5 V, I_{IN} = −18 mA				−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = 5.5 V, V_{IN} = GND				−10	µA
		V_{CC} = 5.5 V, V_{IN} = 0.4 V				−5	
I_{IH}	Input HIGH Current	V_{CC} = 5.5 V, V_{IN} = 2.7 V				5	µA
		V_{CC} = 5.5 V, V_{IN} = 5.5 V				10	
I_{OZH}	Output Off-State Current (High Impedance)	V_{CC} = 5.5 V, V_O = 5.5 V or 2.7 V (Note 3)				+10	µA
I_{OZL}		V_{CC} = 5.5 V, V_O = 0.4 V or GND (Note 3)				−10	µA
I_{SC}	Output Short-Circuit Current	V_{CC} = 5.5 V, V_O = 0 V (Note 4)			−60		mA
I_{CCQ}	Static Supply Current	V_{CC} = 5.5 V, Outputs Open	V_{IN} = V_{CC} or GND	MIL		160	µA
				COM'L		120	
I_{CCT}			V_{IN} = 3.4 V	Data Input		1.5	mA/Bit
				$\overline{OE}$, $\overline{CLR}$, CP, $\overline{EN}$		3.0	
I_{CCD}†	Dynamic Supply Current	V_{CC} = 5.5 V (Note 5)				275	µA/MHz/Bit

Notes: 1. n = number of outputs, m = number of inputs.
2. Input thresholds are tested in combination with other DC parameters or by correlation.
3. Off-state currents are only tested at worst-case conditions of V_{OUT} = 5.5 V or 0.0 V.
4. Not more than one output shorted at a time. Duration should not exceed 100 milliseconds.
5. Measured at a frequency ≤ 10 MHz with 50% duty cycle.

† Not included in Group A tests.

SWITHCING CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

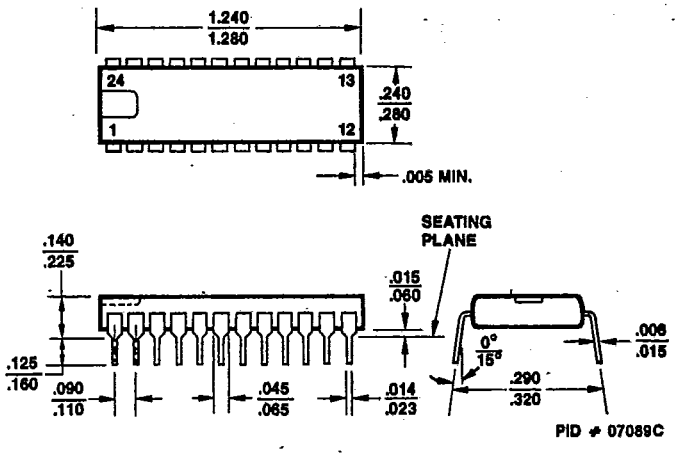
Parameter Symbol	Parameter Description		Test Conditions*	COMMERCIAL Min.	COMMERCIAL Max.	MILITARY Min.	MILITARY Max.	Units
t_{PLH}	Propagation Delay Clock to Y_i ($\overline{OE}$ = LOW)		C_L = 50 pF R_1 = 500 Ω R_2 = 500 Ω		12		14	ns
t_{PHL}					12		14	ns
t_S	Data to CP Setup Time			4		6		ns
t_H	Data to CP Hold Time			2		3		ns
t_S	Enable ($\overline{EN}$ ⎍) to CP Setup Time			4		6		ns
t_S	Enable ($\overline{EN}$ ⎎) to CP Setup Time			4		6		ns
t_H	Enable ($\overline{EN}$) Hold Time			2		3		ns
t_{PHL}	Propagation Delay, Clear to Y_i				13		15	ns
t_{REC}	Clear ($\overline{CLR}$ ⎎) to CP Setup Time			4		6		ns
t_{PWH}	Clock Pulse Width	HIGH		7		11		ns
t_{PWL}		LOW		7		11		ns
t_{PWL}	Clear Pulse Width	LOW		7		11		ns
t_{ZH}	Output Enable Time $\overline{OE}$ ⎍ to Y_i				12		14	ns
t_{ZL}					12		14	ns
t_{HZ}	Output Disable Time $\overline{OE}$ ⎎ to Y_i				12		14	ns
t_{LZ}					12		14	ns

*See Test Circuit and Waveforms.

PACKAGE OUTLINES*

T-90-20

PD3024



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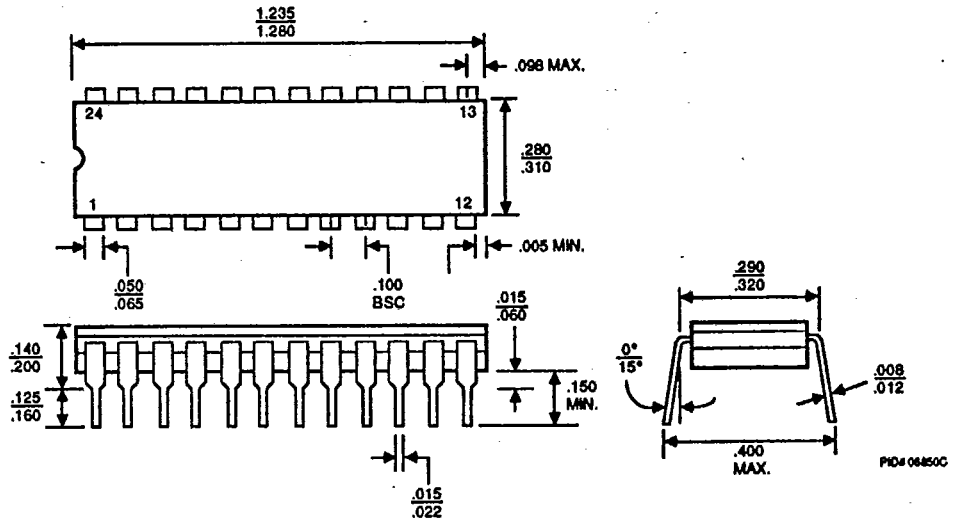

*For reference only.

PACKAGE OUTLINES (Cont'd.)

T-90-20

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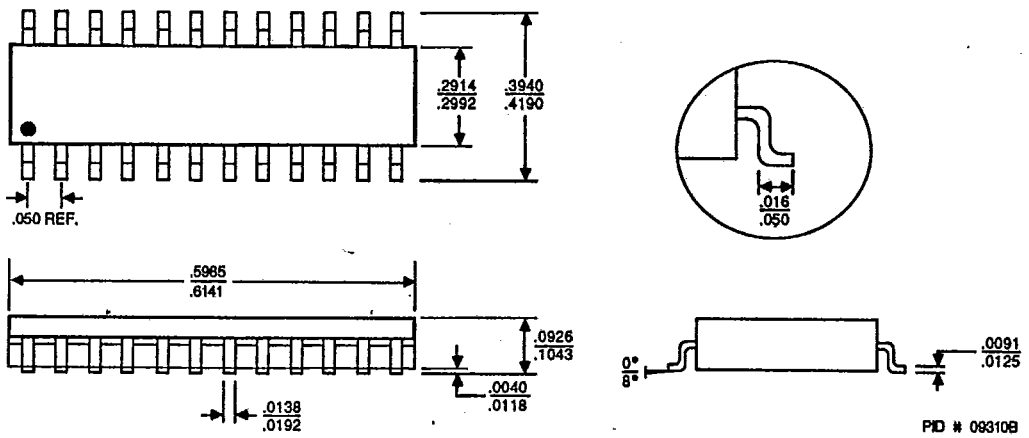

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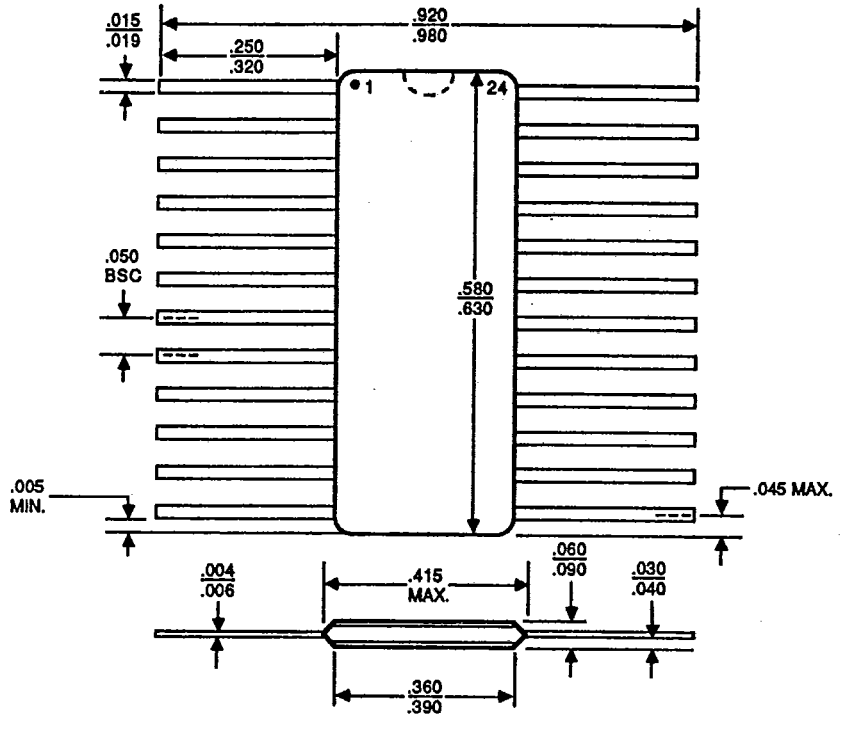

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PACKAGE OUTLINES (Cont'd.)

T-90-20

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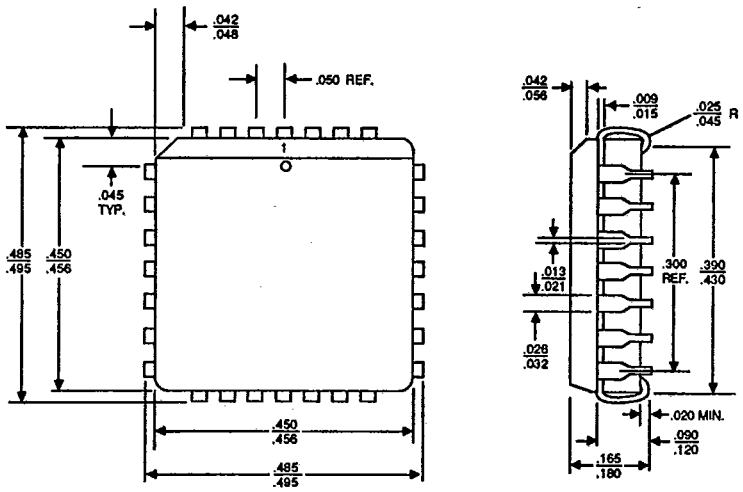

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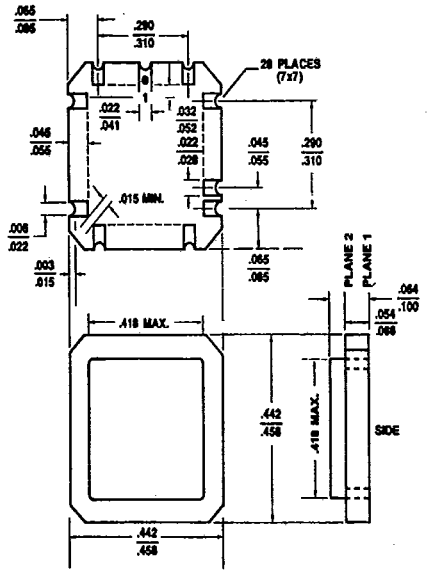

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ADVANCED MICRO DEVICES 901 Thompson Pl., P.O. Box 3453, Sunnyvale, CA 94088, USA
TEL: (408) 732-2400 • TWX: 910-339-9280 • TELEX: 34-6306 • TOLL FREE: (800) 538-8450

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