NEC
ELECTRON DEVICE

BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC1860

BURST LOCK CLOCK GENERATOR

The μPC1860 is an LSI incorporating a PLL circuit to generate nf_{SC} clocks (f_{SC}: color subcarrier frequency), ideal for the processing of digital video signals as in extended definition television (EDTV) systems.

Thanks to the built-in sync separation circuits, phase comparator, and voltage-controlled oscillator (VCO), burst lock clocks can be obtained by merely inputting video signals to this LSI.

FEATURES

- VCO is incorporated (May be used up to 8 f_{SC} clocks).
- Horizontal and vertical sync separation circuits are incorporated (with output pins).
- Horizontal and vertical sync output pulses (TTL level)
- ACC amplifier and killer detector circuits are incorporated.
- 1/4 and 1/8 (1/2 x 1/4) frequency dividers are incorporated.
- f_{SC} phase control circuit is incorporated.
- Applicable to both NTSC and PAL systems.

ORDERING INFORMATION

PART NUMBER	PACKAGE	QUALITY GRADE
μPC1860GS	36-Pin Plastic Shrink SOP (300 mil)	Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

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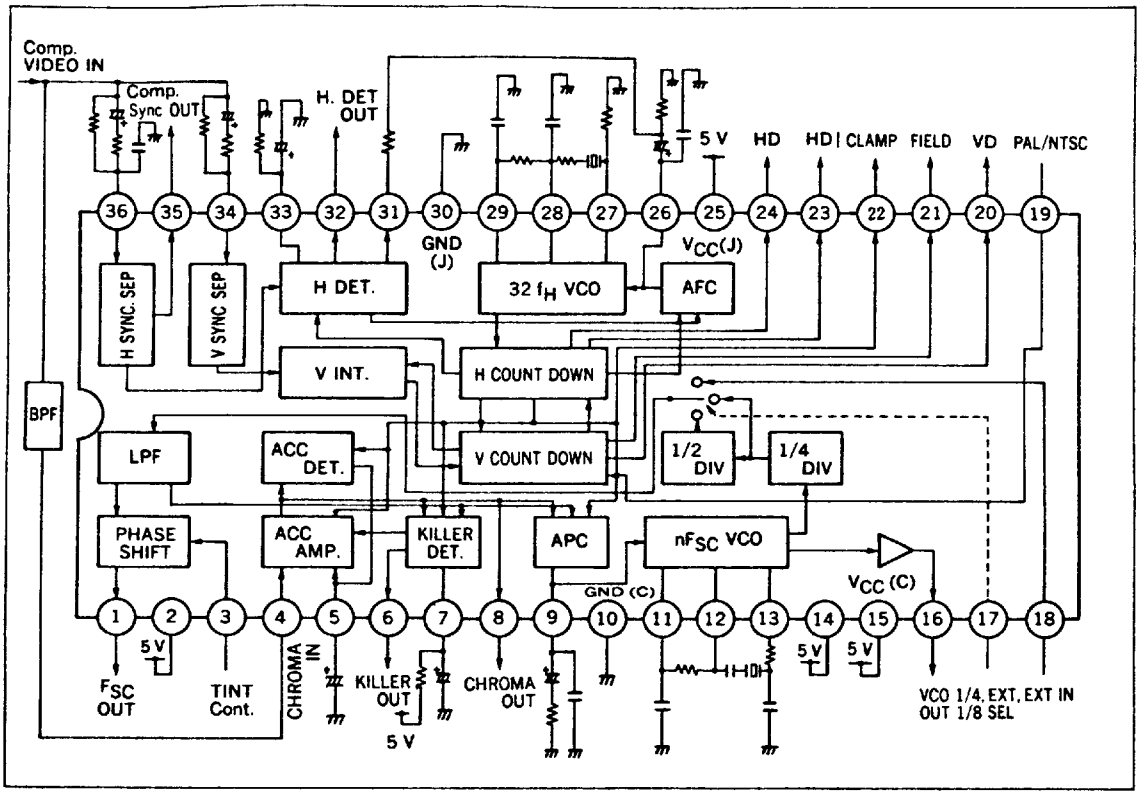
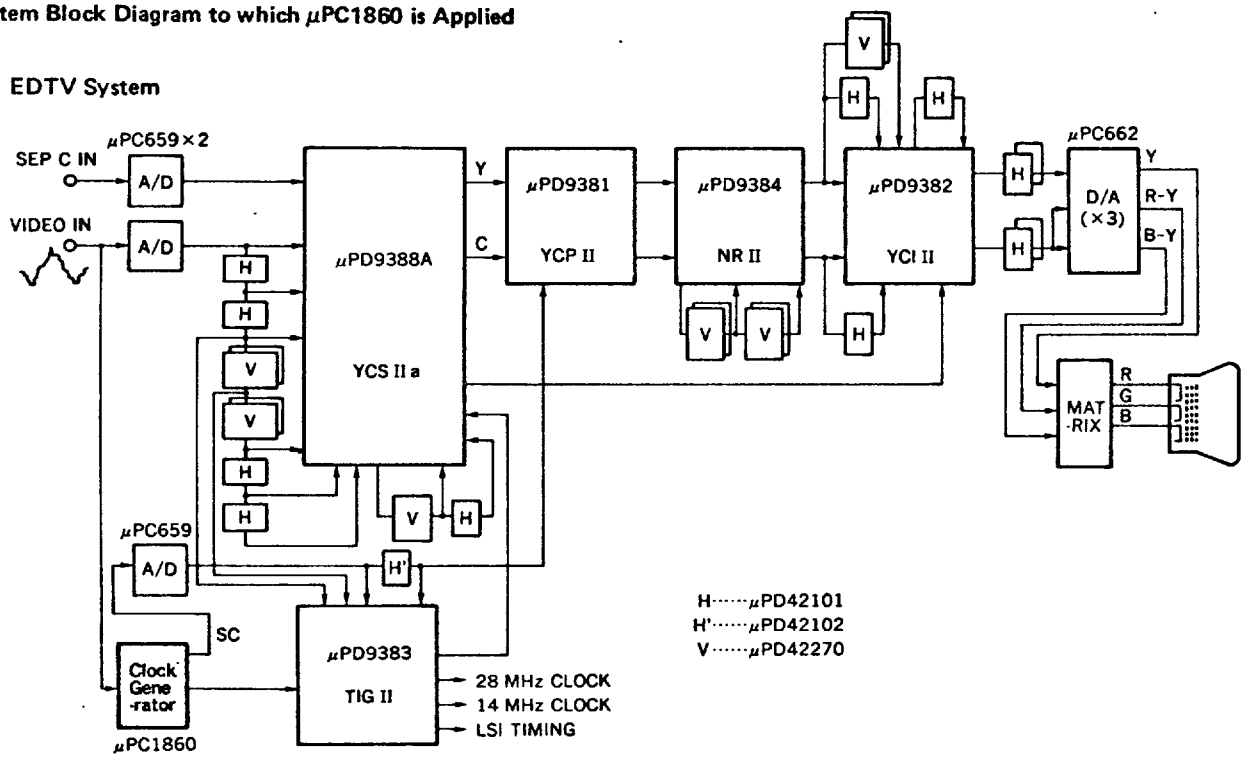
BLOCK DIAGRAM

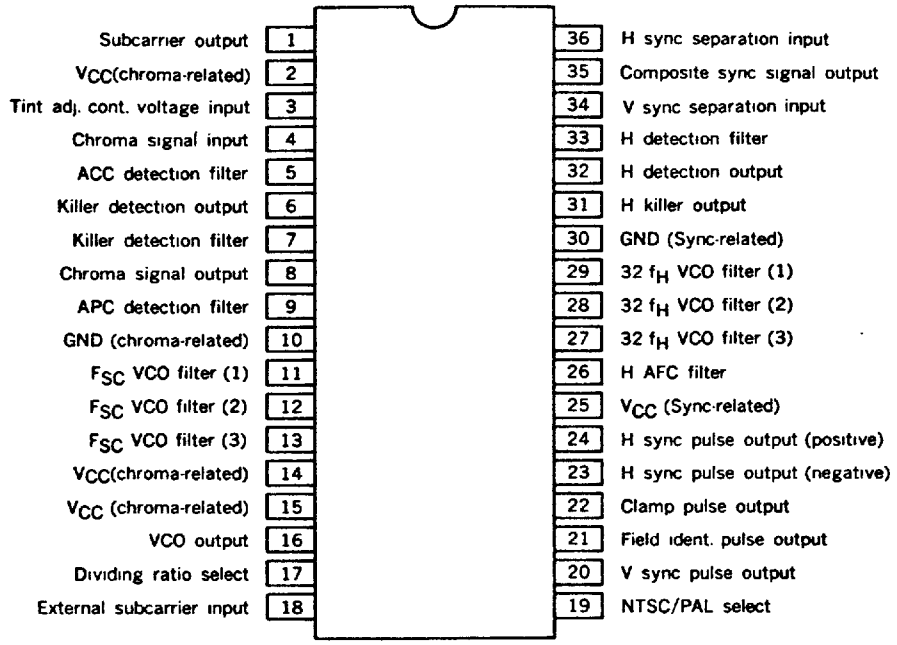


System Block Diagram to which μPC1860 is Applied

(1) EDTV System



PIN ASSIGNMENTS (Top View)



ABSOLUTE MAXIMUM RATINGS (at T_a = 25 °C)

Supply voltage	V_{CC}	7	V
Input signal voltage (Chroma signal)	e_{i4}	3	V_{p-p}
Input signal voltage (H sync separation)	e_{i36}	3	V_{p-p}
Input signal voltage (V sync separation)	e_{i34}	3	V_{p-p}
Input signal voltage (EXT)	e_{i18}	V_{CC}	V_{p-p}
Control signal voltage	e_{c3}	V_{CC}	V
Output current	I_o	−7	mA
Power dissipation of package (when mounted on PCB)	P_D	570 (at T_a = 75 °C)	mW
Operating temperature	T_{opt}	−20 to +75	°C
Storage temperature	T_{stg}	−40 to +150	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input signal voltage (Chroma burst signal)	e_{i4}		150		mV_{p-p}
Input signal voltage (H sync separation)	e_{i36}		1.0		V_{p-p}
Input signal voltage (V sync separation)	e_{i34}		1.0		V_{p-p}
Input signal voltage (EXT IN HIGH voltage)	e_{iH18}	2.0			V
Input signal voltage (EXT IN LOW voltage)	e_{iL18}			0.8	V
Divider select voltage voltage 1 (1/8)	$V_{17(8)}$	4.5			V
Divider selector voltage 2 (1/4)	$V_{17(4)}$			0.5	V
Tint control voltage	V_3		2.5		V
NTSC/PAL select voltage (PAL)	V_{19P}	4.5			V
NTSC/PAL select voltage (NTSC)	V_{19N}			0.5	V
Operating temperature	T_{opt}	−10		+60	°C

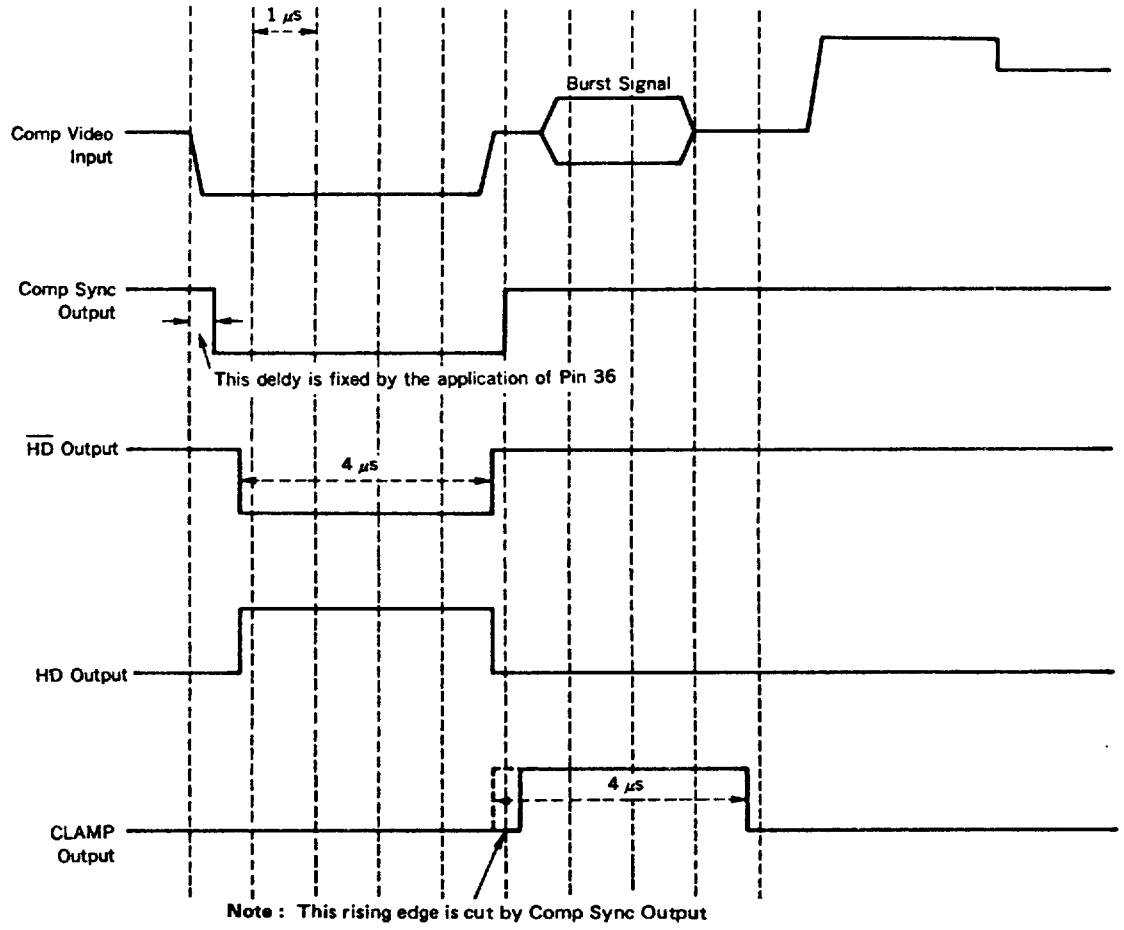
ELECTRICAL CHARACTERISTICS (at T_a = 25 °±3 °C, $R_H \leqq 70$ %, V_{CC} = 12 V)

No.	PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
	<Chroma section>						
1	ACC amplitude characteristic 1	ACC_1	0	1.0	2.0	dB	Fluctuation of chroma output level at +6 dB change of chroma input burst signal (0 dB = 150 mV_{p-p})
2	ACC amplitude characteristic 2	ACC_2	−5.0	−2.0	0	dB	Fluctuation of chroma output level at −20 dB change of chroma input burst signal (0 dB = 150 mV_{p-p})
3	Color killer set point	e_{KS}	−48	−42	−36	dB	Input level at killer ON with chroma input burst sig. (0 dB = 150 mV_{p-p}) being attenuated
4	Color residual of color killer	e_{KR}			10	mV_{p-p}	Residual level of chroma output in Killer ON state when chroma input burst signal of 150 mV_{p-p} is input
5	Chroma output level	E_{OC}		1.65		V_{p-p}	Chroma output level when chroma input burst signal of 150 mV_{p-p} is input
6	Color killer output High level (1)	$E_{KOH(1)}$	2.7	3.5		V	High level of color killer output at color killer OFF I_{OH} = −400 μA
7	Color killer output High level (2)	$E_{KOH(2)}$	3.5	4.0		V	High level of color killer output at color killer OFF I_{OH} = −20 μA
8	Color killer output Low level	E_{KOL}		0.2	0.4	V	Low level of color killer output at color killer ON I_{OL} = +2 mA
9	APC lock-in range	f_P	+400	+600		Hz	Frequency pulled by APC with chroma input burst frequency changed (f_{sc} conversion)
10	VCO control sensitivity	β_P		10		Hz/mV	Rate of variation of frequency when APC filter pin is changed from V to V (f_{sc} conversion)
11	Phase variable range	θ_{CONT}	+40	+45		deg	Amount of phase shift when voltage of phase control pin is set at 2.5 V + 1 V
12	VCO output level	e_{VCO}		1.0		V_{p-p}	VCO output level when chroma input burst signal of 150 mV_{p-p} is input
13	F_{SC} output level	e_{FSC}		240		mV_{p-p}	F_{SC} output level when chroma input burst signal of 150 mV_{p-p} is input
14	Divider select voltage	V_{DIV1}			0.5	V	1/4 freq. division if V17 < V_{DIV1} EXT IN with V17: OPEN 1/8 freq. division if V_{DIV2} < V17
		V_{DIV2}	4.5			V	
15	NTSC/PAL select voltage	$V_{N/P}$	1.7	2.0	2.3	V	f_V = 60 Hz if V19 < $V_{N/P}$ f_V = 50 Hz if $V_{N/P}$ < V19
	<Sync section>						
16	DC level of H sync separation input	V_{SSH}	1.9	2.2	2.5	V	Voltage of Pin No. 36 when connected to GND via 10 kΩ resistor
17	DC level of V sync separation input	V_{SSV}	1.9	2.2	2.5	V	Voltage of Pin No. 34 when connected to GND via 10 kΩ resistor
18	Sync separation output High level (1)	E_{OSH1}	2.7	3.5		V	High level of sync separation output when only 0.3 V_{p-p} sync signal is input to Pin 36 I_{OH} = −400 μA
19	Sync separation output High level (2)	E_{OSH2}	3.5	4.0		V	High level of sync separation output when only 0.3 V_{p-p} sync signal is input to Pin 36 I_{OH} = −20 μA
20	Sync separation output Low level	E_{OSL}		0.2	0.4	V	Low level of sync separation output when only 0.3 V_{p-p} sync signal is input to Pin 36 I_{OL} = +2 mA

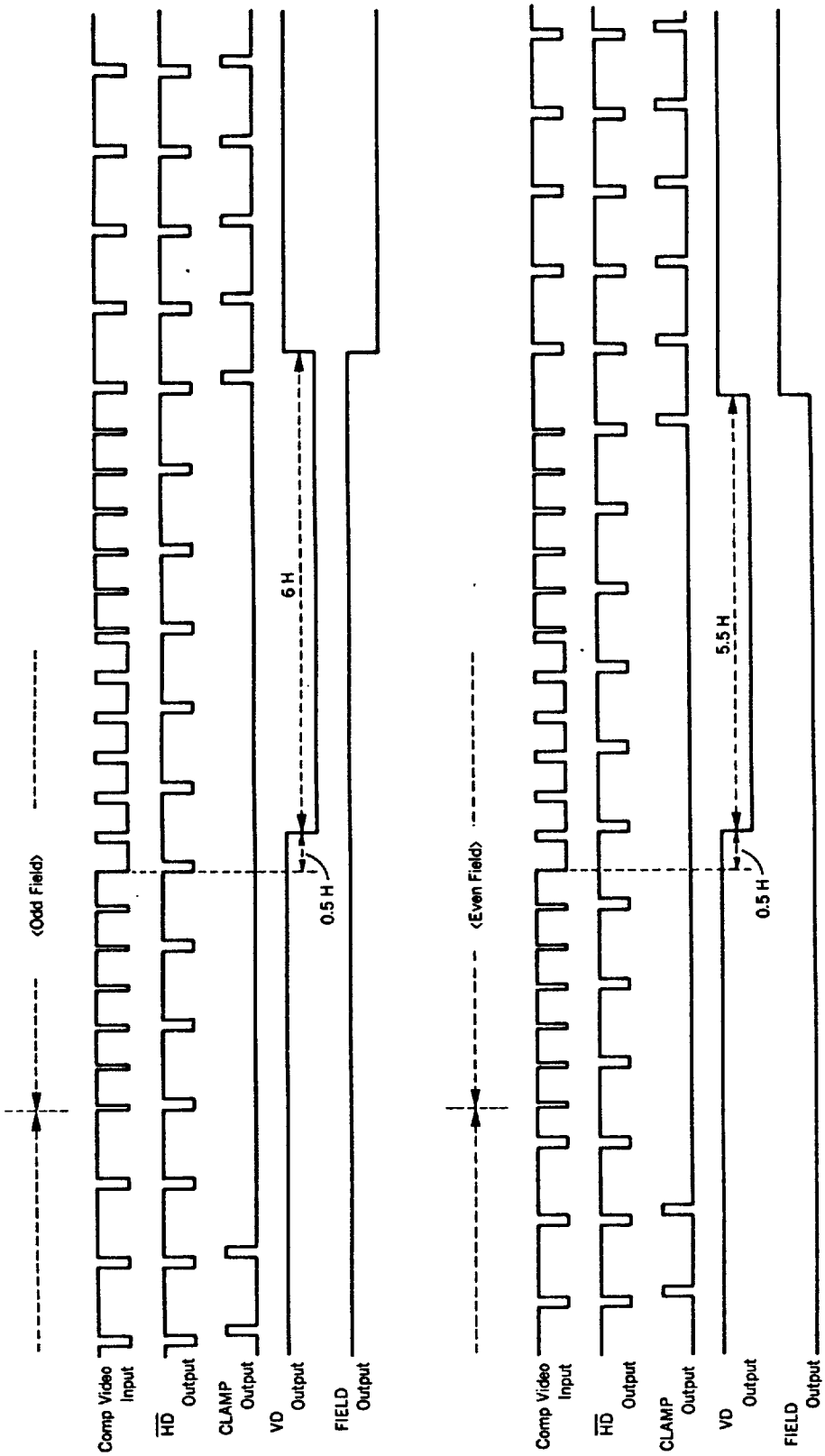
No.	PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
21	HD output High level (1)	E_{HDH1}	2.7	3.5		V	High level of synchronized HD output when only 0.3 V_{p-p} sync signal is input to Pin 36 I_{OH} = −400 μA
22	HD output High level (2)	E_{HDH2}	3.5	4.0		V	High level of synchronized HD output when only 0.3 V_{p-p} sync signal is input to Pin 36 I_{OH} = −20 μA
23	HD output Low level	E_{HDL}		0.2	0.4	V	Low level of synchronized HD output when only 0.3 V_{p-p} sync signal is input to Pin 36 I_{OL} = +2 mA
24	$\overline{HD}$ output High level (1)	E_{HDH1}	2.7	3.5		V	High level of synchronized $\overline{HD}$ output when only 0.3 V_{p-p} sync signal is input to Pin 36 I_{OH} = −400 μA
25	$\overline{HD}$ output High level (2)	E_{HDH2}	3.5	4.0		V	High level of synchronized $\overline{HD}$ output when only 0.3 V_{p-p} sync signal is input to Pin 36 I_{OH} = −20 μA
26	$\overline{HD}$ output Low level	E_{HDL}		0.2	0.4	V	Low level of synchronized $\overline{HD}$ output when only 0.3 V_{p-p} sync signal is input to Pin 36 I_{OL} = +2 mA
27	VD output High level (1)	E_{VDH1}	2.7	3.5		V	High level of synchronized VD output when only 0.3 V_{p-p} sync signal is input to Pin 36 I_{OH} = −400 μA
28	VD output High level (2)	E_{VDH2}	3.5	4.0		V	High level of synchronized VD output when only 0.3 V_{p-p} sync signal is input to Pin 36 I_{OH} = −20 μA
29	HD output Low level	E_{VDL}		0.2	0.4	V	Low level of synchronized HD output when only 0.3 V_{p-p} sync signal is input to Pin 36 I_{OL} = +2 mA
30	Clamp output High level (1)	E_{CLPH1}	2.7	3.5		V	High level of synchronized Clamp output when only 0.3 V_{p-p} sync signal is input to Pin 36 I_{OH} = −400 μA
31	Clamp output High level (2)	E_{CLPH2}	3.5	4.0		V	High level of synchronized Clamp output when only 0.3 V_{p-p} sync signal is input to Pin 36 I_{OH} = −20 μA
32	Clamp output Low level	E_{CLPL}		0.2	0.4	V	Low level of synchronized Clamp output when only 0.3 V_{p-p} sync signal is input to Pin 36 I_{OL} = +2 mA
33	Field ident. output High level (1)	E_{FSH1}	2.7	3.5		V	High level of synchronized Field ident. output when only 0.3 V_{p-p} sync signal is input to Pin 36 I_{OH} = −400 μA
34	Field ident. output High level (2)	E_{FSH2}	3.5	4.0		V	High level of synchronized Field ident. output when only 0.3 V_{p-p} sync signal is input to Pin 36 I_{OH} = −20 μA
35	Field ident. Low level	E_{FSL}		0.2	0.4	V	Low level of synchronized Field ident. output when only 0.3 V_{p-p} sync signal is input to Pin 36 I_{OL} = +2 mA
36	H detection output High level (1)	E_{HKH1}	2.7	3.5		V	High level of asynchronized H detect output without H sync input I_{OH} = −400 μA
37	H detection output High level (2)	E_{HKH2}	3.5	4.0		V	High level of asynchronized H detect output without H sync input I_{OH} = −20 μA
38	H detection output Low level	E_{HKL}		0.2	0.4	V	Low level of synchronized H detect output when only 0.3 V_{p-p} sync signal is input to Pin 36 I_{OL} = +2 mA

No.	PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
39	H sync lock-in range	f_{HP}	+400	+500		Hz	Frequency range that can be pulled when only 0.3 V_{p-p} sync signal is input to Pin 36 and H sync frequency is varied (f_H conversion)
40	Horizontal VCO control sensitivity	β_H		+1.1		Hz/mV	Rate of variation of frequency when AFC filter pin is changed from 3.0 V to 3.4 V without H sync input (f_H conversion)
41	Horizontal VCO free-run frequency	f_{HO}	−50	0	+50	Hz	Frequency difference of HD output from f_H when H sync input is not applied
42	Pulse width of HD output	P_{WHD}	3.8	4.0	4.2	μs	Pulse width of synchronized HD output when only 0.3 V_{p-p} sync signal is input to Pin 36
43	Pulse width of $\overline{HD}$ output	P_{WHD}	3.8	4.0	4.2	μs	Pulse width of synchronized $\overline{HD}$ output when only 0.3 V_{p-p} sync signal is input to Pin 36
44	Pulse width of VD output	P_{WVD1}		6.0		H	Pulse width of synchronized VD output when only 0.3 V_{p-p} sync signal is input to Pin 36 — ODD
		P_{WVD2}		5.5		H	EVEN
45	Pulse width of Clamp output	P_{WCLP}	3.2	3.4	3.6	μs	Pulse width of synchronized Clamp output when only 0.3 V_{p-p} sync signal is input to Pin 36
46	Oscillation start voltage of horizontal VCO	V_{ST}			4.2	V	Output voltage at HD ($\overline{HD}$) when V_{CC} is gradually increased from 0 V without H sync input
47	H killer output Low level	E_{HKL}			0.4	V	Low level of synchronized H killer output when only 0.3 V_{p-p} sync signal is input to Pin 36 Change value of Chroma output
48	V free-run frequency 1	$f_{V1(50)}$		$f_H/352$		Hz	Frequency ratio of HD output to VD output H sync input: No signal; TV mode; V sync input: V_{CC}
		$f_{V1(60)}$		$f_H/288$		Hz	
49	V free-run frequency 2	$f_{V2(50)}$		$f_H/288$		Hz	Same as f_{V1} with the following exception: V sync input: GND
		$f_{V2(60)}$		$f_H/240$		Hz	
50	V free-run frequency 3	$f_{V3(50)}$		$f_H/368$		Hz	Same as f_{V1} with the following exception: VTR mode
		$f_{V3(60)}$		$f_H/296$		Hz	
51	V free-run frequency 4	$f_{V4(50)}$		$f_H/272$		Hz	Same as f_{V1} with the following exceptions: VTR mode V sync input: GND
		$f_{V4(60)}$		$f_H/232$		Hz	

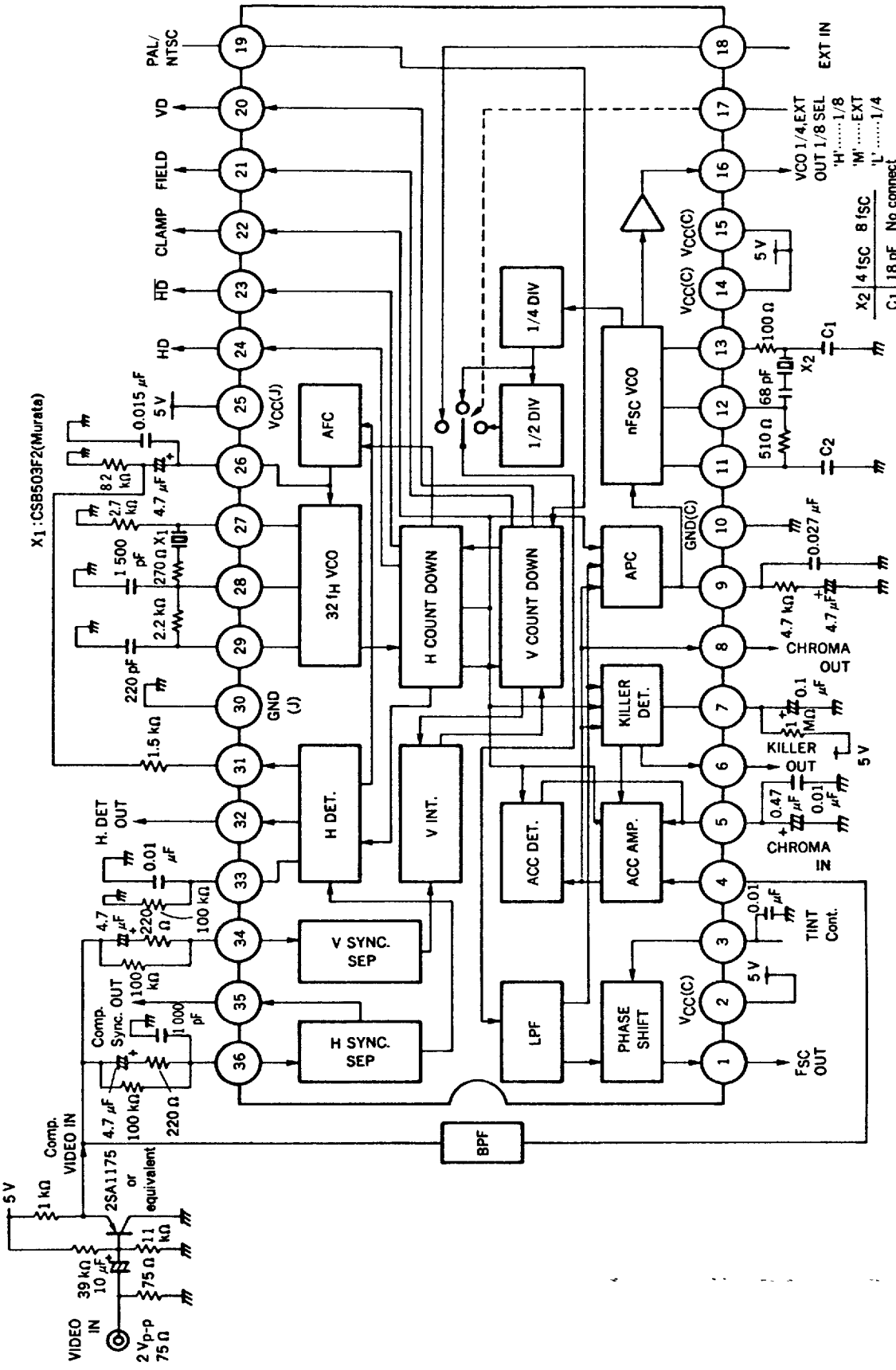
TIMING CHARTS (Horizontal Period)



TIMING CHARTS (Vertical Period)



APPLICATION CIRCUIT

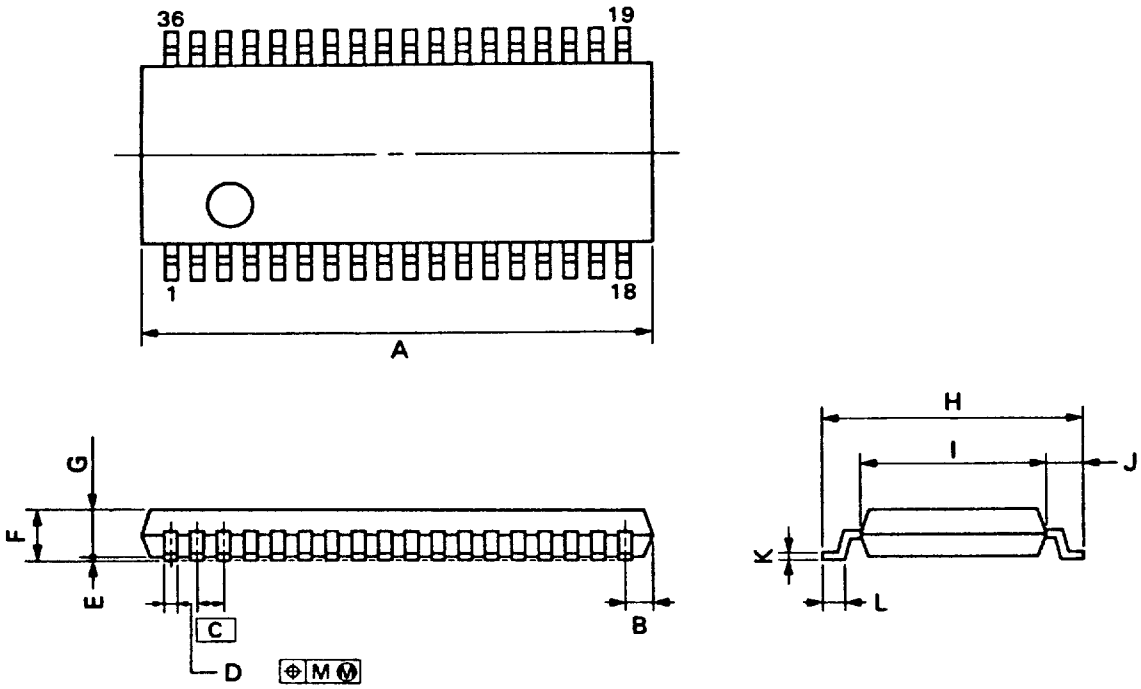


The application circuits and circuit constants in this manual are examples and not apply to full-production design.

Note : Pin 4 must keep a low impedance.

PACKAGE DIMENSIONS

36-pin Plastic Shrink SOP (300 mil)



P36GM-80-300B-1

ITEM	MILLIMETERS	INCHES
A	15.54 MAX.	0.612 MAX.
B	0.97 MAX.	0.039 MAX.
C	0.8 (T.P.)	0.031 (T.P.)
D	$0.35^{+0.10}_{-0.05}$	$0.014^{+0.004}_{-0.003}$
E	0.1 ± 0.1	0.004 ± 0.004
F	1.8 MAX.	0.071MAX.
G	1.55	0.061
H	7.7 ± 0.3	0.303 ± 0.012
I	5.6	0.220
J	1.1	0.043
K	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$
L	0.6 ± 0.2	$0.024^{+0.008}_{-0.009}$
M	0.10	0.004

NOTE

Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.