MC100EL90

-3.3V / -5V Triple ECL Input to PECL Output Translator

The MC100EL90 is a triple ECL to PECL translator. The device receives either –3.3 V or –5 V differential ECL signals, determined by the V_{EE} supply level, and translates them to standard +5 V differential PECL output signals.

To accomplish the level translation, the EL90 requires three power rails. The V_{CC} supply should be connected to the positive supply, and the V_{EE} pin should be connected to the negative power supply. The GND pins, as expected, are connected to the system ground plane. Both V_{EE} and V_{CC} should be bypassed to ground via 0.01 μF capacitors.

Under open input conditions, the $\overline{D}$ input will be biased at $V_{EE}/2$ and the D input will be pulled to V_{EE}. This condition will force the Q output to a LOW, ensuring stability.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

- 500 ps Propagation Delays
- ESD Protection: >2 KV HBM, >200 V MM
- The 100 Series Contains Temperature Compensation
- Operating Range: V_{CC}= 4.75 V to 5.25 V; V_{EE}= –3.0 V to –5.5 V; GND= 0 V
- Internal Input Pulldown Resistors
- Q Output will Default LOW with Inputs Open or at V_{EE}
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 261 devices

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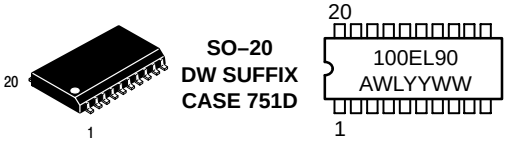
MARKING DIAGRAM*



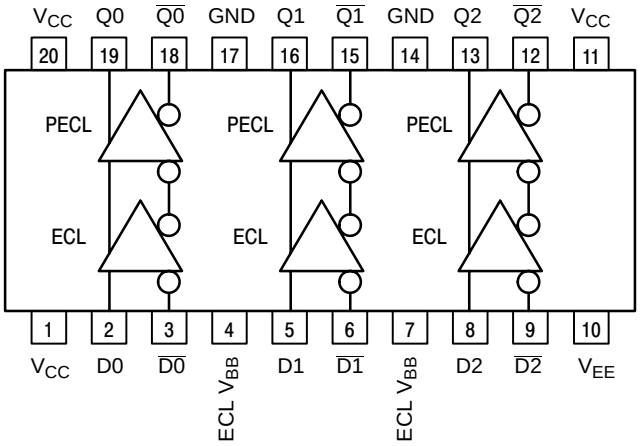
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC100EL90DW	SO–20	38 Units/Rail
MC100EL90DWR2	SO–20	1000 Units/Reel

Logic Diagram and Pinout: 20-Lead SOIC (Top View)



* All V_{CC} pins are tied together on the die.

Warning: All V_{CC}, V_{EE}, and GND pins must be externally connected to Power Supply to guarantee proper operation.

PIN DESCRIPTION

PIN	FUNCTION
Dn, $\overline{Dn}$	ECL Inputs
Qn, $\overline{Qn}$	PECL Outputs
ECL V_{BB}	ECL Reference Voltage Output
V_{CC}	Positive Supply
V_{EE}	Negative Supply
GND	Ground

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Power Supply	GND = 0 V		8 to 0	V
V_{EE}	NECL Power Supply	GND = 0 V		–8 to 0	V
V_I	NECL Input Voltage	GND = 0 V	$V_I \geq V_{EE}$	–6 to 0	V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	ECL V_{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	20 SOIC 20 SOIC	90 60	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	20 SOIC	30 to 35	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

NECL INPUT DC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= –5.0 V; GND= 0 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	V_{EE} Power Supply Current			8.0		6.0	8.0			8.0	mA
V_{IH}	Input HIGH Voltage (Single Ended)	–1165		–880	–1165		–880	–1165		–880	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1810		–1475	–1810		–1475	–1810		–1475	mV
ECL V_{BB}	Output Voltage Reference	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 2.) Vpp < 500 mV Vpp ≧ 500 mV	 V_{EE}+1.3 VEE+1.5		 –0.4 –0.4	 V_{EE}+1.2 VEE+1.4		 –0.4 –0.4	 V_{EE}+1.2 VEE+1.4		 –0.4 –0.4	 V V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5		——	0.5		——	0.5		——	μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input parameters vary 1:1 with GND. V_{EE} can vary –3.0 V / –5.5 V.
2. V_{IHCMR} min varies 1:1 with V_{EE}. V_{IHCMR} max varies 1:1 with GND.

PECL OUTPUT DC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= –5.0 V; GND= 0 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{CC}	V_{CC} Power Supply Current			24		20	24			26	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3915	3995	4120	3975	4045	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3170	3305	3445	3190	3295	3380	3190	3295	3380	mV

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Output parameters vary 1:1 with V_{CC}. V_{CC} can vary ± 0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

AC CHARACTERISTICS V_{CC}= 4.5 V to 5.5 V; V_{EE}= –3.0 V to –5.5 V; GND= 0 V

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency		560			650			700		MHz
t_{PLH} t_{PHL}	Propagation Delay Differential D to Q S.E.	390 340		590 640	420 370		620 670	460 410		660 710	ps
t_{SKEW}	Skew Output–to–Output (Note 1) Part–to–Part (Differential) (Note 1) Duty Cycle (Differential) (Note 2)		20 25	100 200		20 25	100 200		20 25	100 200	ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}	Input Swing (Note 3)	150		1000	150		1000	150		1000	mV
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	230		500	230		500	230		500	ps

1. Skews are valid across specified voltage range, part–to–part skew is for a given temperature.
2. Duty cycle skew is the difference between a TPLH and TPHL propagation delay through a device.
3. V_{PP}(min) is the minimum input swing for which AC parameters are guaranteed. The device has a DC gain of ≈40.

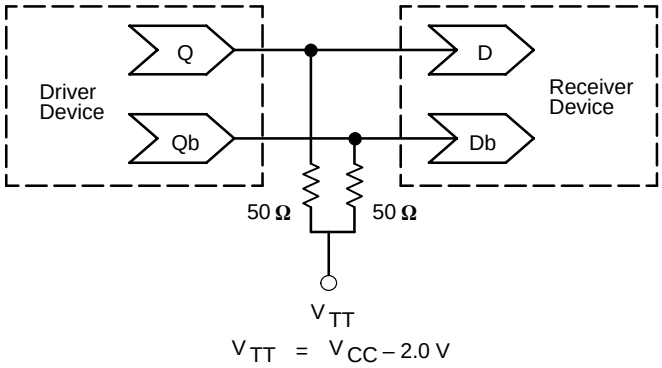


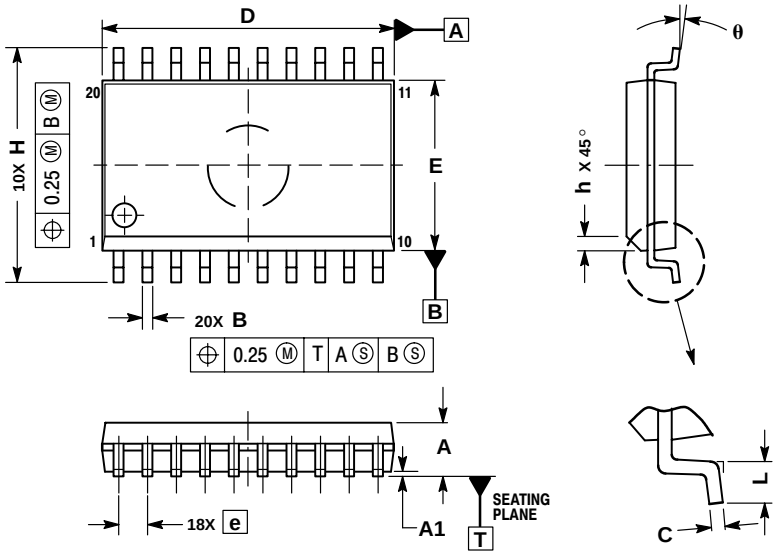
Figure 1. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1560	–	Low Voltage ECLinPS SPICE Modeling Kit
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

PACKAGE DIMENSIONS

SO–20
DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751D–05
ISSUE F



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0 °	7 °

Notes

Notes

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