

Single N-channel MOSFET

ELM13434CA-S

■General description

The ELM13434CA-S uses advanced trench technology to provide excellent RDS(ON) and low gate charge. This device is suitable for use as a load switch or in PWM applications. It is ESD protected.

■Features

- V_{DS}=30V
- I_D=4.2A (V_GS=10V)
- R_{DS(on)} < 52mΩ (V_GS=10V)
- R_{DS(on)} < 75mΩ (V_GS=4.5V)
- ESD protected

■Maximum absolute ratings

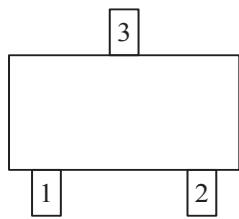
Parameter	Symbol	Limit		Unit	Note
		10sec	Steady-state		
Drain-source voltage	V _{DS}	30		V	
Gate-source voltage	V _G S	±20		V	
Continuous drain current	T _A =25°C	Id	4.2	3.5	A
	T _A =70°C		3.3	2.8	
Pulsed drain current	I _{DM}	30		A	2
Power dissipation	T _A =25°C	P _D	1.40	1.00	W
	T _A =70°C		0.90	0.64	
Junction and storage temperature range	T _J , T _{STG}	-55 to 150		°C	

■Thermal characteristics

Parameter		Symbol	Typ.	Max.	Unit	Note
Maximum junction-to-ambient	t≤10s	R _{θJA}	70	90	°C/W	1
Maximum junction-to-ambient	Steady-state		100	125	°C/W	
Maximum junction-to-lead	Steady-state	R _{θJL}	63	80	°C/W	3

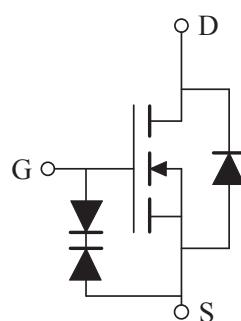
■Pin configuration

SOT-23(TOP VIEW)



Pin No.	Pin name
1	GATE
2	SOURCE
3	DRAIN

■Circuit



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■Electrical characteristics

T_a=25°C

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	
STATIC PARAMETERS								
Drain-source breakdown voltage	BV _{dss}	Id=250μA, V _{gs} =0V		30			V	
Zero gate voltage drain current	Id _{ss}	V _{ds} =30V, V _{gs} =0V	T _j =55°C		1		μA	
					5			
Gate-body leakage current	I _{gss}	V _{ds} =0V, V _{gs} =±16V				10	μA	
Gate threshold voltage	V _{gs(th)}	V _{ds} =V _{gs} , Id=250μA		1.00	1.32	1.80	V	
On state drain current	Id(on)	V _{gs} =10V, V _{ds} =5V		30			A	
Static drain-source on-resistance	R _{ds(on)}	V _{gs} =10V, Id=4.2A	T _j =125°C		43	52	mΩ	
					58	74		
		V _{gs} =4.5V, Id=2A			59	75	mΩ	
Forward transconductance	G _{fs}	V _{ds} =5V, Id=4.2A			8.5		S	
Diode forward voltage	V _{sd}	Is=1A, V _{gs} =0V			0.77	1.00	V	
Max. body-diode continuous current	I _s					1.8	A	
DYNAMIC PARAMETERS								
Input capacitance	C _{iss}	V _{gs} =0V, V _{ds} =15V, f=1MHz			269	340	pF	
Output capacitance	C _{oss}				65		pF	
Reverse transfer capacitance	C _{rss}				41		pF	
Gate resistance	R _g	V _{gs} =0V, V _{ds} =0V, f=1MHz			1.0	1.5	Ω	
SWITCHING PARAMETERS								
Total gate charge (10V)	Q _g	V _{gs} =10V, V _{ds} =15V, Id=4.2A			5.70	7.20	nC	
Total gate charge (4.5V)	Q _g				3.00		nC	
Gate-source charge	Q _{gs}				1.37		nC	
Gate-drain charge	Q _{gd}				0.65		nC	
Turn-on delay time	t _{d(on)}	V _{gs} =10V, V _{ds} =15V R _l =3.6Ω, R _{gen} =3Ω			2.6	3.8	ns	
Turn-on rise time	t _r				5.5	8.0	ns	
Turn-off delay time	t _{d(off)}				15.2	23.0	ns	
Turn-off fall time	t _f				3.7	5.5	ns	
Body diode reverse recovery time	t _{rr}	I _f =4.2A, dI/dt=100A/μs			15.5	21.0	ns	
Body diode reverse recovery charge	Q _{rr}	I _f =4.2A, dI/dt=100A/μs			7.1		nC	

NOTE :

1. The value of R_{θja} is measured with the device mounted on 1in² FR-4 board of 2oz. Copper, in still air environment with T_a=25°C. The value in any given applications depends on the user's specific board design, The current rating is based on the t≤10s thermal resistance rating.
2. Repetitive rating, pulse width limited by junction temperature.
3. The R_{θja} is the sum of the thermal impedance from junction to lead R_{θjl} and lead to ambient.
4. The static characteristics in Figures 1 to 6 are obtained using 80μs pulses, duty cycle 0.5%max.
5. These tests are performed with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_a=25°C. The SOA curve provides a single pulse rating.
6. The current rating is based on the t≤10s thermal resistance rating.



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■Typical electrical and thermal characteristics

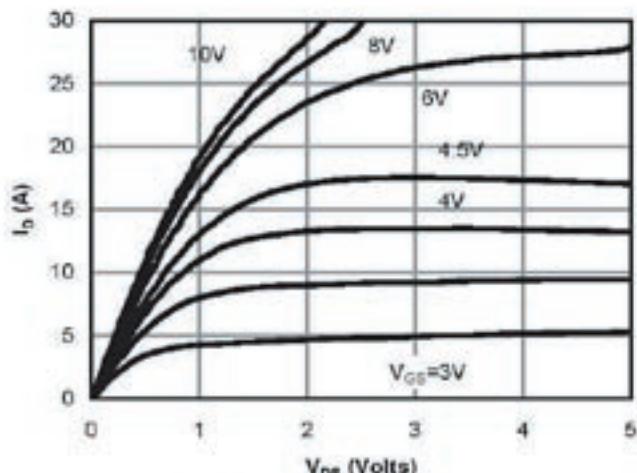


Fig 1: On-Region Characteristics

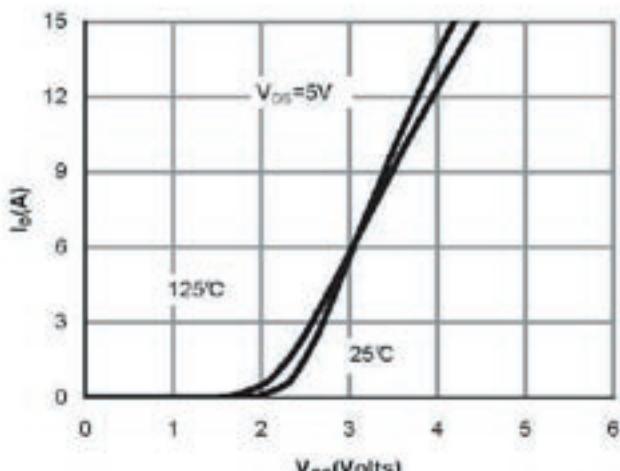


Figure 2: Transfer Characteristics

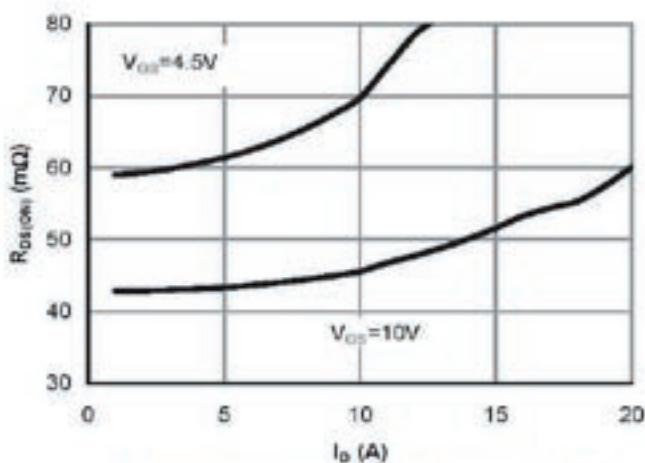


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

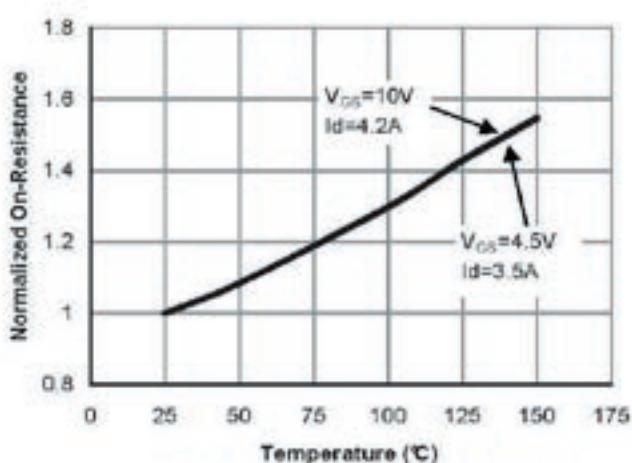


Figure 4: On-Resistance vs. Junction Temperature

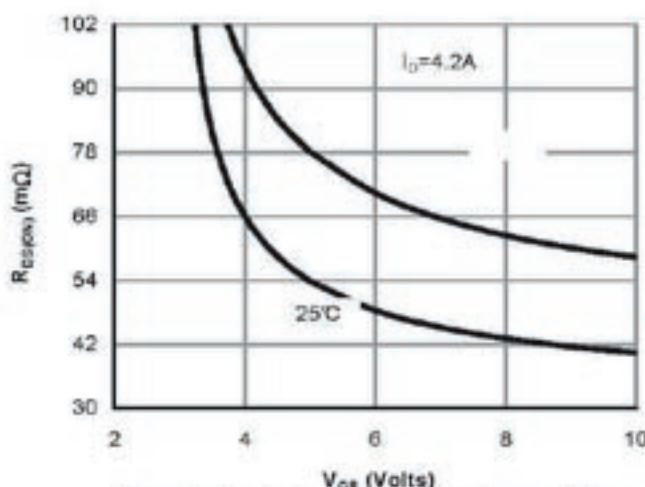


Figure 5: On-Resistance vs. Gate-Source Voltage

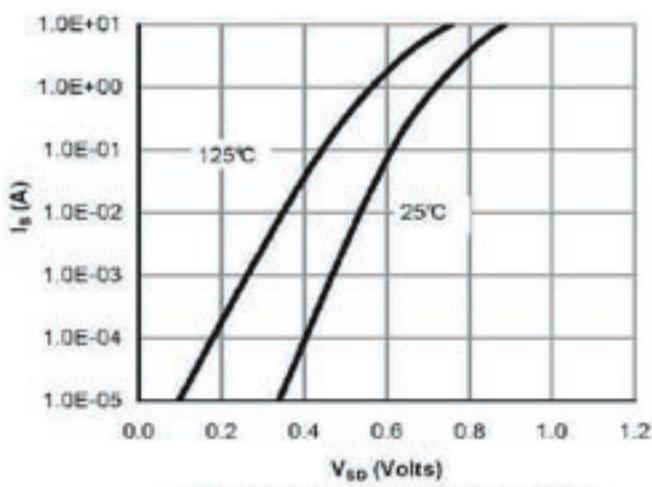


Figure 6: Body-Diode Characteristics

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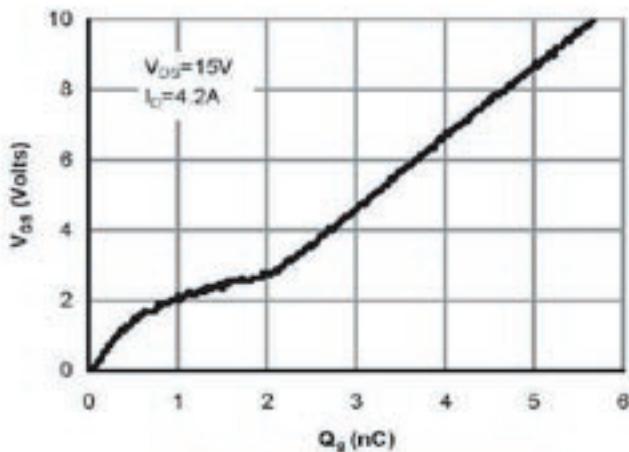


Figure 7: Gate-Charge Characteristics

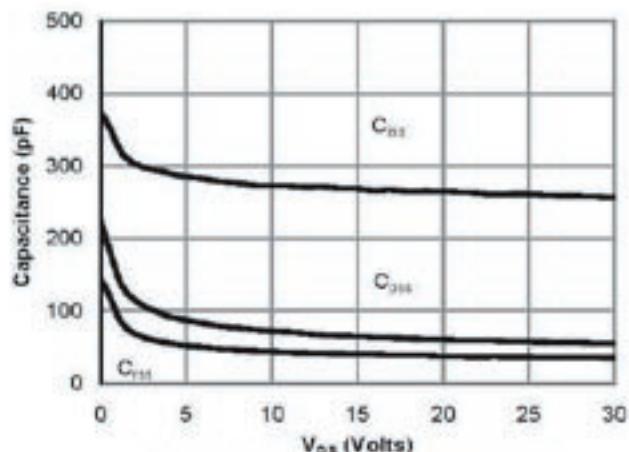


Figure 8: Capacitance Characteristics

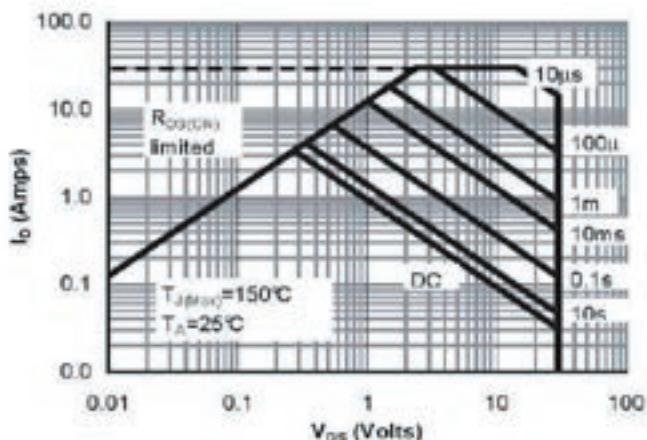


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

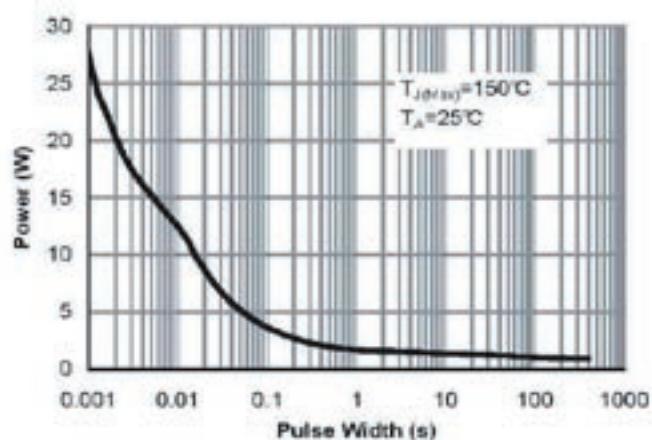


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

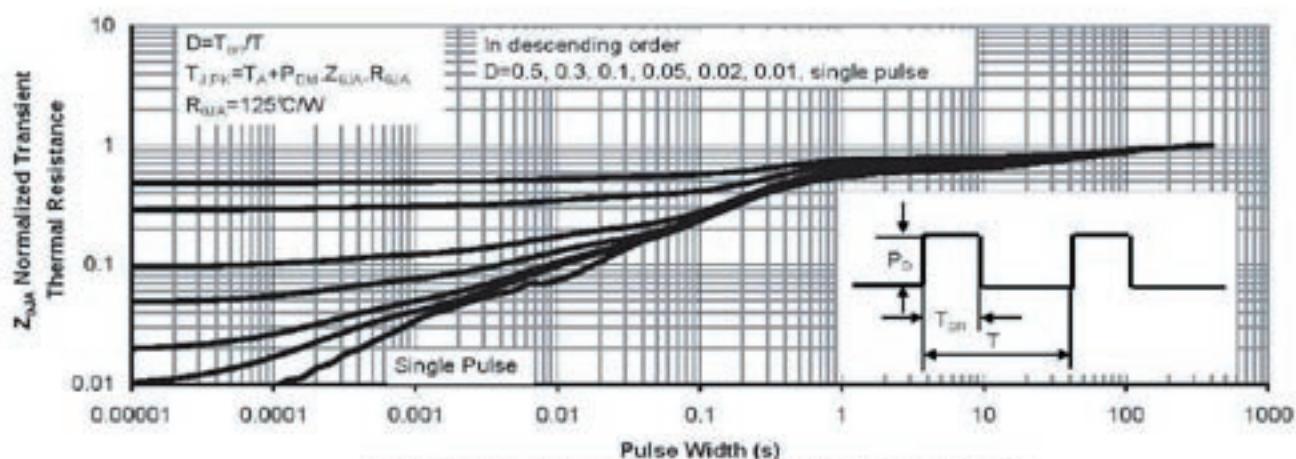


Figure 11: Normalized Maximum Transient Thermal Impedance