

CCD Vertical Clock Driver

Description

The CXD1267N is a vertical clock driver for CCD image sensors. This IC is the successor of the CXD1250N with attractive features.

Features

- 1) Substrate voltage (V_{sub}) generator is built-in.
 - Variable V_{sub} in the range of 4.0V to 18.5V.
 - Reduction of peripheral parts saves space.
- 2) Only two power supplies (+15V and -8.5V) are needed.
 - V_{DD} (5V) and V_{HH} (20V) are eliminated.
- 3) 3.3V clock interface is acceptable.
- 4) 20-pin VSOP package is used.

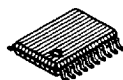
Absolute Maximum Ratings ($T_a=25^\circ\text{C}$)

• Supply voltage	V_L	0 to -10	V
• Supply voltage	V_H	$V_L-0.3$ to $2V_L+35$	V
• Supply voltage	V_M	$V_L-0.3$ to 3.0	V
• Input voltage	V_I	$V_L-0.3$ to $V_H+0.3$	V
• Output voltage (V_2, V_4)	$MV\phi$	$V_L-0.3$ to $V_M+0.3$	V
• Output voltage (V_1, V_3)	$HV\phi$	$V_L-0.3$ to $V_H+0.3$	V
• Output voltage (V_{SHT})	$HHV\phi$	$V_L-0.3$ to $V_H+0.3$	V
• Operational amplifier output current	I_{OUT}	± 5	mA
• Operating temperature	T_{opr}	-25 to +85	$^\circ\text{C}$
• Storage temperature	T_{stg}	-40 to +125	$^\circ\text{C}$

Recommended Operating Conditions

• Supply voltage	V_H	14.5 to 15.5	V
• Supply voltage	V_M	0	V
• Supply voltage	V_L	-7.5 to -9.0	V
• Input voltage (except for pin 3)	V_I	0 to 6.0	V
• Operational amplifier input voltage	V_{IOP}	1.0 to 4.5	V
• Operating temperature	T_{opr}	-20 to +75	$^\circ\text{C}$

20 pin VSOP (Plastic)



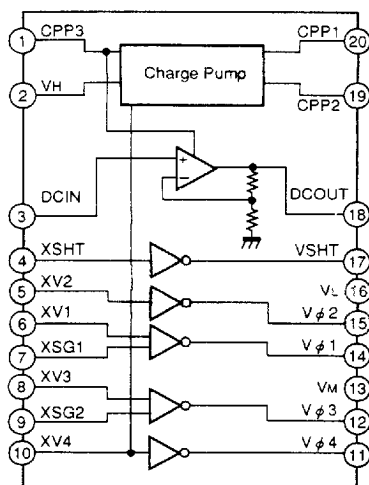
Applications

CCD cameras

Structure

CMOS

Block Diagram and Pin Configuration (Top View)



Pin Description

Pin No.	Symbol	I/O	Description
1	CPP3	O	Charge pump
2	VH	—	Power supply (15V)
3	DCIN	I	Operational amplifier input
4	XSHT	I	Output control (VSHT)
5	XV2	I	Output control (V ϕ 2)
6	XV1	I	Output control (V ϕ 1)
7	XSG1	I	Output control (V ϕ 1)
8	XV3	I	Output control (V ϕ 3)
9	XSG2	I	Output control (V ϕ 3)
10	XV4	I	Output control (V ϕ 4)
11	V ϕ 4	O	High-voltage output (2 levels: VM, VL)
12	V ϕ 3	O	High-voltage output (3 levels: VH, VM, VL)
13	VM	—	GND
14	V ϕ 1	O	High-voltage output (3 levels: VH, VM, VL)
15	V ϕ 2	O	High-voltage output (2 levels: VM, VL)
16	VL	—	Power supply (−8.5 V)
17	VSHT	O	High-voltage output (2 levels: VH, VL)
18	DCOUT	O	Operational amplifier output
19	CPP2	—	Charge pump
20	CPP1	—	Charge pump

Truth Table

Input				Output		
XV1, 3	XSG1, 2	XV2, 4	XSHT	V ϕ 1, 3	V ϕ 2, 4	VSHT
L	L	X	X	V _H	X	X
H	L	X	X	Z	X	X
L	H	X	X	V _M	X	X
H	H	X	X	V _L	X	X
X	X	L	X	X	V _M	X
X	X	H	X	X	V _L	X
X	X	X	L	X	X	V _H
X	X	X	H	X	X	V _L

X: Don't care
Z: High impedance

Electrical Characteristics

DC Characteristics

(Unless otherwise specified, Ta=25°C, V_H=15V, V_M=GND, V_L=-8.5V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
High level input voltage	V _{IH}		2.3	—	—	V
Low level input voltage	V _{IL}		—	—	1.3	V
High level output voltage	V _{OH}	I _O =-20 μ A	14.9	15.0	—	V
Middle level output voltage	V _{OM1}	I _O =20 μ A	—	0.0	0.1	V
Middle level output voltage	V _{OM2}	I _O =-20 μ A	-0.1	0.0	—	V
Low level output voltage	V _{OL}	I _O =20 μ A	—	-8.5	-8.4	V
Charge pump output voltage	V _{CP3}	-1 $\leq$ I _{CP3} $\leq$ 0mA I _{OUT} =0mA, Ta=-20 to 75°C V _{IOP} =4.5V	20	—	—	V
Input current	I _I	V _I =V _L to 5V	-1.0	0.0	1.0	μ A
Operating supply current	I _H	*1	—	2.0	3.5	mA
Operating supply current	I _M	*1	—	4.5	5.0	mA
Operating supply current	I _L	*1	-8.5	-6.5	—	mA
Output current	I _{OL}	V ϕ 1 to 4=-8.0V	25	—	—	mA
Output current	I _{OM1}	V ϕ 1 to 4=-0.5V	—	—	-10	mA
Output current	I _{OM2}	V ϕ 1, 3=0.5V	9	—	—	mA
Output current	I _{OH}	V ϕ 1, 3=14.5V	—	—	-12	mA
Output current	I _{OSL}	VSHT=-8.0V	12	—	—	mA
Output current	I _{OSH}	VSHT=14.5V	—	—	-7	mA
Operational amplifier gain	G	I _{OUT} =-200/+100 μ A	—	$\times 4.40$	—	
Gain error	ΔG	Ta=-20 to 75°C *2 I _{OUT} =-200/+100 μ A V _{IOP} =1.0 to 4.5V	-3	—	-3	%

*1 See Measurement Circuit. Shutter speed: 1/10000.

*2 See Operational Amplifier Gain Characteristic.

Note) Current directions: + indicates the direction flowing to IC; - indicates the direction flowing from IC

Switching Characteristics

(V_H=15V, V_M=GND, V_L=-8.5V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Propagation delay time	TPLM	Load free*1	10	40	70	ns
Propagation delay time	TPMH	Load free*1	10	30	70	ns
Propagation delay time	TPLH	Load free*1	10	40	100	ns
Propagation delay time	TPML	Load free*1	10	100	200	ns
Propagation delay time	TPHM	Load free*1	10	100	180	ns
Propagation delay time	TPHL	Load free*1	10	60	100	ns
Rise time	TTLM	V _L →V _M *1	400	700	930	ns
Rise time	TTMH	V _M →V _H *1	400	650	930	ns
Rise time	TTLH	V _L →V _H *1	10	50	100	ns
Fall time	TTML	V _M →V _L *1	200	300	500	ns
Fall time	TTMH	V _H →V _M *1	400	600	820	ns
Fall time	TTHL	V _H →V _L *1	10	50	100	ns
Charge pump boosting time	Tc	*2	—	—	10	ms
Output noise voltage	VCLH	*3	—	—	0.5	V
Output noise voltage	VCLL	*3	—	—	0.5	V
Output noise voltage	VCMH	*3	—	—	0.5	V
Output noise voltage	VCML	*3	—	—	0.5	V

*1 See Response of Voltage Pulse.

*2 CP1=0.1 μF, CP2=0.1 μF, VCPP3=20V; boosting time after all power supplies rose.

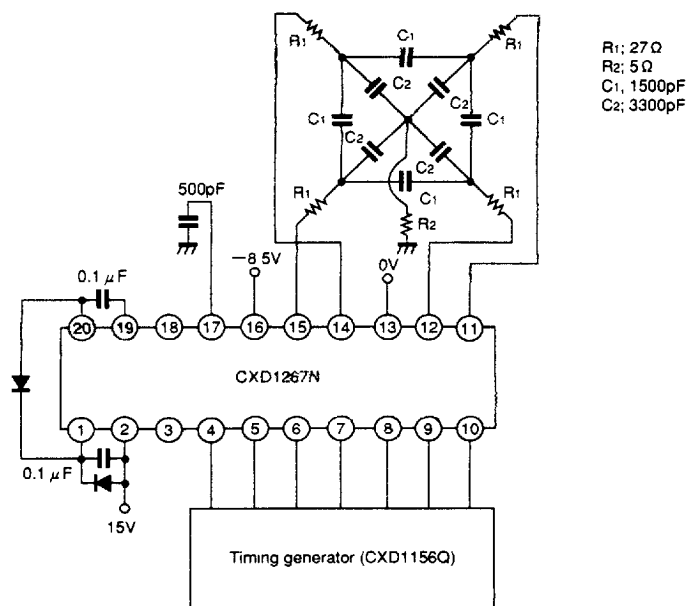
*3 See Noise on a Waveform.

Note) Each item is evaluated by Measurement Circuit.

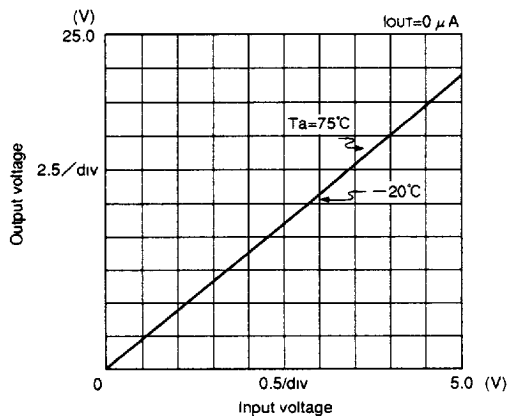
Notes on Operation (See Application Circuit.)

1. Be sure to protect against static electricity because this IC is MOS structure.
2. A bypass capacitor is connected between each power supply (V_H, V_L) and GND.
3. To prevent latch-up, use a capacitor of 0.1 μF (CP1, CP2) for charge pump.
Insert a silicon diode (D2) between CPP3 and CPP1.
4. In order to protect CCD image sensor, pre-clamp is requested prior to clamp by DCOUT.

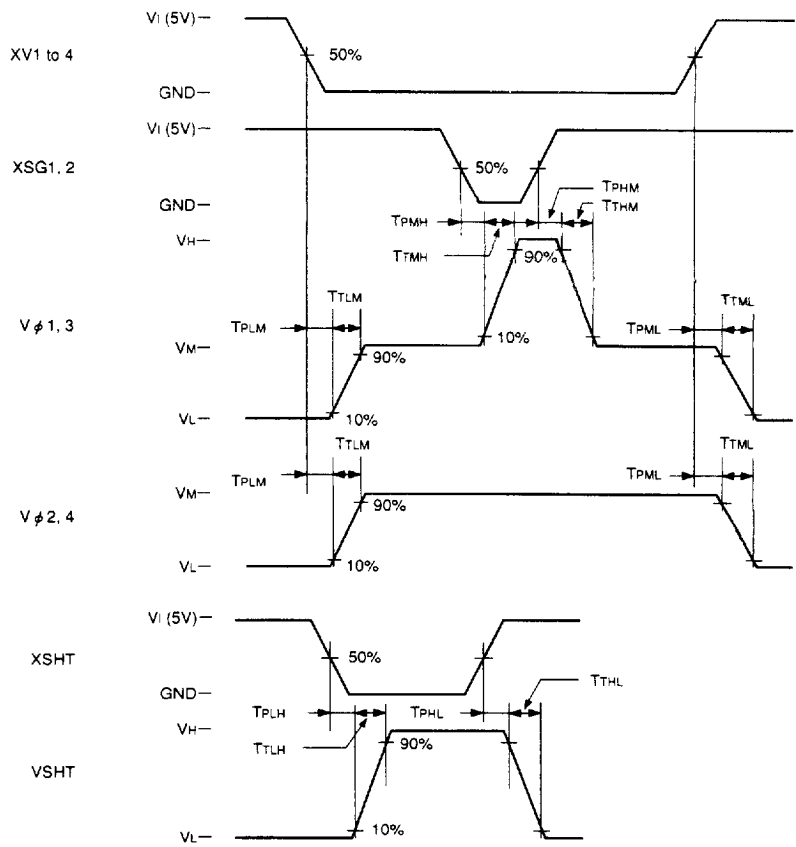
Measurement Circuit



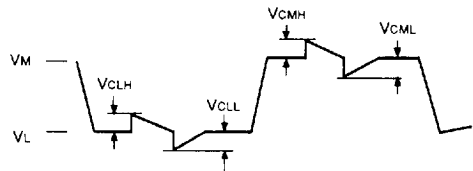
Operational Amplifier Gain Characteristics



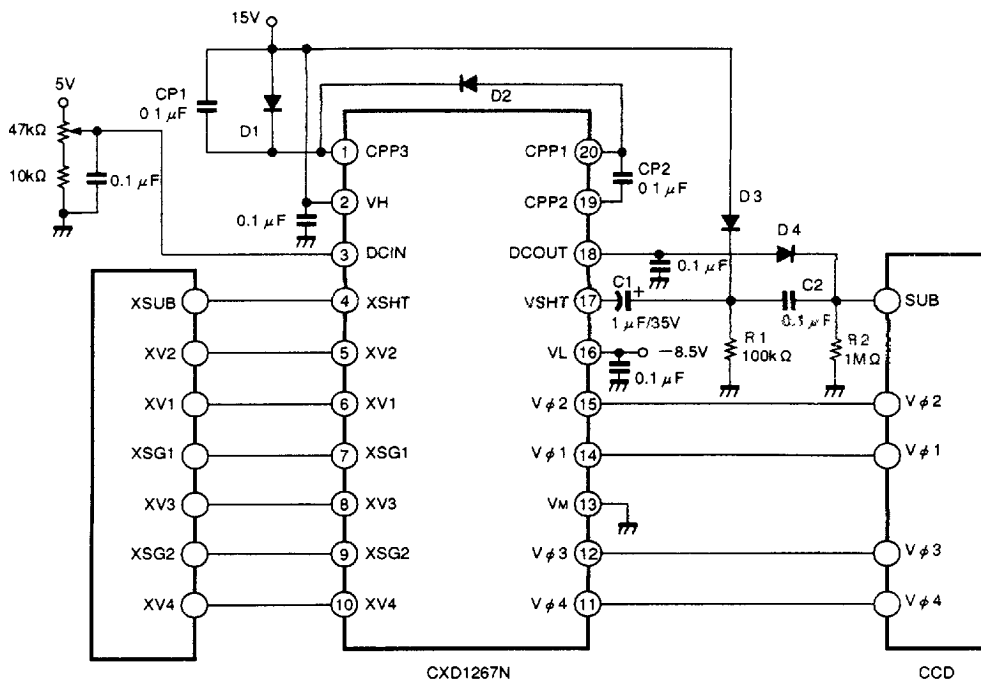
Response of Voltage Pulse



Noise on a Waveform



Application Circuit

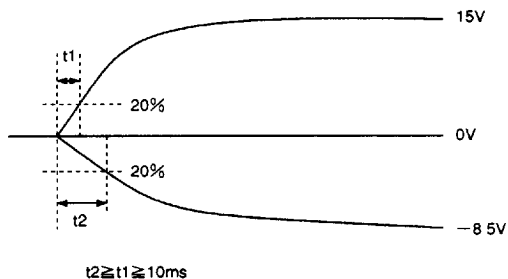


* A peripheral circuit can be simplified by CCD image sensor.

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same

Note with power-on sequence

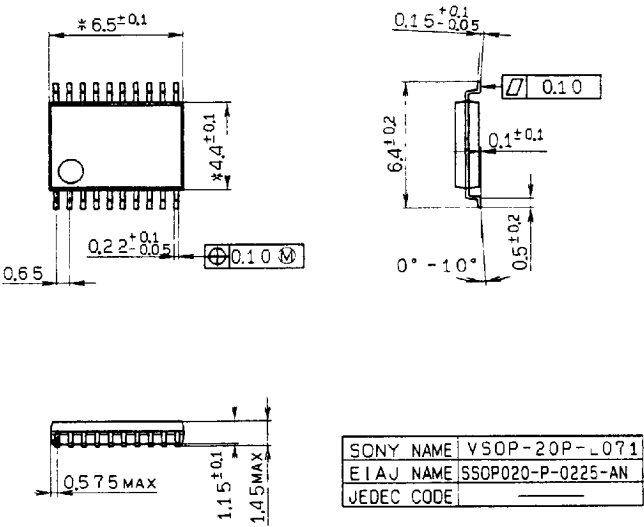
To protect CCD image sensor, rise two power supplies as follows.



Package Outline

Unit: mm

20pin VSOP (Plastic) 225mil 0 086g



Note) Dimensions marked with *
do not include resin residue.