Features

- Lead free versions available
- RoHS compliant (lead free version)*
- New Product Development
- Integrated Passive Device
- ESD Protection to IEC61000-4-2 Spec.

BOURNS®

2FAH-C20R Series - Integrated Passive & Active Device using CSP

General Information

This application specific integrated passive component is designed to provide all of the necessary ESD protection and line resistance required on the data port of a custom portable electronic device. The ESD protection provided by the component enables the data port to withstand ±8 KV Contact / ±15 KV Air Discharge when tested according to the method specified in IEC 61000-4-2. The component incorporates 7 identical channels and is supplied in a 20 pin CSP package which is intended to be mounted directly onto an FR4 printed circuit board. This package will meet typical thermal cycle and bend test specifications without the use of an underfill material.

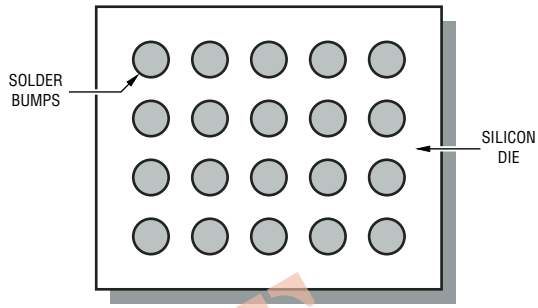


Figure 1 – CSP Format

Electrical & Thermal Characteristics

Electrical Characteristics (T_A = 25 °C unless otherwise noted)	**Symbol**	**Minimum**	**Nominal**	**Maximum**	**Unit**
Zener Diode					
Breakdown Voltage @ 1 mA	V_{BR}	6	7.2	8	V
Leakage Current @ 3 V	I_R			1	µA
ESD Performance (Note 1)					
Withstand					
Contact Discharge		±8			kV
Air Discharge		±15			kV
Let Through (Note 2)					
Contact Discharge				±150	V
Air Discharge				±150	V
Channel Specification					
Resistance	R	90	100	110	Ω
Capacitance @ 1 V & 1 MHz	C	8.5	10.5	12.5	pF
Thermal Characteristics (T_A = 25 °C unless otherwise noted)					
Operating Temperature	T_J	-40	25	+85	°C
Storage Temperature	T_{stg}	-60	25	+125	°C
Total Power Dissipation @ 70 °C	P_D			100	mW

Note: 1. *The IEC 61000-4-2 test method will be adapted for component level testing. The device will provide the specified ESD protection performance on the "IN 1-7" pins only.*
2. *"Let Through" is a measure of the component of an incident ESD transient that the protection device allows through to the down stream circuitry.*

*RoHS Directive 2002/95/EC Jan 27 2003 including Annex

Mechanical Characteristics

This is a Silicon-based device and is packaged using chip scale packaging technology. Solder bumps, formed on the Silicon die, provide the interconnect medium from die to PCB. The bumps are arranged on the die in a regular grid formation. The grid pitch is 0.5mm. The dimensions for the CSP packaged device are shown in Fig. 2 below.

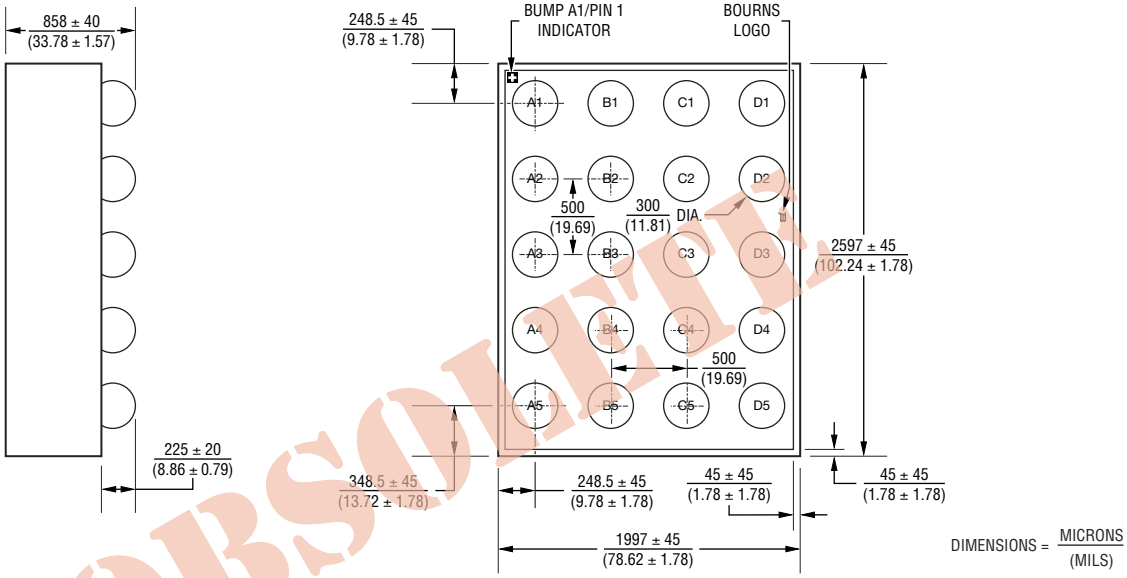


Fig. 2 – Device Mechanical Drawing

Reliability

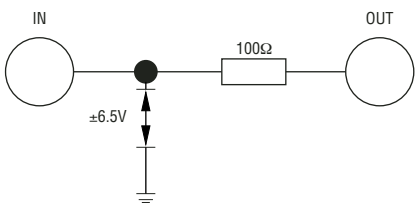
Reliability data exists and continues to be gathered on an ongoing basis for Bourns Integrated Passive and Active Devices using CSP packaging.

"Package level" testing of the integrity of the solder joint is carried out on an independent Daisy-Chain test device. A 25-Pin Daisy Chain component is available from Bourns for this purpose (part number 2TAD-C25R). This is a 5 x 5 array featuring 0.5mm pitch solder bumps. The Distance to Neutral Point (DNP) on that component is larger than that of the 2FAH-C20R and is thus deemed a worse case for Thermal Cycle testing.

"Silicon level" reliability performance will be assured by similarity to other Integrated Passive and Active Devices using CSP product from Bourns.

Individual Channel Schematic

This section contains the schematic (See Fig. 3 below) for the single channel in the integrated passive device. Note that the electrical parameters of primary interest are (a) DC Resistance and (b) ESD performance. In terms of DC parameters it should be noted that all resistor values have a tolerance of ±10 %. This schematic consists of a series 100ohm resistance and Back to Back Zener 6.5 Volt diodes for ESD protection.



Key Design Parameters
DC Channel Resistance: 100 Ω ±10 %
DC Channel Capacitance: 12.5 pF Maximum
V_{BR}: 6 V Min, 8 V Max @ I_{BR} = 1 mA.
I_R: 1 uA Max @ V_R =3 V.

Fig. 3 – Channel Schematic

Block Diagram

Figure 4 contains a block diagram of the CSP device. This diagram includes the pin names and basic electrical connections associated with each channel.

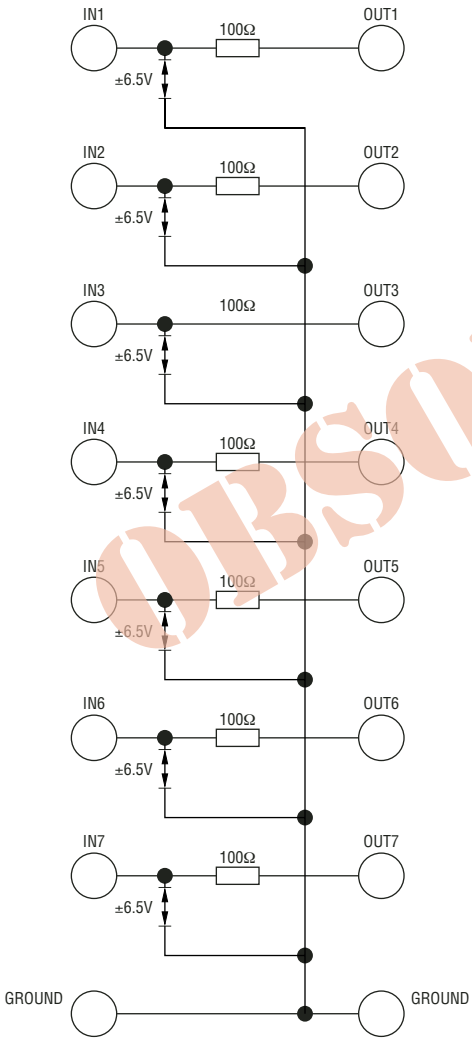


Fig. 4 – Device Block Diagram

Marking

The device will be laser marked on the backside according to the following Fig. 5 scheme below. Position A1, on the Bump Grid is located at the top left of the die when the die is orientated so that the mark is read in the normal fashion.

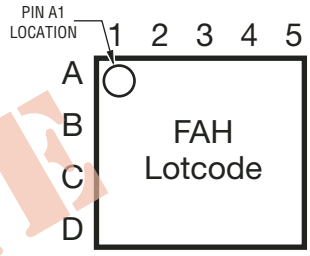


Fig. 5 – Backside Laser Mark

PCB Design and SMT Processing

Please consult Bourns' *Thin Film on Silicon using CSP* Users Guide Application Note for notes on PCB design and SMT processing.

How to Order

2 FAH - C20R __

Thinfilm

Model

Chipscale

No. of Solder Bumps

Packaging Option
R = Tape and Reel
Packaged 3000 pcs. / 7 " reel

Terminations
LF = Sn/Ag/Cu (lead free)
Blank = Sn/Pb

Device Pin Out

The Pin-Out for the device is shown in Fig. 6. Note also that the device is shown with bumps facing up.

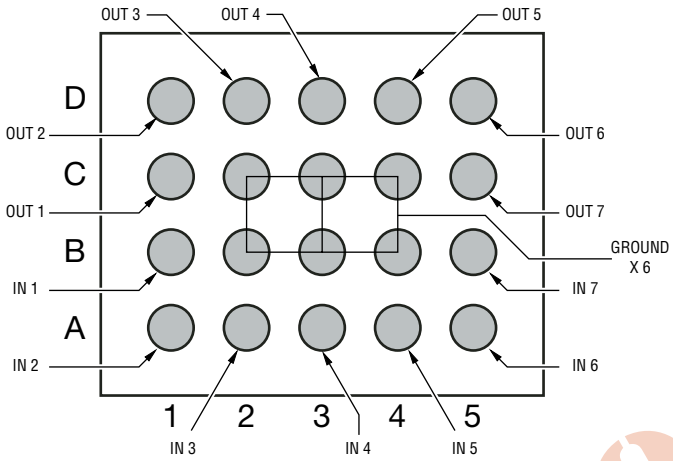


Fig. 6 (a) - Device Pin Out "Bumps Up" View

Function	Pin Out	Function	Pin Out
IN1	B1	OUT4	D3
IN2	A1	OUT5	D4
IN3	A2	OUT6	D5
IN4	A3	OUT7	C5
IN5	A4	Ground	B2
IN6	A5	Ground	B3
IN7	B5	Ground	B4
OUT1	C1	Ground	C2
OUT2	D1	Ground	C3
OUT3	D2	Ground	C4

Fig. 6 (b) - Pin Listings

Packaging

The product will be dispensed in an 8mm x 4mm Tape and Reel format - see Fig. 7 diagram below. The Tape and Reel package will conform to customer specification.

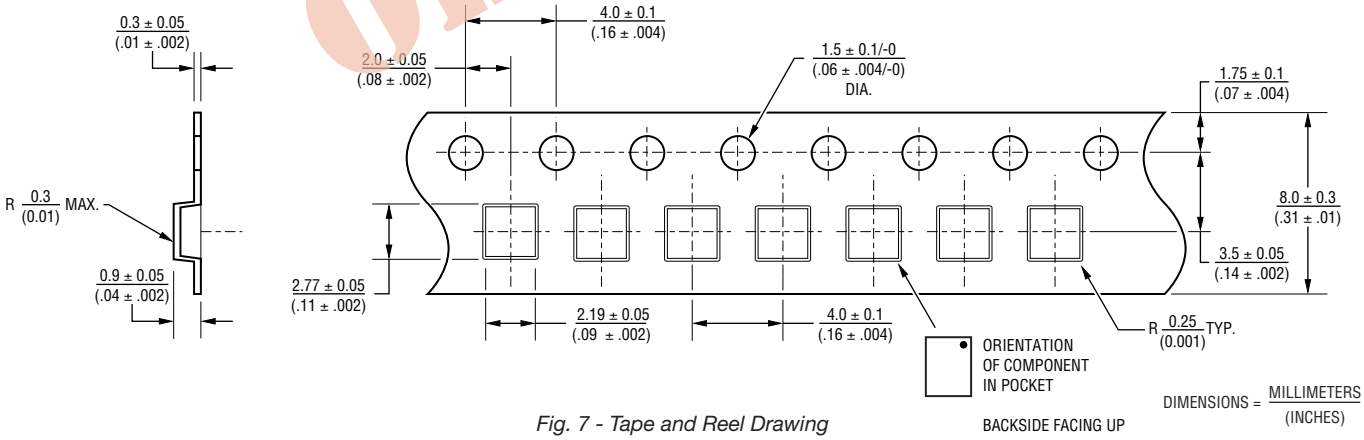


Fig. 7 - Tape and Reel Drawing

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