

# MC74LCX16373

## Low-Voltage CMOS 16-Bit Transparent Latch

### With 5 V-Tolerant Inputs and Outputs (3-State, Non-Inverting)

The MC74LCX16373 is a high performance, non-inverting 16-bit transparent latch operating from a 2.3 to 3.6 V supply. The device is byte controlled. Each byte has separate Output Enable and Latch Enable inputs. These control pins can be tied together for full 16-bit operation. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A  $V_I$  specification of 5.5 V allows MC74LCX16373 inputs to be safely driven from 5 V devices.

The MC74LCX16373 contains 16 D-type latches with 3-state 5 V-tolerant outputs. When the Latch Enable (LEn) inputs are HIGH, data on the Dn inputs enters the latches. In this condition, the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The 3-state outputs are controlled by the Output Enable (OEn) inputs. When OE is LOW, the outputs are enabled. When OE is HIGH, the standard outputs are in the high impedance state, but this does not interfere with new data entering into the latches.

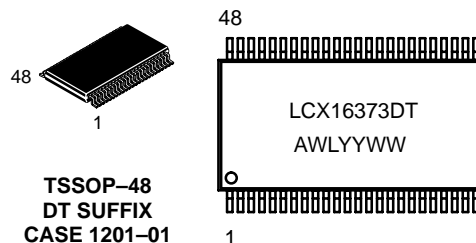
- Designed for 2.3 to 3.6 V  $V_{CC}$  Operation
- 5.4 ns Maximum  $t_{pd}$
- 5 V Tolerant — Interface Capability With 5 V TTL Logic
- Supports Live Insertion and Withdrawal
- I<sub>OFF</sub> Specification Guarantees High Impedance When  $V_{CC} = 0$  V
- LVTTL Compatible
- LVCMOS Compatible
- 24 mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (20  $\mu$ A) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500 mA
- ESD Performance: Human Body Model >2000 V; Machine Model >200 V



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#### MARKING DIAGRAM



TSSOP-48  
DT SUFFIX  
CASE 1201-01

A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week

#### ORDERING INFORMATION

Device	Package	Shipping
MC74LCX16373DT	TSSOP-48	39 Units/Rail
MC74LCX16373DTR2	TSSOP-48	2500 Units/Reel

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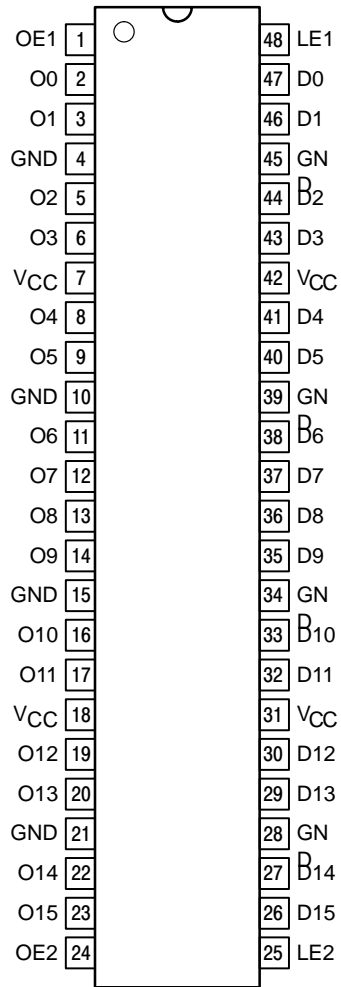


Figure 1. Pinout: 48-Lead  
(Top View)

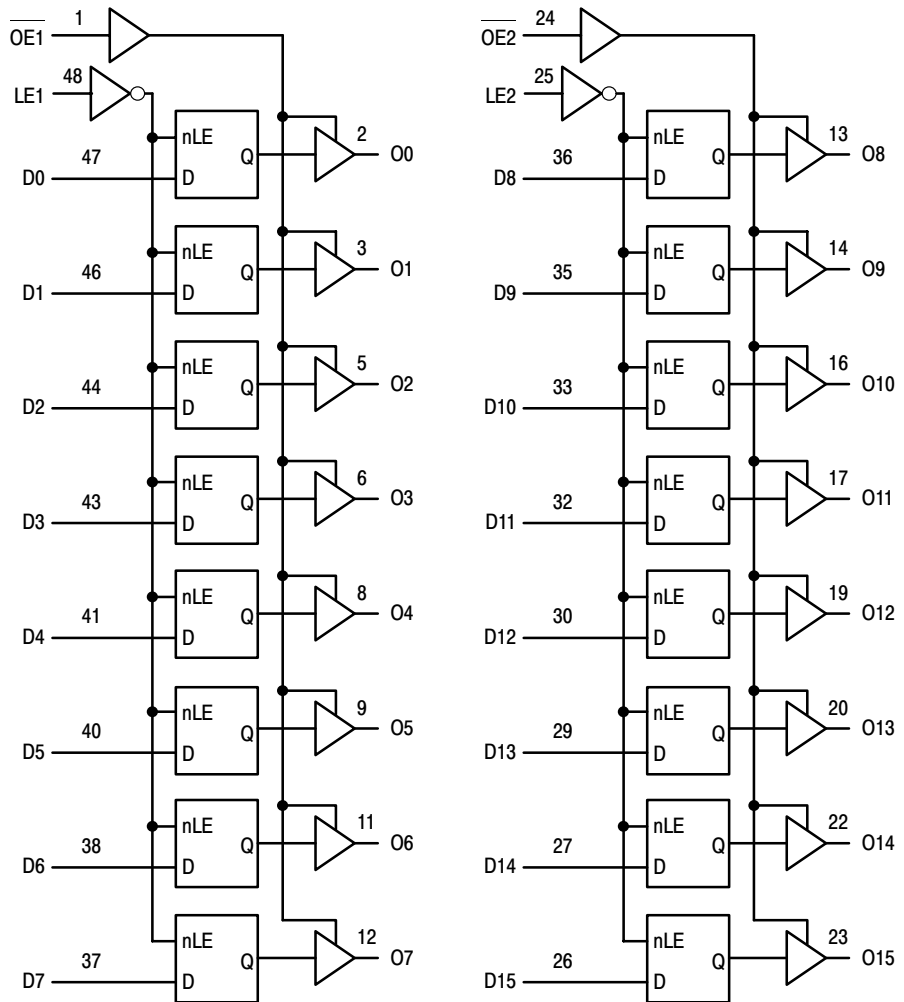


Figure 2. Logic Diagram

### PIN NAMES

PINS	FUNCTION
$\overline{OE}n$	Output Enable Inputs
$\overline{LE}n$	Latch Enable Inputs
D0–D15	Inputs
O0–O15	Outputs

### TRUTH TABLE

Inputs			Outputs	Inputs			Outputs
LE1	$\overline{OE}1$	D0:7	O0:7	LE2	$\overline{OE}2$	D8:15	O8:15
X	H	X	Z	X	H	X	Z
H	L	L	L	H	L	L	L
H	L	H	H	H	L	H	H
L	L	X	O0	L	L	X	O0

H = High Voltage Level; L = Low Voltage Level; Z = High Impedance State; X = High or Low Voltage Level and Transitions Are Acceptable, for I<sub>CC</sub> reasons, DO NOT FLOAT Inputs

# MC74LCX16373

## ABSOLUTE MAXIMUM RATINGS\*

Symbol	Parameter	Value	Condition	Unit
V <sub>CC</sub>	DC Supply Voltage	-0.5 to +7.0		V
V <sub>I</sub>	DC Input Voltage	-0.5 ≤ V <sub>I</sub> ≤ +7.0		V
V <sub>O</sub>	DC Output Voltage	-0.5 ≤ V <sub>O</sub> ≤ +7.0	Output in 3-State	V
		-0.5 ≤ V <sub>O</sub> ≤ V <sub>CC</sub> + 0.5	Output in HIGH or LOW State. (Note 1.)	V
I <sub>IK</sub>	DC Input Diode Current	-50	V <sub>I</sub> < GND	mA
I <sub>OK</sub>	DC Output Diode Current	-50	V <sub>O</sub> < GND	mA
		+50	V <sub>O</sub> > V <sub>CC</sub>	mA
I <sub>O</sub>	DC Output Source/Sink Current	±50		mA
I <sub>CC</sub>	DC Supply Current Per Supply Pin	±100		mA
I <sub>GND</sub>	DC Ground Current Per Ground Pin	±100		mA
T <sub>STG</sub>	Storage Temperature Range	-65 to +150		°C

\* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

1. I<sub>O</sub> absolute maximum rating must be observed.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit	
V <sub>CC</sub>	Supply Voltage	Operating	2.0	2.5, 3.3	3.6	V
		Data Retention Only	1.5	2.5, 3.3	3.6	
V <sub>I</sub>	Input Voltage	0		5.5	V	
V <sub>O</sub>	Output Voltage	(HIGH or LOW State)	0		V <sub>CC</sub>	V
		(3-State)	0		5.5	
I <sub>OH</sub>	HIGH Level Output Current			-24 -12 -8	mA	
I <sub>OL</sub>	LOW Level Output Current	V <sub>CC</sub> = 3.0 V - 3.6 V			+24	mA
		V <sub>CC</sub> = 2.7 V - 3.0 V			+12	
		V <sub>CC</sub> = 2.3 V - 2.7 V			+8	
T <sub>A</sub>	Operating Free-Air Temperature	-40		+85	°C	
Δt/ΔV	Input Transition Rise or Fall Rate, V <sub>IN</sub> from 0.8 V to 2.0 V, V <sub>CC</sub> = 3.0 V	0		10	ns/V	

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## DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	T <sub>A</sub> = -40°C to +85°C		Unit
			Min	Max	
V <sub>IH</sub>	HIGH Level Input Voltage (Note 2.)	2.3 V ≤ V <sub>CC</sub> ≤ 2.7 V	1.7		V
		2.7 V ≤ V <sub>CC</sub> ≤ 3.6 V	2.0		
V <sub>IL</sub>	LOW Level Input Voltage (Note 2.)	2.3 V ≤ V <sub>CC</sub> ≤ 2.7 V		0.7	V
		2.7 V ≤ V <sub>CC</sub> ≤ 3.6 V		0.8	
V <sub>OH</sub>	HIGH Level Output Voltage	2.3 V ≤ V <sub>CC</sub> ≤ 3.6 V; I <sub>OL</sub> = 100 μA	V <sub>CC</sub> - 0.2		V
		V <sub>CC</sub> = 2.3 V; I <sub>OH</sub> = -8 mA	1.8		
		V <sub>CC</sub> = 2.7 V; I <sub>OH</sub> = -12 mA	2.2		
		V <sub>CC</sub> = 3.0 V; I <sub>OH</sub> = -18 mA	2.4		
		V <sub>CC</sub> = 3.0 V; I <sub>OH</sub> = -24 mA	2.2		
V <sub>OL</sub>	LOW Level Output Voltage	2.3 V ≤ V <sub>CC</sub> ≤ 3.6 V; I <sub>OL</sub> = 100 μA		0.2	V
		V <sub>CC</sub> = 2.3 V; I <sub>OL</sub> = 8 mA		0.6	
		V <sub>CC</sub> = 2.7 V; I <sub>OL</sub> = 12 mA		0.4	
		V <sub>CC</sub> = 3.0 V; I <sub>OL</sub> = 16 mA		0.4	
		V <sub>CC</sub> = 3.0 V; I <sub>OL</sub> = 24 mA		0.55	
I <sub>I</sub>	Input Leakage Current	2.3 V ≤ V <sub>CC</sub> ≤ 3.6 V; 0 V ≤ V <sub>I</sub> ≤ 5.5 V		±5.0	μA
I <sub>OZ</sub>	3-State Output Current	2.3 ≤ V <sub>CC</sub> ≤ 3.6 V; 0 V ≤ V <sub>O</sub> ≤ 5.5 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>		±5.0	μA
I <sub>OFF</sub>	Power-Off Leakage Current	V <sub>CC</sub> = 0 V; V <sub>I</sub> or V <sub>O</sub> = 5.5 V		10	μA
I <sub>CC</sub>	Quiescent Supply Current	2.3 ≤ V <sub>CC</sub> ≤ 3.6 V; V <sub>I</sub> = GND or V <sub>CC</sub>		20	μA
I <sub>CC</sub>	Quiescent Supply Current	2.3 ≤ V <sub>CC</sub> ≤ 3.6 V; 3.6 ≤ V <sub>I</sub> or V <sub>O</sub> ≤ 5.5 V		±20	μA
ΔI <sub>CC</sub>	Increase in I <sub>CC</sub> per Input	2.3 ≤ V <sub>CC</sub> ≤ 3.6 V; V <sub>IH</sub> = V <sub>CC</sub> - 0.6 V		500	μA

2. These values of V<sub>I</sub> are used to test DC electrical characteristics only.

## AC CHARACTERISTICS t<sub>R</sub> = t<sub>F</sub> = 2.5 ns; C<sub>L</sub> = 50 pF; R<sub>L</sub> = 500 Ω

Symbol	Parameter	Waveform	Limits						Unit
			T <sub>A</sub> = -40°C to +85°C						
			V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		
			C <sub>L</sub> = 50 pF		C <sub>L</sub> = 50 pF		C <sub>L</sub> = 30 pF		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay D <sub>n</sub> to O <sub>n</sub>	1	1.5	5.4	1.5	5.9	1.5	6.5	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay LE to O <sub>n</sub>	3	1.5	5.5	1.5	6.4	1.5	6.6	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time to High and Low Level	2	1.5	6.1	1.5	6.5	1.5	7.9	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time From High and Low Level	2	1.5	6.0	1.5	6.3	1.5	7.2	ns
t <sub>s</sub>	Setup Time, HIGH or LOW D <sup>n</sup> to LE	3	2.5		2.5		3.0		ns
t <sub>h</sub>	Hold Time, HIGH or LOW D <sup>n</sup> to LE	3	1.5		1.5		2.0		ns
t <sub>w</sub>	LE Pulse Width, HIGH	3	3.0		3.0		3.5		ns
t <sub>OSSL</sub> t <sub>OSSL</sub>	Output-to-Output Skew (Note 3.)			1.0					ns

3. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t<sub>OSSL</sub>) or LOW-to-HIGH (t<sub>OSSL</sub>); parameter guaranteed by design.

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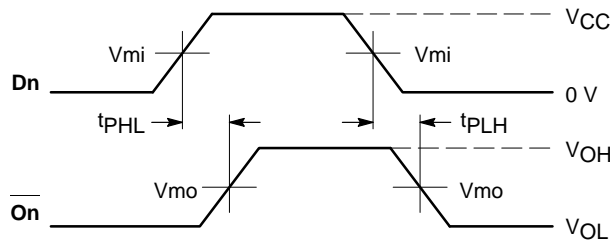
## DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Characteristic	Condition	T <sub>A</sub> = +25°C			Unit
			Min	Typ	Max	
V <sub>OLP</sub>	Dynamic LOW Peak Voltage (Note 4.)	V <sub>CC</sub> = 3.3 V, C <sub>L</sub> = 50 pF, V <sub>IH</sub> = 3.3 V, V <sub>IL</sub> = 0 V		0.8		V
		V <sub>CC</sub> = 2.5 V, C <sub>L</sub> = 30 pF, V <sub>IH</sub> = 2.5 V, V <sub>IL</sub> = 0 V		0.6		V
V <sub>OLV</sub>	Dynamic LOW Valley Voltage (Note 4.)	V <sub>CC</sub> = 3.3 V, C <sub>L</sub> = 50 pF, V <sub>IH</sub> = 3.3 V, V <sub>IL</sub> = 0 V		-0.8		V
		V <sub>CC</sub> = 2.5 V, C <sub>L</sub> = 30 pF, V <sub>IH</sub> = 2.5 V, V <sub>IL</sub> = 0 V		-0.6		V

4. Number of outputs defined as “n”. Measured with “n-1” outputs switching from HIGH-to-LOW or LOW-to-HIGH. The remaining output is measured in the LOW state.

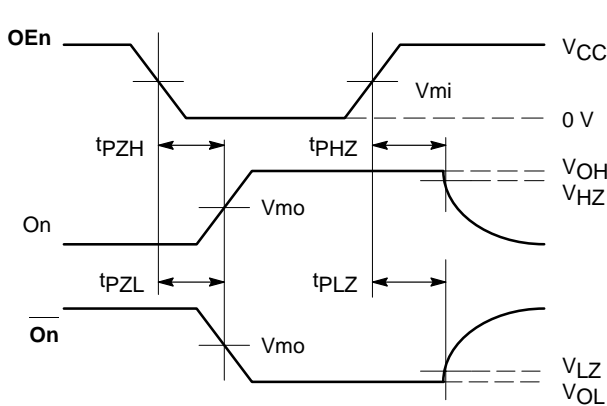
## CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>CC</sub> = 3.3 V, V <sub>I</sub> = 0 V or V <sub>CC</sub>	7	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>CC</sub> = 3.3 V, V <sub>I</sub> = 0 V or V <sub>CC</sub>	8	pF
C <sub>PD</sub>	Power Dissipation Capacitance	10 MHz, V <sub>CC</sub> = 3.3 V, V <sub>I</sub> = 0 V or V <sub>CC</sub>	20	pF



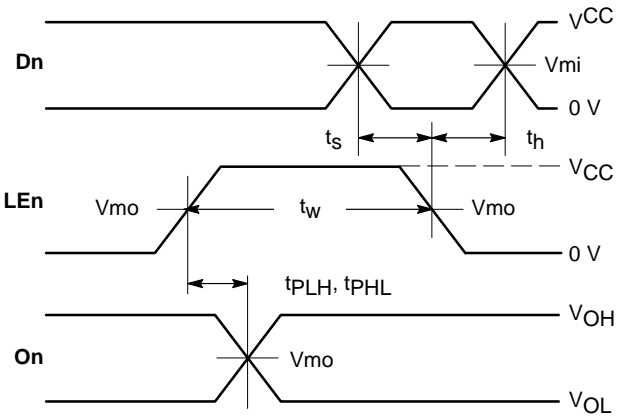
**WAVEFORM 1 – PROPAGATION DELAYS**

t<sub>R</sub> = t<sub>F</sub> = 2.5 ns, 10% to 90%; f = 1 MHz; t<sub>W</sub> = 500 ns



**WAVEFORM 2 – OUTPUT ENABLE AND DISABLE TIMES**

t<sub>R</sub> = t<sub>F</sub> = 2.5 ns, 10% to 90%; f = 1 MHz; t<sub>W</sub> = 500 ns



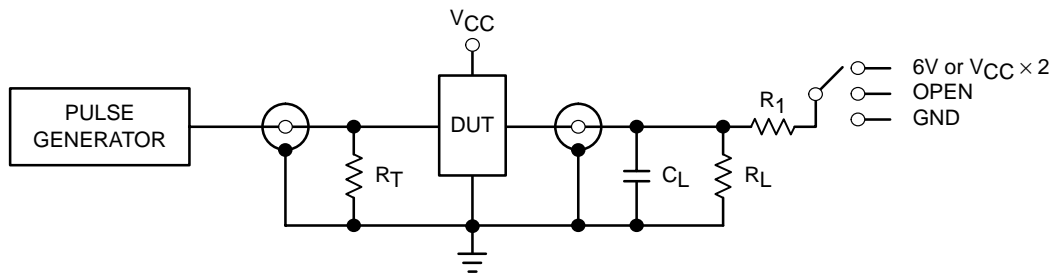
**WAVEFORM 3 – LE to On PROPAGATION DELAYS, LE MINIMUM PULSE WIDTH, Dn to LE SETUP AND HOLD TIMES**

t<sub>R</sub> = t<sub>F</sub> = 2.5ns, 10% to 90%; f = 1MHz; t<sub>W</sub> = 500ns except when noted

Symbol	V <sub>CC</sub>		
	3.3 V ± 0.3 V	2.7 V	2.5 V ± 0.2 V
V <sub>mi</sub>	1.5 V	1.5 V	V <sub>CC</sub> /2
V <sub>mo</sub>	1.5 V	1.5 V	V <sub>CC</sub> /2
V <sub>HZ</sub>	V <sub>OL</sub> + 0.3 V	V <sub>OL</sub> + 0.3 V	V <sub>OL</sub> + 0.15 V
V <sub>LZ</sub>	V <sub>OL</sub> - 0.3 V	V <sub>OL</sub> - 0.3 V	V <sub>OL</sub> - 0.15 V

**Figure 3. AC Waveforms**

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TEST	SWITCH
$t_{PLH}$ , $t_{PHL}$	Open
$t_{PZL}$ , $t_{PLZ}$	6V at $V_{CC} = 3.3 \pm 0.3$ V 6V at $V_{CC} = 2.5 \pm 0.2$ V
Open Collector/Drain $t_{PLH}$ and $t_{PHL}$	6V
$t_{PZH}$ , $t_{PHZ}$	GND

$C_L = 50$  pF at  $V_{CC} = 3.3 \pm 0.3$  V or equivalent (includes jig and probe capacitance)

$C_L = 30$  pF at  $V_{CC} = 2.5 \pm 0.2$  V or equivalent (includes jig and probe capacitance)

$R_L = R_1 = 500$   $\Omega$  or equivalent

$R_T = Z_{OUT}$  of pulse generator (typically 50  $\Omega$ )

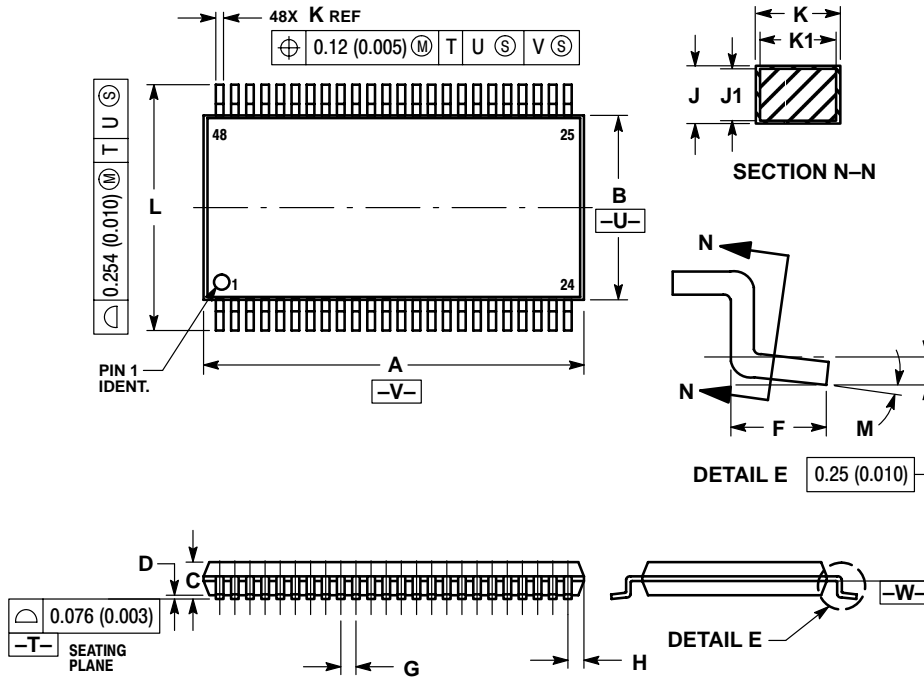
Figure 4. Test Circuit

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## PACKAGE DIMENSIONS

TSSOP-48  
DT SUFFIX  
CASE 1201-01  
ISSUE A


SCALE 2:1



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.40	12.60	0.488	0.496
B	6.00	6.20	0.236	0.244
C	---	1.10	---	0.043
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.50 BSC		0.0197 BSC	
H	0.37	---	0.015	---
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.17	0.27	0.007	0.011
K1	0.17	0.23	0.007	0.009
L	7.95	8.25	0.313	0.325
M	0°	8°	0°	8°

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