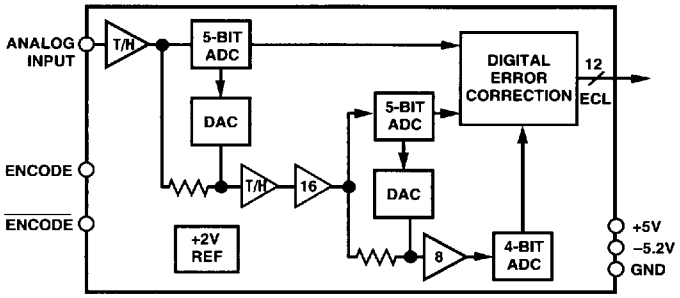
12-Bit 20 MSPS Monolithic A/D Converter

AD9023

FEATURES
Monolithic
12-Bit 20 MSPS A/D Converter
Low Power Dissipation: 1.5 Watts
On-Chip T/H and Reference
High Spurious-Free Dynamic Range
ECL Logic

APPLICATIONS
Radar Receivers
Digital Communications
Digital Instrumentation
Electro-Optic
Medical Imaging
Digital Filters

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD9023 is a high speed, high performance, monolithic 12-bit analog-to-digital converter. All necessary functions, including track-and-hold (T/H) and reference, are included on chip to provide a complete conversion solution. It is a companion unit to the AD9022; the primary difference between the two is that all logic for the AD9022 is TTL compatible, while the AD9023 utilizes ECL logic for digital inputs and outputs. Pinouts for the two parts are nearly identical.

Operating from +5 V and –5.2 V supplies, the AD9023 provides excellent dynamic performance. Sampling at 20 Msps with A_{IN} = 1 MHz, the spurious-free dynamic range (SFDR) is typically 74 dB; with A_{IN} = 9.6 MHz, SFDR is 72 dB. SNR is typically 65 dB.

The on-board T/H has a 110 MHz bandwidth and, more importantly, is designed to provide excellent dynamic performance for analog input frequencies above Nyquist. This feature is necessary in many undersampling signal processing applications, such as in direct IF-to-digital conversion.

To maintain dynamic performance at higher IFs, monolithic RF track-and-holds (such as the AD9100 and AD9101 Samplifier™) can be used with the AD9023 to process signals up to and beyond 70 MHz.

Samplifier is a trademark of Analog Devices, Inc.

With DNL typically less than 0.5 LSB and 20 ns transient response settling time, the AD9023 provides excellent results when low frequency analog inputs must be over-sampled (such as CCD digitization). The full-scale analog input is ±1 V with a 300 Ω input impedance. The analog input can be driven directly from the signal source, or can be buffered by the AD96xx series of low noise, low distortion buffer amplifiers.

All timing is internal to the AD9023; the clock signal initiates the conversion cycle. For best results, the encode command should contain as little jitter as possible. High speed layout practices must be followed to ensure optimum A/D performance.

The AD9023 is built on a trench isolated bipolar process and utilizes an innovative multipass architecture (see the block diagram). The unit is packaged in 28-pin ceramic DIPs and gullwing surface mount packages. The AD9023 is specified to operate over the industrial (–25°C to +85°C) and extended (–55°C to +125°C) temperature ranges.

REV. A

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AD9023–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS ($+V_S$ = +5 V; $-V_S$ = –5.2 V; Encode = 20 MSPS, unless otherwise noted)

Parameter (Conditions)	Temp	Test Level	AD9023AQ/AZ Min	AD9023AQ/AZ Typ	AD9023AQ/AZ Max	AD9023BQ/BZ Min	AD9023BQ/BZ Typ	AD9023BQ/BZ Max	AD9023SQ/SZ Min	AD9023SQ/SZ Typ	AD9023SQ/SZ Max	Units
RESOLUTION			12			12			12			Bits
DC ACCURACY												
Differential Nonlinearity	+25°C	I		0.6	0.75		0.4	0.5		0.6	0.75	LSB
	Full	VI			1.0			1.0			1.0	LSB
Integral Nonlinearity	+25°C	I		1.2	2.5		1.2	2.0		1.2	2.5	LSB
	Full	VI		1.6	3.0		1.6	3.0		1.6	3.0	LSB
No Missing Codes	Full	VI	Guaranteed			Guaranteed			Guaranteed			
Offset Error	+25°C	I		5	25		5	25		5	25	mV
	Full	VI		15	35		15	35		15	35	mV
Gain Error	+25°C	I		0.5	2.5		0.5	2.5		0.5	2.5	% FS
	Full	VI		0.6	3.5		0.6	3.5		0.6	3.5	% FS
Thermal Noise	+25°C	V		0:57			0.57			0.57		LSB, rms
ANALOG INPUT												
Input Voltage Range				±1.024			±1.024			±1.024		V
Input Resistance	Full	IV	240	300	360	240	300	360	240	300	360	Ω
Input Capacitance	+25°C	V		6			6			6		pF
Analog Bandwidth	+25°C	V		110			110			110		MHz
SWITCHING PERFORMANCE[1]												
Minimum Conversion Rate	+25°C	IV			4			4			4	Msps
Maximum Conversion Rate	Full	VI	20			20			20			Msps
Aperture Delay (t_A)	+25°C	IV	0.50	0.78	1.05	0.50	0.78	1.05	0.50	0.78	1.05	ns
Aperture Uncertainty (Jitter)	+25°C	V		5			5			5		ps, rms
Output Delay (t_{OD})	Full	VI	8.5		19.5	8.5		19.5	8.5		19.5	ns
ENCODE INPUT												
Logic Compatibility				ECL			ECL			ECL		
Logic "1" Voltage	Full	VI	–1.1			–1.1			–1.1			V
Logic "0" Voltage	Full	VI			–1.5			–1.5			–1.5	V
Logic "1" Current	Full	VI		5	20		5	20		5	20	µA
Logic "0" Current	Full	VI		5	20		5	20		5	20	µA
Input Capacitance	+25°C	V		6			6			6		pF
Pulse Width (High)	+25°C	IV	22.5		125	22.5		125	22.5		125	ns
Pulse Width (Low)	+25°C	IV	20		125	20		125	20		125	ns
DYNAMIC PERFORMANCE												
Transient Response	+25°C	V		20			20			20		ns
Overvoltage Recovery Time	+25°C	V		20			20			20		ns
Harmonic Distortion[2]												
Analog Input @ 1.2 MHz	+25°C	I	65	72		70	74		65	72		dBc
@ 1.2 MHz	Full			72			74			72		dBc
@ 4.3 MHz	+25°C	V		72			74			72		dBc
@ 9.6 MHz	+25°C	I	63	69		69	71		63	69		dBc
@ 9.6 MHz	Full			68			71			68		dBc
Signal-to-Noise Ratio[2]												
Analog Input @ 1.2 MHz	+25°C	I	62	63		64	65		62	63		dB
@ 1.2 MHz	Full	V		62			64			62		dB
@ 4.3 MHz	+25°C	V		63			65			63		dB
@ 9.6 MHz	+25°C	I	61	62		63	64		61	62		dB
@ 9.6 MHz	Full	V		62			64			62		dB
Signal-to-Noise Ratio[2] (Without Harmonics)												
Analog Input @ 1.2 MHz	+25°C	I	63	64		65	66		63	64		dB
@ 1.2 MHz	Full	V		63			65			63		dB
@ 4.3 MHz	+25°C	V		64			66			64		dB
@ 9.6 MHz	+25°C	I	62	63		64	65		62	63		dB
@ 9.6 MHz	Full	V		62			64			62		dB

Parameter (Conditions)	Temp	Test Level	AD9023AQ/AZ Min	Typ	Max	AD9023BQ/BZ Min	Typ	Max	AD9023SQ/SZ Min	Typ	Max	Units
Two-Tone Intermodulation Distortion Rejection[3]	+25°C	V		74			74			74		dBc
DIGITAL OUTPUTS[1]												
Logic Compatibility				ECL			ECL			ECL		
Logic "1" Voltage	Full	VI	–1.1			–1.1			–1.1			V
Logic "0" Voltage	Full	VI			–1.5			–1.5			–1.5	V
Output Coding				Offset Binary			Offset Binary			Offset Binary		
POWER SUPPLY												
$+V_S$ Supply Voltage	Full	VI	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	mA
$+V_S$ Supply Current	Full	VI		100	120		100	120		100	120	mA
$-V_S$ Supply Voltage	Full	VI	–5.45	–5.2	–4.95	–5.45	–5.2	–4.95	–5.45	–5.2	–4.95	mA
$-V_S$ Supply Current	Full	VI		195	240		195	240		195	240	mA
Power Dissipation	Full	VI		1.5	2.0		1.5	2.0		1.5	2.0	W
Power Supply Rejection Ratio (PSRR)[4]	Full	V		32			32			32		mV/V

NOTES
[1]AD9023 load is 100 Ω to –2.0 V.
[2]RMS signal-to-rms noise with analog input signal 1 dB below full scale at specified frequency.
[3]Intermodulation measured with analog input frequencies of 8.9 MHz and 9.8 MHz at 7 dB below full scale.
[4]PSRR is sensitivity of offset error to power supply variations within the 5% limits shown.
Specifications subject to change without notice.

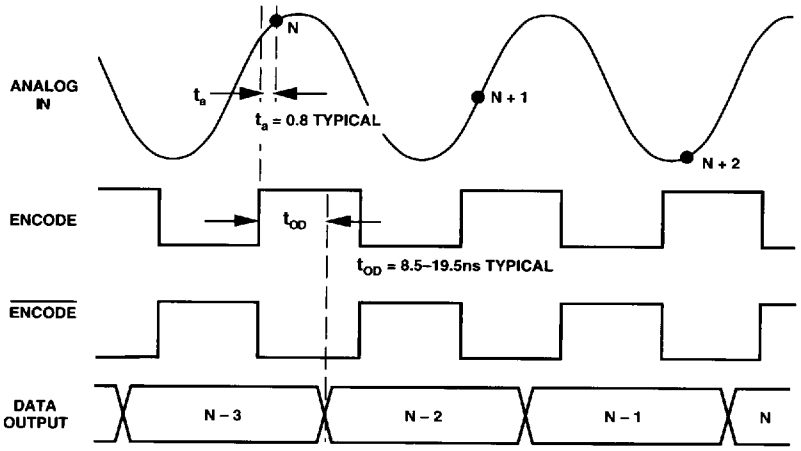
ABSOLUTE MAXIMUM RATINGS[1]

$+V_S$ ..... +6 V
$-V_S$ ..... –6 V
Analog Input ..... $-V_S$ to $+V_S$
Digital Inputs ..... $-V_S$ to 0 V
Digital Output Current ..... 20 mA
Operating Temperature Range
AD9023AQ/AZ/BQ/BZ ..... –25°C to +85°C
AD9023SQ/SZ ..... –55°C to +125°C
Maximum Junction Temperature[2] ..... +175°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Storage Temperature Range ..... –65°C to +150°C

NOTES
[1]Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.
[2]Typical thermal impedances: "Q" Package (Ceramic DIP): θ_{JC} = 10°C/W; θ_{JA} = 35°C/W. "Z" Package (Gullwing Surface Mount): θ_{JC} = 13°C/W; θ_{JA} = 45°C/W.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9023 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



Timing Diagram

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9023AQ/BQ	–25°C to +85°C	28-Pin Ceramic DIP	Q-28
AD9023AZ/BZ	–25°C to +85°C	28-Pin Ceramic Leaded Chip Carrier	Z-28
AD9023SQ	–55°C to +125°C	28-Pin Ceramic DIP	Q-28
AD9023SZ	–55°C to +125°C	28-Pin Ceramic Leaded Chip Carrier	Z-28

EXPLANATION OF TEST LEVELS

Test Level

I – 100% production tested.

II – 100% production tested at +25°C, and sample tested at specified temperatures. AC testing done on sample basis.

III – Sample tested only.

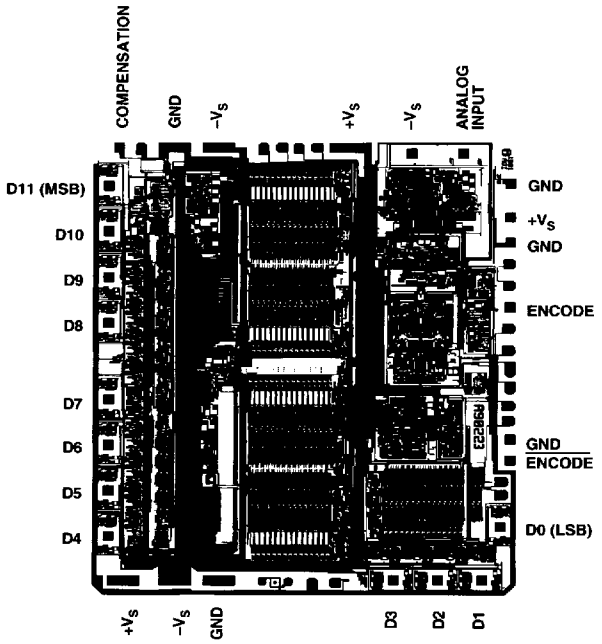
IV – Parameter is guaranteed by design and characterization testing.

V – Parameter is a typical value only.

VI – All devices are 100% production tested at +25°C; guaranteed by design and characterization testing at temperature extremes for industrial devices.

DIE LAYOUT AND MECHANICAL INFORMATION

Die Dimensions	205 × 228 × 21 (±1) mils
Pad Dimensions	4 × 4 mils
Metalization	Aluminum
Backing	None
Substrate Potential	$-V_S$
Transistor Count	4,128
Passivation	Oxynitride
Bond Wire	Aluminum



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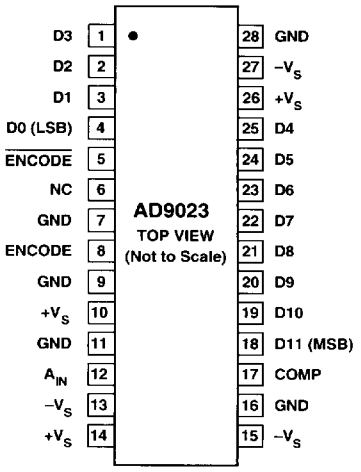
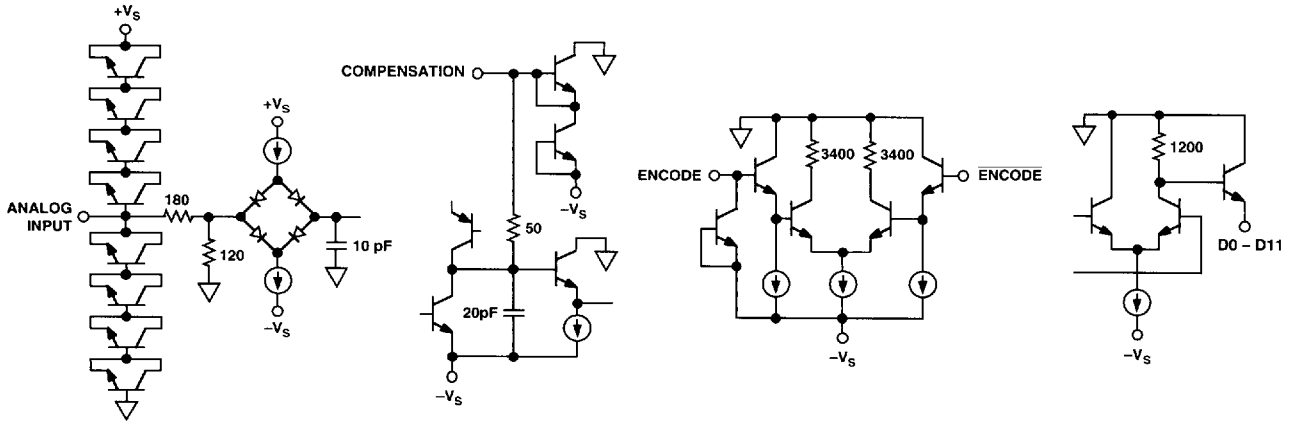
PIN DESCRIPTION

Pin No.	Name	Function
1–3	D3–D1	Digital output bits of ADC; ECL compatible.
4	D0 (LSB)	Least significant bit of ADC output; ECL compatible.
5	$\overline{\text{ENCODE}}$	Complementary encode input to ADC.
6	NC	No Connect
7	GND	Ground
8	ENCODE	Encode clock input to ADC. Internal T/H is placed in hold mode (ADC is encoding) on rising edge of encode signal.
9	GND	Ground
10	$+V_S$	+5 V Power Supply
11	GND	Ground
12	A_{IN}	Noninverting input to T/H amplifier.
13	$-V_S$	–5.2 V Power Supply
14	$+V_S$	+5 V Power Supply
15	$-V_S$	–5.2 V Power Supply
16	GND	Ground
17	COMP	Should be connected to $-V_S$ through 0.1 μF capacitor.
18	D11 (MSB)	Most significant bit of ADC output; ECL compatible.
19–25	D10–D4	Digital output bits of ADC; ECL compatible.
26	$+V_S$	+5 V Power Supply
27	$-V_S$	–5.2 V Power Supply
28	GND	Ground

PIN DESIGNATIONS



NC = NO CONNECT
COMPENSATION (PIN 17) SHOULD BE CONNECTED TO $-V_S$ THROUGH 0.1μF



Analog Input *Compensation* *Encode Input* *Output Stage*

Figure 1. Equivalent Circuits

Typical Characteristics

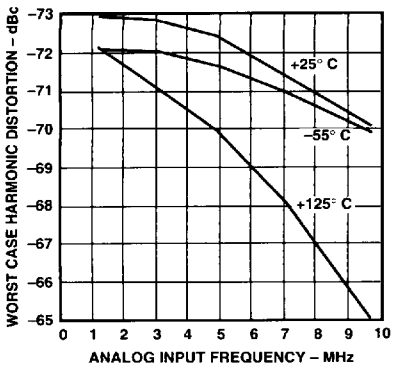


Figure 2. Harmonic Distortion vs. Analog Input Frequency

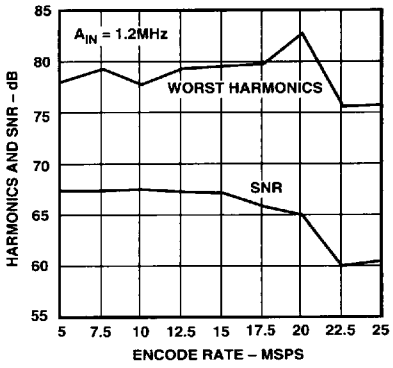


Figure 3. SNR and Harmonics vs. Encode Rate

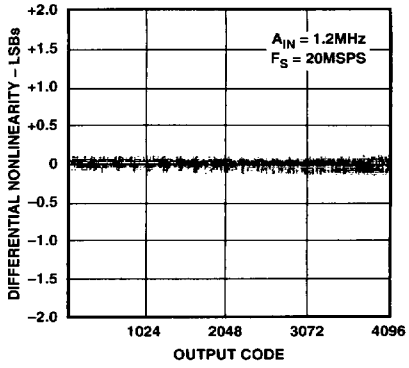


Figure 4. Differential Nonlinearity vs. Output Code

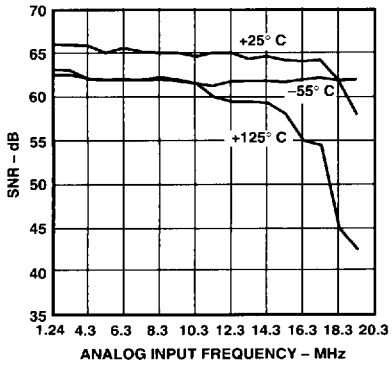


Figure 5. Signal-to-Noise Ratio vs. Analog Input Frequency

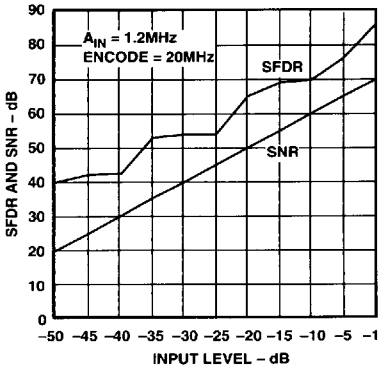


Figure 6. SFDR and SNR vs. Input Level

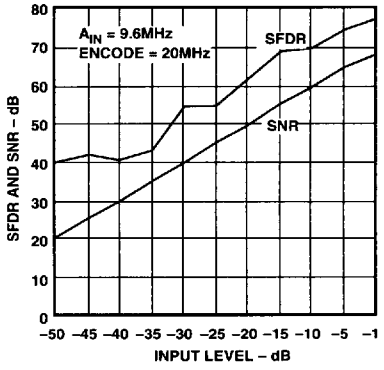


Figure 7. SFDR and SNR vs. Analog Input Level

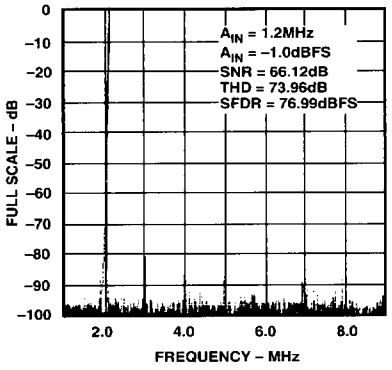


Figure 8. FFT Plot

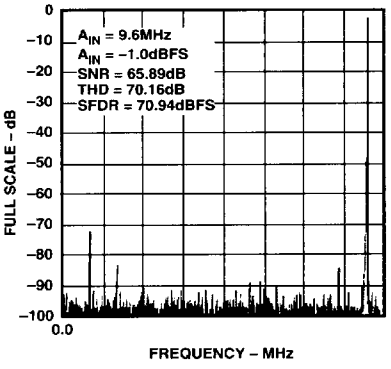


Figure 9. FFT Plot

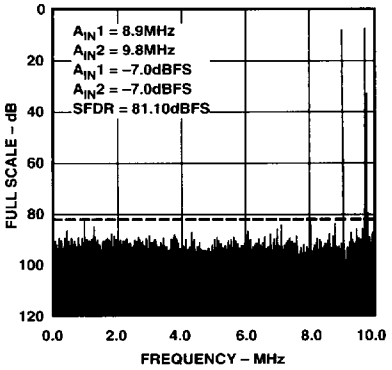


Figure 10. Two Tone FFT

THEORY OF OPERATION

Refer to the block diagram. The AD9023 employs a three pass subranging architecture and digital error correction. This combination of design techniques insures 12-bit accuracy at relatively low power.

Analog input signals are immediately attenuated through a resistor divider and applied directly to the sampling bridge of the track-and-hold (T/H). The T/H holds whatever analog value is present when the unit is strobed with an ENCODE command. The conversion process begins on the rising edge of this pulse, which should conform to the minimum and maximum pulse width requirements shown in the specifications. Operation below the recommended encode rate (4 Msps) may result in excessive droop in the internal T/H devices–leading to large dc and ac errors.

The held analog value of the first track-and-hold is applied to a 5-bit flash converter and a second T/H. The 5-bit flash converter resolves the most significant bits (MSBs) of the held analog voltage. These 5 bits are reconstructed via a 5-bit DAC and subtracted from the original T/H output signal to form a residue signal.

A second T/H holds the amplified residue signal while it is encoded with a second 5-bit flash ADC. Again the 5 bits are reconstructed and subtracted from the second T/H output to form a residue signal. This residue is amplified and encoded with a 4-bit flash ADC to provide the 3 least significant bits (LSBs) of the digital output and one bit of error correction.

Digital Error Correction logic aligns the data from the three flash converters and presents the result as a 12-bit parallel digital word. The output stage of the AD9023 is ECL. Output data may be strobed on the rising edge of the ENCODE command.

AD9023 Noise Performance

High speed, wide bandwidth ADCs such as the AD9023 are optimized for dynamic performance over a wide range of analog input frequencies. However, there are many applications (Imaging, Instrumentation, etc.) where dc precision is also important. Due to the wide input bandwidth of the AD9023 for a given input voltage, there will be a range of output codes which may occur. This is caused by unavoidable circuit noise within the wideband circuits in the ADC. If a dc signal is applied to the ADC and several thousand outputs are recorded, a distribution of codes such as that shown in the histogram below may result.

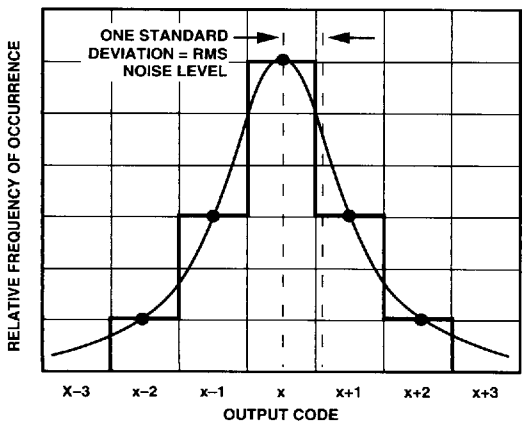


Figure 11. Equivalent Input Noise

The correct code appears most of the time, but adjacent codes also appear with reduced probability. If a normal probability density curve is fitted to this Gaussian distribution of codes, the standard deviation will be equal to the equivalent input rms noise of the ADC. The rms noise may also be approximated by converting the SNR, as measured by a low frequency FFT, to an equivalent input noise. This method is accurate only if the SNR performance is dominated by random thermal noise (the low frequency SNR without harmonics is the best measure). Sixty-three dB equates to 1 LSB rms for a 2 V p-p (0.707 V rms) input signal. The AD9023 has approximately 0.5 LSB of rms noise or a noise limited SNR of 69 dB, indicating that noise alone does not limit the SNR performance of the device (quantization noise and linearity are also major contributors).

This thermal noise may come from several sources. The drive source impedance should be kept low to minimize resistor thermal noise. Some of the internal ADC noise is generated in the wideband T/H. Sampling ADCs generally have input bandwidths which exceed the Nyquist frequency of one-half the sampling rate. (The AD9023 has an input bandwidth of over 100 MHz, even though the sampling rate is limited to 20 Msps.)

USING THE AD9023

Layout Information

Preserving the accuracy and dynamic performance of the AD9023 requires that designers pay special attention to the layout of the printed circuit board.

Analog paths should be kept as short as possible and be properly terminated to avoid reflections. The analog input connection should be kept away from digital signals paths; this reduces the amount of digital switching noise which is capacitively coupled into the analog section. Digital signal paths should also be kept short, and run lengths should be matched to avoid propagation delay mismatch. The AD9023 digital outputs should be buffered or latched close to the device (< 2 cm). This prevents load transients which may feed back into the device.

In high speed circuits, layout of the ground is critical. A single, low impedance ground plane on the component side of the board is recommended. Power supplies should be capacitively coupled to the ground plane with high quality 0.1 µF chip capacitors to reduce noise in the circuit. All power pins of the AD9023 should be bypassed individually. The compensation pin (COMP Pin 17) should be bypassed directly to the $-V_S$ supply (Pin 15) as close to the part as possible using a 0.1 µF chip capacitor.

Multilayer boards allow designers to lay out signal traces without interrupting the ground plane, and provide low impedance ground planes. In systems with dedicated analog and digital grounds, all grounds for the AD9023 should be connected to the analog ground plane.

In systems using multilayer boards, dedicated power planes are recommended to provide low impedance connections for device power. Sockets limit dynamic performance and are not recommended for use with the AD9023.

Timing

Conversion by the AD9023 is initiated by the rising edge of the ENCODE clock (Pin 8). All required timing is generated internal to the ADC. Care should be taken to ensure that the encode clock to the AD9023 is free from jitter that can degrade dynamic performance.

Pulse width of the ADC encode clock must be controlled to ensure the best possible performance. Dynamic performance is guaranteed with a clock pulse HIGH minimum of 25 ns. Operation with narrower pulses will degrade SNR and dynamic performance. From a system perspective, this is generally not a problem because a simple inverter can be used to generate a suitable clock if the system clock is less than 25 ns wide.

The AD9023 provides latched data outputs. Data outputs are available two pipeline delays and one propagation delay after the rising edge of the encode clock (refer to the AD9023 Timing Diagram). The length of the output data lines and the loads placed on them should be minimized to reduce transients within the AD9023; these transients can detract from the converter's dynamic performance. Operation at encode rates less than 4 Msps is not recommended. The internal track-and-hold saturates, causing erroneous conversions. This T/H saturation precludes clocking the AD9023 in a burst mode.

The duty cycle of the encode clock for the AD9023 is critical for obtaining rated performance of the ADC. Internal pulse widths within the track-and-hold are established by the encode command pulse width; to ensure rated performance, minimum and maximum pulse width restrictions should be observed. Operation at 20 Msps is optimized when the duty cycle is held at 55%.

Analog Input

The analog input (Pin 12) voltage range is nominally ±1.024 volts. The range is set with an internal voltage reference and cannot be adjusted by the user. The input resistance is 300 Ω and the analog bandwidth is 110 MHz, making the AD9023 useful in undersampling applications.

The AD9023 should be driven from a low impedance source. The noise and distortion of the amplifier should be considered to preserve the dynamic range of the AD9023.

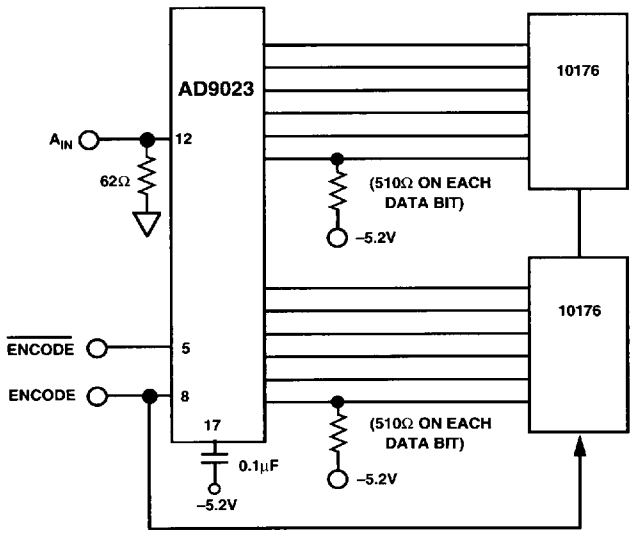


Figure 12. AD9023 Evaluation Board

Power Supplies

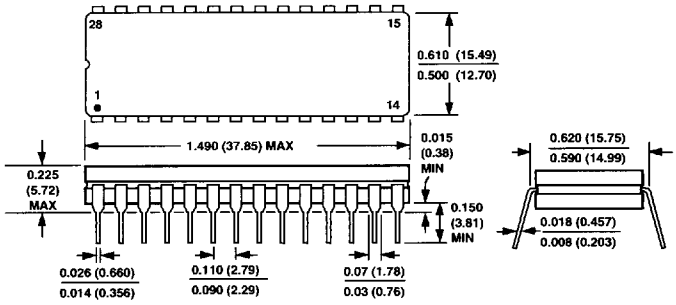
The power supplies of the AD9023 should be isolated from the supplies used for noisy devices (digital logic especially) to reduce the amount of noise coupled into the ADC. For optimum performance, linear supplies ensure that switching noise from the supplies does not introduce distortion products during the encoding process. If switching supplies must be used, decoupling recommendations above are critically important. The PSRR of the AD9023 is a function of the ripple frequency present on the supplies. Clearly, power supplies with the lowest possible frequency should be selected.

C1963–10–10/94

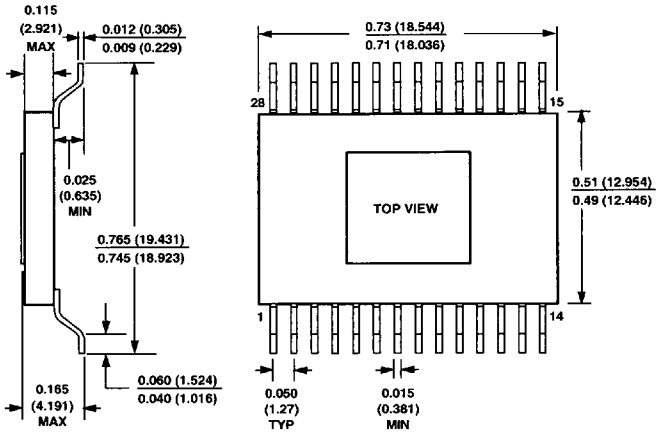
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

Q-28 (Ceramic DIP)



Z-28 (Ceramic Leaded Chip Carrier)



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