REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET																			
REV																			
SHEET	15	16	17	18	19	20	21	22	23	24	25								
REV STATUS OF SHEETS	REV																		
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14				

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
93-11-26

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, ADVANCED CMOS, SERIALLY CONTROLLED ACCESS NETWORK, INVERTING LINE DRIVER WITH THREE-STATE OUTPUTS, TTL COMPATIBLE, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-93127
A	67268	

SHEET 1 OF 25

DESC FORM 193
JUL 91

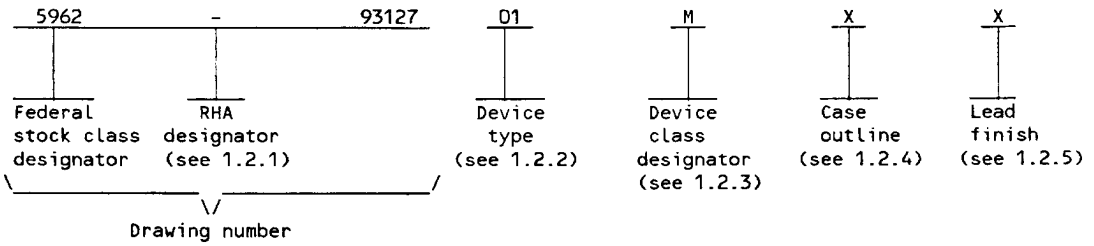
5962-E018-94

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes Q and M) and space application (device class V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device class M RHA marked devices shall meet the MIL-I-38535 appendix A specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	SCAN18540T	Serially controlled access network, inverting line driver with three-state outputs, TTL compatible inputs

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835, and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	GDFP1-F56	56	Flat pack

1.2.5 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein) for class M or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc
DC input voltage range (V_{IN})	-0.5 V dc to V_{CC} + 0.5 V dc
DC output voltage range (V_{OUT})	-0.5 V dc to V_{CC} + 0.5 V dc
DC input clamp current (I_{IK}):	
V_{IN} = -0.5 V	-20 mA
V_{IN} = V_{CC} + 0.5 V	+20 mA
DC output clamp current (I_{OK}):	
V_{OUT} = -0.5 V	-20 mA
V_{OUT} = V_{CC} + 0.5 V	+20 mA
DC output source/sink current (I_{OL})	±70 mA
DC V_{CC} or GND current (I_{CC}, I_{GND})	±1330 mA 4/
Storage temperature range (T_{STG})	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (Θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+175°C
Maximum power dissipation (P_D)	750 mW

1.4 Recommended operating conditions. 2/ 3/

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Input voltage range (V_{IN})	+0.0 V dc to V_{CC}
Output voltage range (V_{OUT})	+0.0 V dc to V_{CC}
Maximum low level input voltage (V_{IL})	0.8 V
Minimum high level input voltage (V_{IH})	2.0 V
Case operating temperature range (T_C)	-55°C to +125°C
Minimum input edge rate ($\Delta V/\Delta t$) (V_{IN} from 0.8 V to 2.0 V or from 2.0 V to 0.8 V)	125 mV/ns
Maximum high level output current (I_{OH})	-24 mA
Maximum low level output current (I_{OL})	48 mA

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	XX percent 5/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, bulletin, and handbook. Unless otherwise specified, the following specification, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Unless otherwise noted, all voltages are referenced to GND.

3/ The limits for the parameters specified herein shall apply over the full specified V_{CC} range and case temperature range of -55°C to +125°C.

4/ This value represents the maximum total current flowing into or out of all V_{CC} or GND pins.

5/ Values will be added when they become available.

SPECIFICATION

MILITARY

MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DOD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS (IEEE)

IEEE Standard 1149.1 - IEEE Standard Test Access Port and Boundary Scan Architecture.

(Applications for copies should be addressed to the Institute of Electrical and Electronics Engineers, 445 Hoes Lane, Piscataway, NJ 08854-4150.)

ELECTRONIC INDUSTRIES ASSOCIATIONS (EIA)

JEDEC Standard No. 20 - Standardized for Description of 54/74ACXXXX and 54/74ACTXXXX Advanced High-Speed CMOS Devices.

(Applications for copies should be addressed to the Electronics Industries Association, 2001 Eye Street, NW, Washington, DC 20006.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents may also be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Block diagrams. The block diagrams shall be as specified on figure 3.

3.2.5 Description of boundary-scan circuitry. The description of boundary-scan circuitry shall be as specified on figure 4.

3.2.6 Ground bounce load circuit and waveforms. The ground bounce load circuit and waveforms shall be as specified on figure 5.

3.2.7 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 6.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range. Test conditions for these specified characteristics and limits are as specified in table I.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.2 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.1 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 37 (see MIL-I-38535, appendix A).

3.11 IEEE 1149.1 compliance. This device shall be compliant with IEEE 1149.1.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein). For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

TABLE I. Electrical performance characteristics.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ $-55°C \le T_C \le +125°C$, $+4.5\ V \le V_{CC} \le +5.5\ V$, unless otherwise specified		V_{CC}	Group A subgroups	Limits 3/ Min	Limits 3/ Max	Unit
High level output voltage 3006	V_{OH}	For all inputs affecting output under test V_{IN} = 2.0 V or 0.8 V; For all other inputs $V_{IN} = V_{CC}$ or GND	I_{OH} = -50 µA	4.5 V	1, 2, 3	3.15		V
				5.5 V	1, 2, 3	4.15		
			I_{OH} = -24 mA	4.5 V	1, 2, 3	2.4		
				5.5 V	1, 2, 3	2.4		
			I_{OH} = -27 mA 4/	5.5 V	1, 2, 3	2.0		
Low level output voltage 3007	V_{OL}	For all inputs affecting output under test V_{IN} = 2.0 V or 0.8 V; For all other inputs $V_{IN} = V_{CC}$ or GND	I_{OL} = 50 µA	4.5 V	1, 2, 3		0.10	V
				5.5 V	1, 2, 3		0.10	
			I_{OL} = 48 mA	4.5 V	1, 2, 3		0.55	
				5.5 V	1, 2, 3		0.55	
			I_{OL} = 63 mA 4/	5.5 V	1, 2, 3		0.8	
Positive input clamp voltage 3022	V_{IC+}	For input under test I_{IN} = 18 mA		5.5 V	1, 2, 3		5.7	V
Negative input clamp voltage 3022	V_{IC-}	For input under test I_{IN} = -18 mA		5.5 V	1, 2, 3		-1.2	V
Input current high 3010	I_{IH}	For input under test V_{IN} = 5.5 V; For all other inputs $V_{IN} = V_{CC}$ or GND	TDI and TMS inputs	5.5 V	1		2.8	µA
					2, 3		3.7	
			All other inputs	5.5 V	1		0.1	
					2, 3		1.0	
Input current low 3009	I_{IL}	For input under test V_{IN} = 0.0 V; For all other inputs $V_{IN} = V_{CC}$ or GND	TDI and TMS inputs	5.5 V	1, 2, 3	-160	-385	µA
			All other inputs	5.5 V	1		-0.1	
					2, 3		-1.0	
Three-state output leakage current high 3021	I_{OZH} 5/	$\overline{AOE}_m$ or $\overline{BOE}_m$ = 2.0 V; For all other inputs, $V_{IN} = V_{CC}$ or GND; V_{OUT} = 4.5 V		4.5 V	1		0.5	µA
					2, 3		10.0	
				5.5 V	1		0.5	
					2, 3		10.0	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified		V_{CC}	Group A subgroups	Limits 3/		Unit
						Min	Max	
Three-state output leakage current low 3020	I_{OZL} 5/	$\overline{AOE}_m$ or $\overline{BOE}_m$ = 2.0 V For all other inputs, $V_{IN} = V_{CC}$ or GND V_{OUT} = 0.0 V		4.5 V	1		-0.5	µA
					2, 3		-10.0	
				5.5 V	1		-0.5	
					2, 3		-10.0	
Output short circuit current 3011	I_{OS} 6/	For all inputs, $V_{IN} = V_{CC}$ or GND V_{OUT} = 0.0 V		5.5 V	1, 2, 3	-100		mA
Quiescent supply current 3005	I_{CC}	For all other inputs $V_{IN} = V_{CC}$ or GND V_{OUT} = open	TDI, TDM = 5.5 V	5.5 V	1		16	µA
					2, 3		168	
			TDI, TDM = 0.0 V	5.5 V	1		750	
					2, 3		930	
Quiescent supply current delta, TTL input level 3005	ΔI_{CC} 7/	For input under test $V_{IN} = V_{CC} - 2.1$ V For all other inputs $V_{IN} = V_{CC}$ or GND	TDI and TMS inputs	5.5 V	1, 2, 3		2.15	mA
			All other inputs	5.5 V	1, 2, 3		2.0	
Input capacitance 3012	C_{IN}	T_C = +25°C See 4.4.1c		5.0 V	4		5	pF
Output capacitance 3012	C_{OUT} 5/			5.0 V	4		15	pF
Power dissipation capacitance	C_{PD} 8/			5.0 V	4		35	pF
Low level ground bounce noise	V_{OLP} 9/	V_{IH} = 3.0 V, V_{IL} = 0.0 V T_A = +25°C See 4.4.1d See figure 5		5.0 V	4		800	mV
	V_{OLV} 9/			5.0 V	4		-500	
High level V_{CC} bounce noise	V_{OHP} 9/			5.0 V	4		V_{OH} + 800	mV
	V_{OHV} 9/			5.0 V	4		V_{OH} - 500	
Functional test	10/	V_{IH} = 2.0 V, V_{IL} = 0.8 V Verify output V_O See 4.4.1b		4.5 V	7, 8	L	H	
				5.5 V	7, 8	L	H	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	V_{CC}	Group A subgroups	Limits 3/ Min	Limits 3/ Max	Unit
NORMAL OPERATION							
Propagation delay time, $\overline{AI}_n/BI_n$ to AO_n/BO_n 3003	t_{PLH1} 11/	C_L = 50 pF minimum R_L = 500Ω See figure 6	4.5 V	9	2.5	9.0	ns
				10, 11	2.5	10.5	
	t_{PHL1} 11/		4.5 V	9	2.5	9.0	ns
				10, 11	2.5	11.0	
Propagation delay time, output enable, $\overline{AOE}_m/\overline{BOE}_m$ to AO_n/BO_n 3003	t_{PZH1} 11/		4.5 V	9	2.0	11.0	ns
				10, 11	2.0	12.0	
	t_{PZL1} 11/		4.5 V	9	2.0	12.3	ns
				10, 11	2.0	14.0	
Propagation delay time, output disable, $\overline{AOE}_m/\overline{BOE}_m$ to AO_n/BO_n 3003	t_{PHZ1}, t_{PLZ1} 11/		4.5 V	9	1.5	10.2	ns
				10, 11	1.5	11.2	
Output skew	t_{OSHL}, t_{OSLH} 13/		4.5 V	9, 10, 11		1.0	ns
SCAN TEST OPERATION							
Propagation delay time, TCK to TDO 3003	t_{PLH2}, t_{PHL2} 11/	C_L = 50 pF minimum R_L = 500Ω See figure 6	4.5 V	9	3.5	13.2	ns
				10, 11	3.5	15.8	
Propagation delay time, output enable, TCK to TDO 3003	t_{PZH2} 11/		4.5 V	9	3.0	14.5	ns
				10, 11	3.0	16.7	
	t_{PZL2} 11/		4.5 V	9	3.0	15.0	ns
				10, 11	3.0	16.7	
Propagation delay time, output disable, TCK to TDO 3003	t_{PHZ2} 11/		4.5 V	9	2.5	11.5	ns
				10, 11	2.5	12.8	
	t_{PLZ2} 11/		4.5 V	9	2.5	12.0	ns
				10, 11	2.5	12.8	
Propagation delay time, TCK to data out, during update-DR state 3003	t_{PLH3}, t_{PHL3} 11/		4.5 V	9	5.0	18.0	ns
				10, 11	5.0	21.7	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	V_{CC}	Group A subgroups	Limits 3/		Unit
					Min	Max	
Propagation delay time, TCK to data out, during update-IR state 3003	t_{PLH4}, t_{PHL4} 11/	C_L = 50 pF minimum R_L = 500Ω See figure 6	4.5 V	9	5.0	18.6	ns
				10, 11	5.0	21.2	
Propagation delay time, TCK to data out, during test logic reset 3003	t_{PLH5}, t_{PHL5} 11/		4.5 V	9	5.5	19.9	ns
				10, 11	5.5	23.0	
Propagation delay time, output disable, TCK to data out, during update-DR state 3003	t_{PHZ3}, t_{PLZ3} 11/		4.5 V	9	4.0	16.4	ns
				10, 11	4.0	19.6	
Propagation delay time, output disable, TCK to data out, during update-IR state 3003	t_{PHZ4}, t_{PLZ4} 11/		4.5 V	9	5.0	19.5	ns
				10, 11	5.0	22.4	
Propagation delay time, output disable, TCK to data out, during test logic reset 3003	t_{PHZ5}, t_{PLZ5} 11/		4.5 V	9	5.0	19.9	ns
				10, 11	5.0	23.3	
Propagation delay time, output enable, TCK to data out, during update-DR state 3003	t_{PZH3}, t_{PZL3} 11/		4.5 V	9	5.0	18.9	ns
				10, 11	5.0	22.6	
Propagation delay time, output enable, TCK to data out, during update-IR state 3003	t_{PZH4}, t_{PZL4} 11/		4.5 V	9	6.5	22.4	ns
				10, 11	6.5	26.2	
Propagation delay time, output enable, TCK to data out, during test logic reset 3003	t_{PZH5}, t_{PZL5} 11/		4.5 V	9	7.0	23.8	ns
				10, 11	7.0	27.4	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	V_{CC}	Group A subgroups	Limits 3/		Unit
					Min	Max	
Setup time, high or low, data to TCK	t_{s1} 12/ 14/	C_L = 50 pF minimum R_L = 500Ω See figure 6	4.5 V	9, 10, 11	3.0		ns
Hold time, high or low, TCK to data	t_{h1} 12/ 14/		4.5 V	9	4.5		ns
				10, 11	5.5		
Setup time, high or low, AOE_m, BOE_m to TCK	t_{s2} 12/ 15/		4.5 V	9, 10, 11	3.0		ns
Hold time, high or low, TCK to AOE_m, BOE_m	t_{h2} 12/ 15/		4.5 V	9, 10, 11	4.5		ns
Setup time, high or low, internal AOE_m, BOE_m to TCK	t_{s3} 12/ 16/		4.5 V	9, 10, 11	3.0		ns
Hold time, high or low, TCK to internal AOE_m, $\overline{BOE_m}$	t_{h3} 12/ 16/		4.5 V	9, 10, 11	3.0		ns
Setup time, high or low, TMS to TCK	t_{s4} 12/		4.5 V	9, 10, 11	8.0		ns
Hold time, high or low, TCK to TMS	t_{h4} 12/		4.5 V	9, 10, 11	2.0		ns
Setup time, high or low, TDI to TCK	t_{s5} 12/		4.5 V	9, 10, 11	4.0		ns
Hold time, high or low, TCK to TDI	t_{h5} 12/		4.5 V	9, 10, 11	4.5		ns
Pulse width, high, TCK	t_{w1} 12/		4.5 V	9, 10, 11	12.0		ns
Pulse width, low, TCK	t_{w2} 12/		4.5 V	9, 10, 11	5.0		ns
Wait time, power-up to TCK	t_{pu} 12/	C_L = 50 pF minimum R_L = 500Ω	4.5 V	9, 10, 11		100	ns
Power down delay time	t_{dn} 12/		0.0 V	9, 10, 11		100	ms
Maximum TCK clock frequency	f_{MAX} 12/		4.5 V	9, 10, 11	25		MHz

1/ For tests not listed in the referenced MIL-STD-883 (e.g. ΔI_{CC}), utilize the general test procedure of 883 under the conditions listed herein.

2/ Each input/output, as applicable, shall be tested at the specified temperature, for the specified limits, to the tests in table I herein. Output terminals not designated shall be high level logic, low level logic, or open, except for the I_{CC} and ΔI_{CC} tests, the output terminals shall be open. When performing the I_{CC} and ΔI_{CC} tests, the current meter shall be placed in the circuit such that all current flows through the meter.

3/ For negative and positive voltage and current values, the sign designates the potential difference in reference to GND and the direction of current flow respectively; and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein. All devices shall meet or exceed the limits specified in table I , as applicable, at 4.5 V ≤ V_{CC} ≤ 5.5 V.

4/ Transmission driving tests are performed at V_{CC} = 5.5 V dc with a 2 ms duration maximum. This test may be performed using V_{IN} = V_{CC} or GND. When V_{IN} = V_{CC} or GND is used, the test is guaranteed for V_{IN} = 2.0 V or 0.8 V.

5/ Three-state output conditions are required.

6/ This test shall be performed one output loaded at a time with a 2 ms duration maximum.

7/ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}. This test may be performed either one input at a time (preferred method) or with all input pins simultaneously at V_{IN} = V_{CC} - 2.1 V (alternate method). When the test is performed using the alternate test method, the maximum limit is equal to the number of inputs at a high TTL input level times 2.0 mA or 2.15 mA, as applicable; and the preferred method and limits are guaranteed. When testing the TDI input, the TMS input shall be open. When testing the TMS input, the TDI input shall be open.

8/ Power dissipation capacitance (C_{PD}) determines both the power consumption (P_D) and current consumption (I_S). Where

$$P_D = (C_{PD} + C_L)(V_{CC} \times V_{CC})f + (I_{CC} \times V_{CC}) + (n \times d \times \Delta I_{CC} \times V_{CC})$$
$$I_S = (C_{PD} + C_L) V_{CC} f + I_{CC} + (n \times d \times \Delta I_{CC})$$

and f is the frequency of the input signal; n is the number of device inputs at TTL levels; and d is the duty cycle of the input signal.

9/ This test is for qualification only. Ground and V_{CC} bounce tests are performed on a non-switching (quiescent) output and are used to measure the magnitude of induced noise caused by other simultaneously switching outputs. The test is performed on a low noise bench test fixture. For the device under test, all outputs shall be loaded with 50Ω of load resistance and a minimum of 50 pF of load capacitance (see figure 5). Only chip capacitors and resistors shall be used. The output load components shall be located as close as possible to the device outputs. It is suggested that, whenever possible, this distance be kept to less than 0.25 inches. Decoupling capacitors shall be placed in parallel from V_{CC} to ground. The values of these decoupling capacitors shall be determined by the device manufacturer. The low and high level ground and V_{CC} bounce noise is measured at the quiet output using a 1 GHz minimum bandwidth oscilloscope with a 50Ω input impedance.

The device inputs shall be conditioned such that all outputs are at a high nominal V_{OH} level. The device inputs shall then be conditioned such that they switch simultaneously and the output under test remains at V_{OH} as all other outputs possible are switched from V_{OH} to V_{OL}. V_{OHV} and V_{OHP} are then measured from the nominal V_{OH} level to the largest negative and positive peaks, respectively (see figure 5). This is then repeated with the same outputs not under test switching from V_{OL} to V_{OH}.

The device inputs shall be conditioned such that all outputs are at a low nominal V_{OL} level. The device inputs shall then be conditioned such that they switch simultaneously and the output under test remains at V_{OL} as all other outputs possible are switched from V_{OL} to V_{OH}. V_{OLP} and V_{OLV} are then measured from the nominal V_{OL} level to the largest positive and negative peaks, respectively (see figure 5). This is then repeated with the same outputs not under test switching from V_{OH} to V_{OL}.

10/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic patterns used for fault detection. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2 herein. For V_{OUT} measurements, L < 1.5 V and H ≥ 1.5 V.

11/ AC limits at V_{CC} = 5.5 V are equal to the limits at V_{CC} = 4.5 V and guaranteed by testing at V_{CC} = 4.5 V. Minimum propagation delay time limits for V_{CC} = 5.5 V shall be guaranteed to be no more than 0.5 ns less than those specified at V_{CC} = 4.5 V in table I herein. For propagation delay tests, all paths must be tested.

TABLE I. Electrical performance characteristics - Continued.

12/ This parameter shall be guaranteed, if not tested, to the limits specified in table I herein.

13/ This parameter is guaranteed, if not tested, to the limits specified in table I herein. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device: AO_m and AO_k; AO_m and BO_n; BO_m and BO_k; where k = 0 to 8, m = 0 to 8, and n = 0 to 8; and where $m \neq k$. The specification applies to any outputs switching in the same direction, either high-to-low (t_{OSHL}) or low-to-high (t_{OSLH}). The limits at V_{CC} = 5.5 V are equal to the limits at V_{CC} = 4.5 V and guaranteed by testing at V_{CC} = 4.5 V.

14/ This delay represents the timing relationship between the data input and TCK at the associated scan cells numbered 0-8, 9-17, 18-26, and 27-35.

15/ This timing parameter pertains to boundary scan registers (BSR) 37, 38, 40, and 41.

16/ This delay represents the timing relationship between $\overline{AOE}_n/\overline{BOE}_n$ and TCK for scan cells 36 and 39 only.

Device type	01						
Case outline	X						
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	$\overline{TMS}$	15	$\overline{BO}_0$	29	TCK	43	AI_8
2	$\overline{AO}_0$	16	BO_1	30	$\overline{BI}_8$	44	AI_7
3	$\overline{AOE}_1$	17	GND	31	$\overline{BOE}_2$	45	GND
4	$\overline{AO}_1$	18	$\overline{BO}_2$	32	BI_7	46	AI_6
5	$\overline{AO}_2$	19	$\overline{BO}_3$	33	BI_6	47	AI_5
6	GND	20	V_{CC}	34	GND	48	V_{CC}
7	$\overline{AO}_3$	21	$\overline{BO}_4$	35	BI_5	49	AI_4
8	$\overline{AO}_4$	22	$\overline{BO}_5$	36	BI_4	50	AI_3
9	V_{CC}	23	GND	37	V_{CC}	51	GND
10	$\overline{AO}_5$	24	$\overline{BO}_6$	38	BI_3	52	AI_2
11	$\overline{AO}_6$	25	$\overline{BO}_7$	39	BI_2	53	$\overline{AI}_1$
12	GND	26	$\overline{BOE}_1$	40	GND	54	$\overline{AOE}_2$
13	$\overline{AO}_7$	27	$\overline{BO}_8$	41	BI_1	55	AI_0
14	$\overline{AO}_8$	28	TDO	42	BI_0	56	TDI

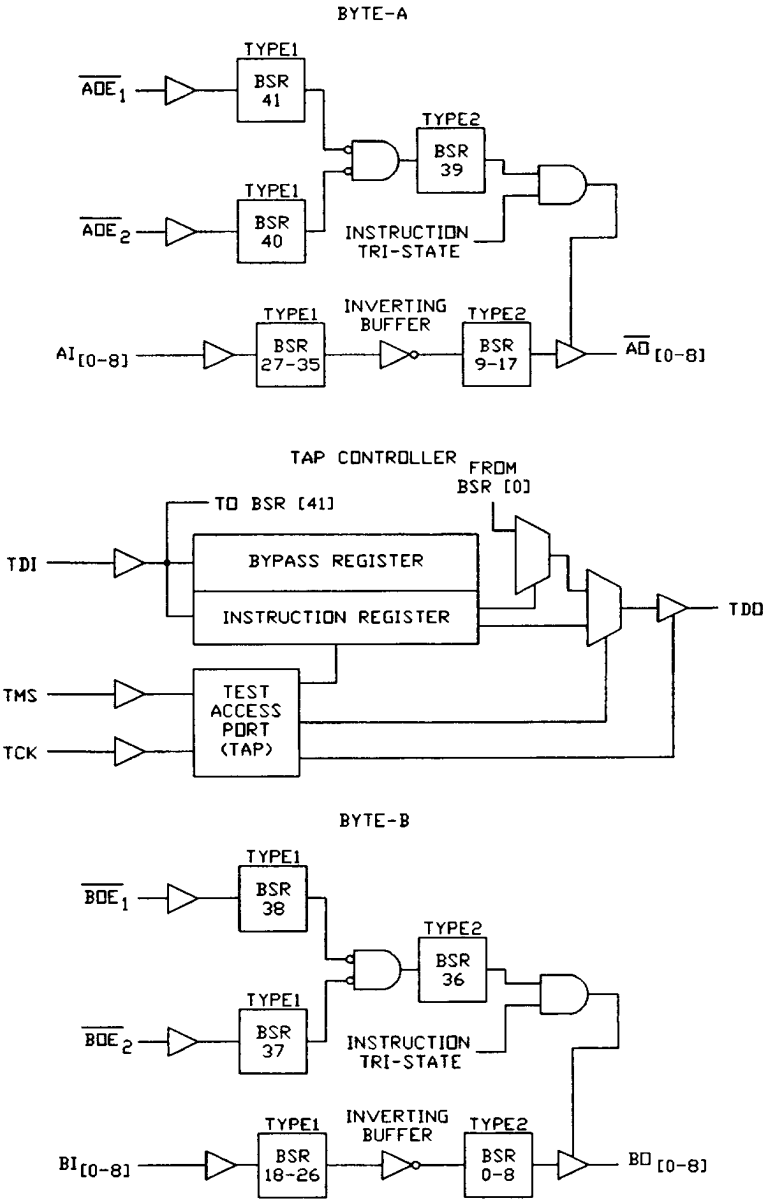
Terminal descriptions	
Terminal symbol	Description
AI_n (n = 0 to 8) BI_n (n = 0 to 8)	Data inputs, A side Data inputs, B side
$\overline{AO}_n$ (n = 0 to 8) $\overline{BO}_n$ (n = 0 to 8)	Outputs, A side Outputs, B side
$\overline{AOE}_m$ (m = 1, 2) $\overline{BOE}_m$ (m = 1, 2)	Output enable control inputs, A side Output enable control inputs, B side
TDI TDO TMS TCK	Test data input Test data output Test mode select input Test clock input

FIGURE 1. Terminal connections.

Device type 01			
Inputs			Outputs
$\overline{AOE}_1/\overline{BOE}_1$	$\overline{AOE}_2/\overline{BOE}_2$	AI_n/BI_n	$\overline{AO}_n/\overline{BO}_n$
L	L	H	L
H	X	X	Z
X	H	X	Z
L	L	L	H

H = High voltage level
L = Low voltage level
X = Immaterial
Z = High impedance

FIGURE 2. Truth table.



NOTES:
1. BSR stands for boundary-scan register.
2. See figure 4 for further description.

FIGURE 3. Block diagrams.

Boundary-scan register scan chain definition

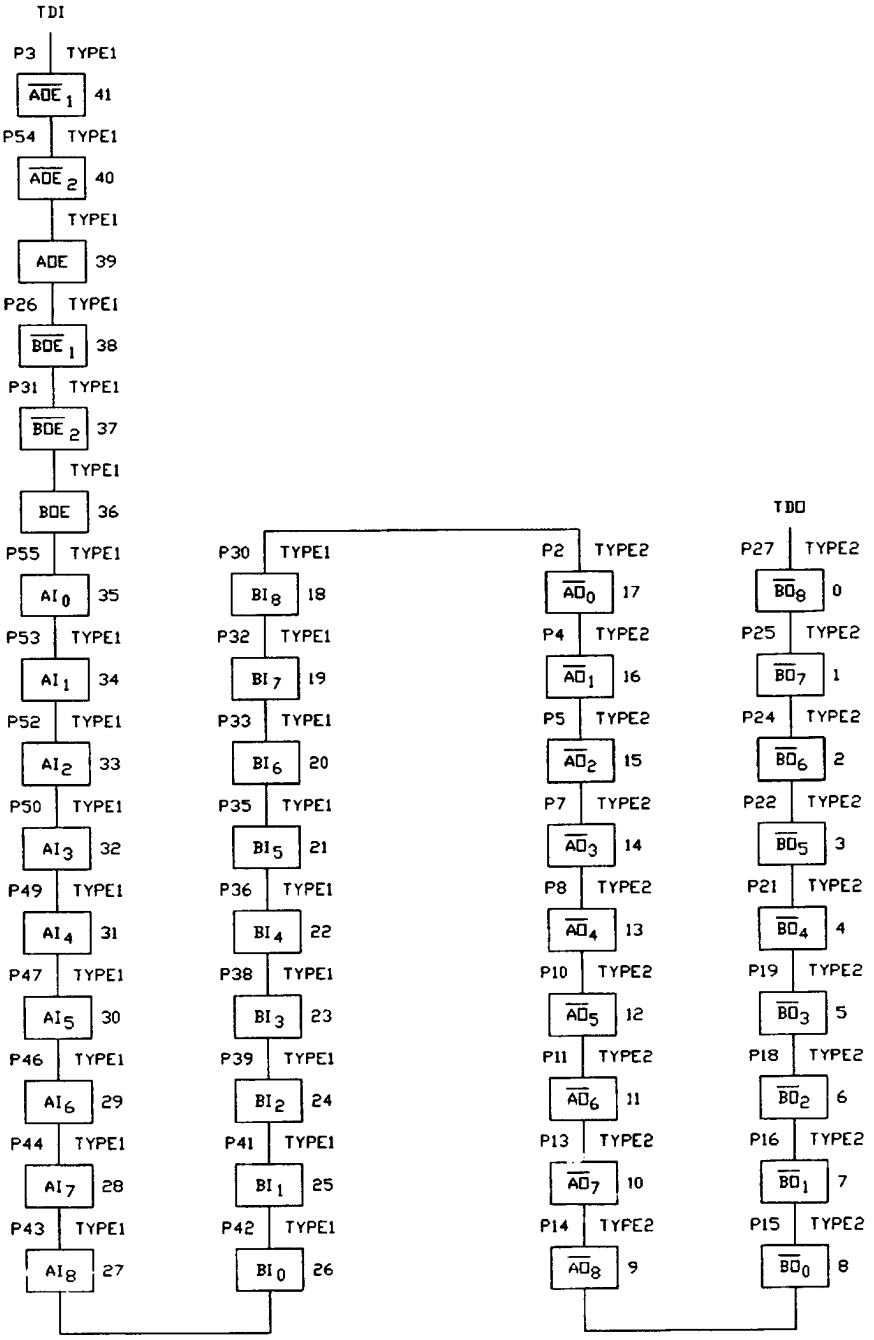
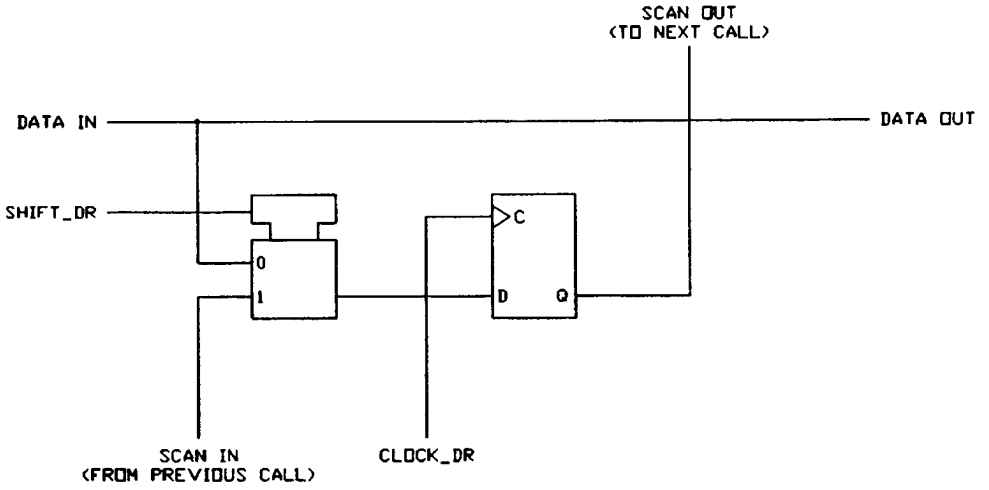


FIGURE 4. Description of boundary-scan circuitry.

The scan cells used in the boundary-scan register are one of the following two types depending upon their location. Scan cell TYPE1 is intended to solely observe system data, while TYPE2 has the additional ability to control system data. (See IEEE Standard 1149.1 for a further description of the scan cells.)

Scan cell TYPE1
Located on each system input pin



Scan cell TYPE2
Located at each system output pin as well as at each
of the two internal active-high output enable signals

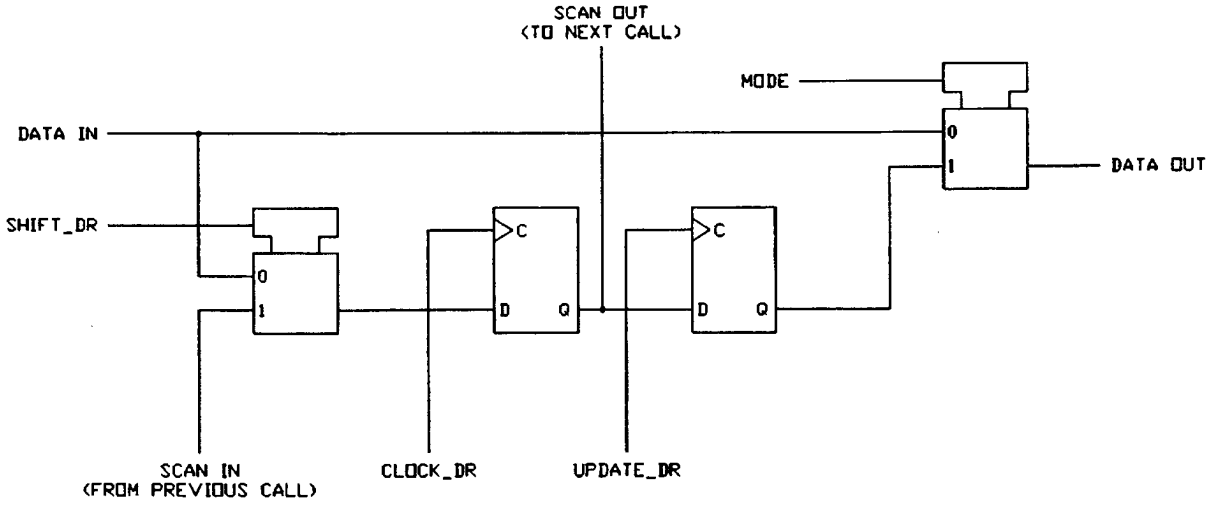
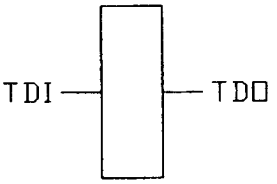


FIGURE 4. Description of boundary-scan circuitry - Continued.

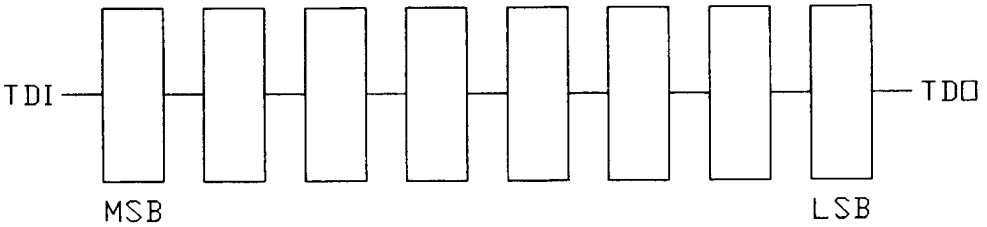
The bypass register is a single bit shift register stage identical to scan cell TYPE1. It captures a fixed logic low.

Bypass register scan chain definition
Logic 0



The instruction register is an eight-bit register which captures the value 01001101.

Instruction register scan chain definition

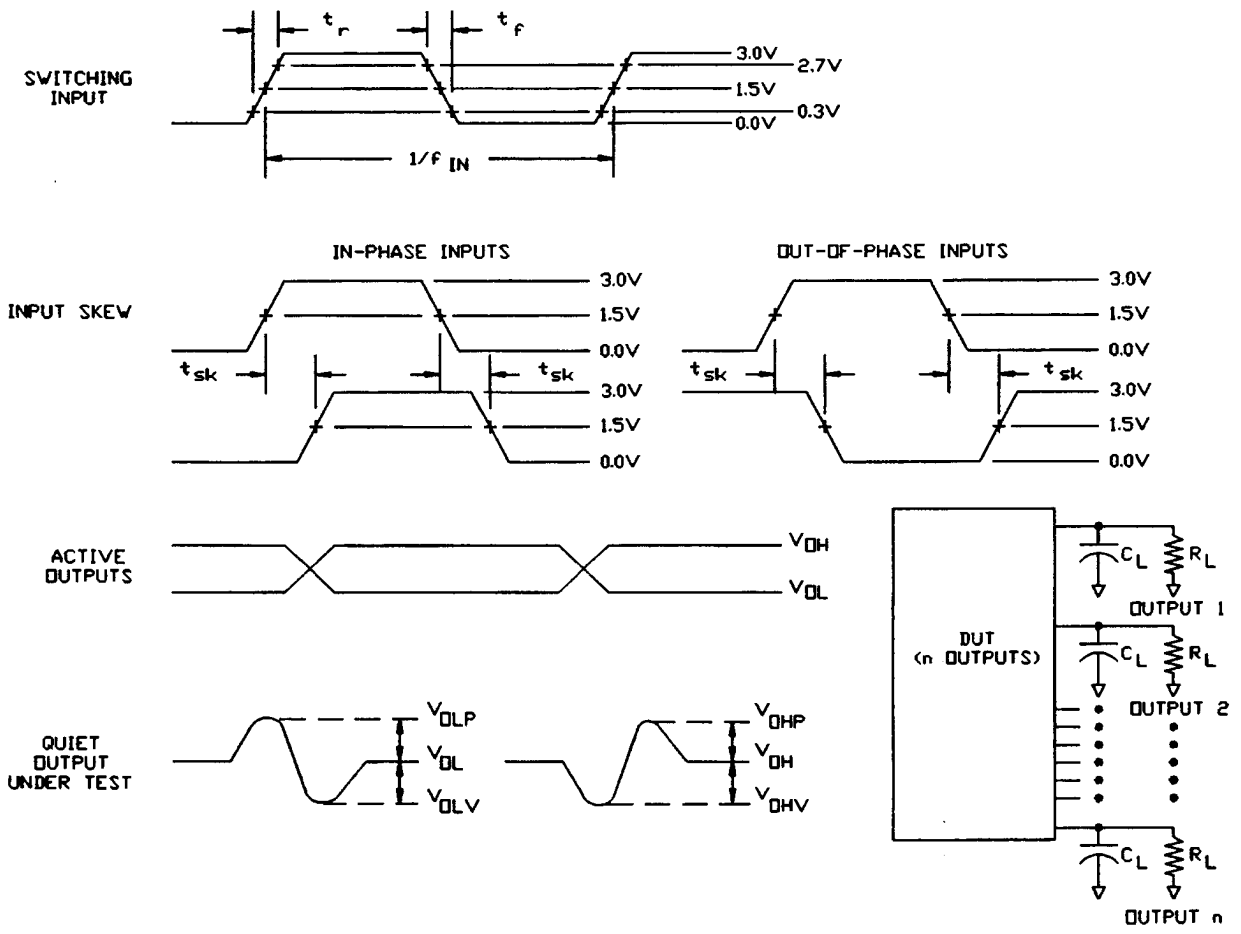


MSB → LSB

Instruction Code	Instruction
00000000	EXTEST
10000001	SAMPLE/PRELOAD
10000010	CLAMP
00000011	HIGHZ
All others	BYPASS

NOTE: For further information on bounbary-scan circuitry, see IEEE 1149.1.

FIGURE 4. Description of boundary-scan circuitry - Continued.



NOTES:
1. C_L includes a 47 pF chip capacitor (-0 percent, +20 percent) and at least 3 pF of equivalent capacitance from the test jig and probe.
2. R_L = 450Ω ±1 percent, chip resistor in series with a 50Ω termination. For monitored outputs, the 50Ω termination shall be the 50Ω characteristic impedance of the coaxial connector to the oscilloscope.
3. Input signal to the device under test:
   a. V_{IN} = 0.0 V to 3.0 V; duty cycle = 50 percent; $f_{IN} \geq 1$ MHz.
   b. t_r, t_f = 3 ns ±1.0 ns. For input signal generators incapable of maintaining these values of t_r and t_f, the 3.0 ns limit may be increased up to 10 ns, as needed, maintaining the ±1.0 ns tolerance and guaranteeing the results at 3.0 ns ±1.0 ns; skew between any two switching inputs signals (t_{sk}): ≤ 250 ps.

FIGURE 5. Ground bounce load circuit and waveforms.

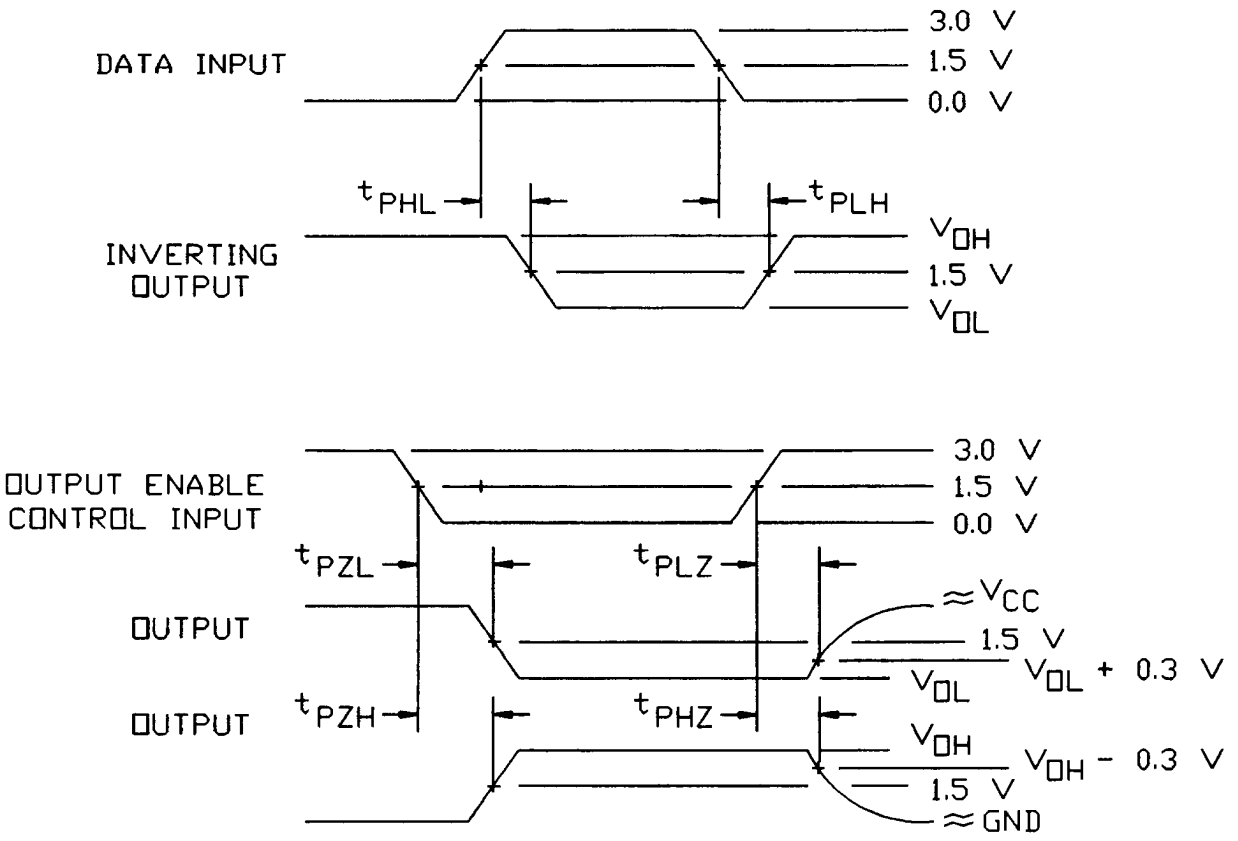


FIGURE 6. Switching waveforms and test circuit.

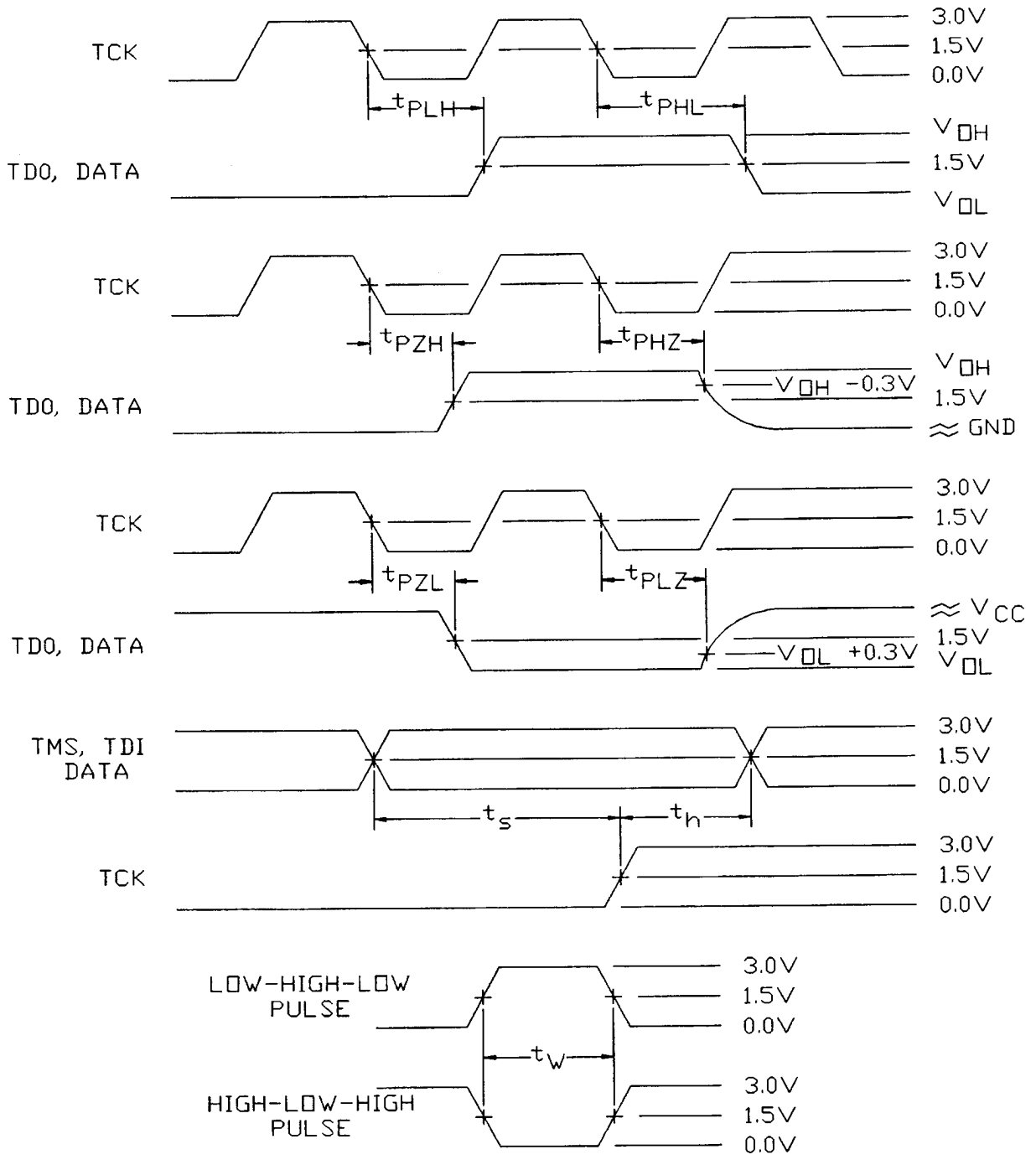
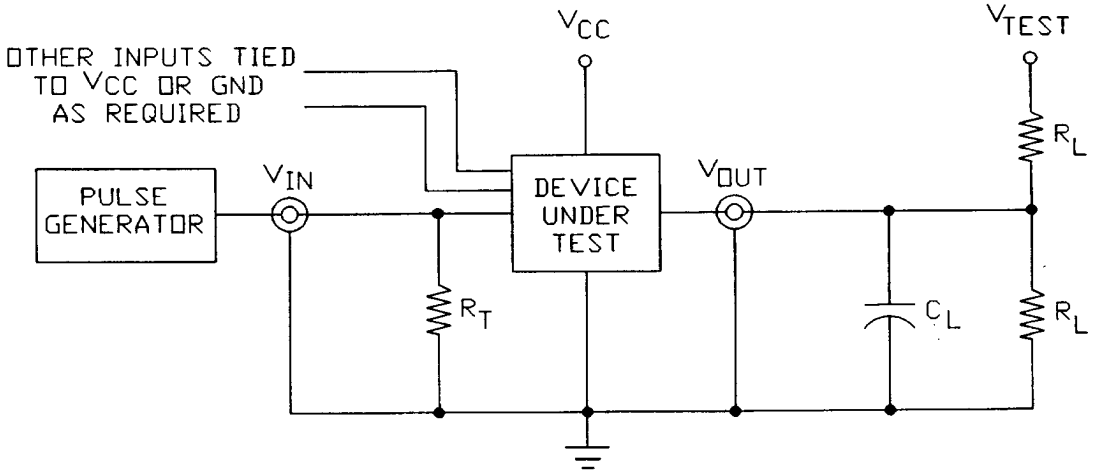


FIGURE 6. Switching waveforms and test circuit - Continued.



NOTES:
1. When measuring t_{PLZ} and t_{PZL}: V_{TEST} = 7.0 V.
2. When measuring t_{PHZ}, t_{PZH}, t_{PLH}, and t_{PHL}: V_{TEST} = open.
3. The t_{PZL} and t_{PLZ} reference waveform is for the output under test with internal conditions such that the output is at V_{OL} except when disabled by the output enable control. The t_{PZH} and t_{PHZ} reference waveform is for the output under test with internal conditions such that the output is at V_{OH} except when disabled by the output enable control.
4. C_L = 50 pF minimum or equivalent (includes test jig and probe capacitance).
5. R_L = 500Ω or equivalent.
6. R_T = 50Ω or equivalent.
7. Input signal from pulse generator: V_{IN} = 0.0 V to 3.0 V; PRR ≤ 10 MHz; t_r ≤ 3.0 ns; t_f ≤ 3.0 ns; t_r and t_f shall be measured from 0.3 V to 2.7 V and from 2.7 V to 0.3 V, respectively; duty cycle = 50 percent.
8. Timing parameters shall be tested at a minimum input frequency of 1 MHz.
9. The outputs are measured one at a time with one transition per measurement.

FIGURE 6. Switching waveforms and test circuit - Continued.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

(3) For device class M, unless otherwise noted, method 1015 of MIL-STD-883 shall be followed.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.3.1 Electrostatic discharge sensitivity qualification inspection . Electrostatic discharge sensitivity (ESDS) testing shall be performed in accordance with MIL-STD-883, method 3015. ESDS testing shall be measured only for initial qualification and after process or design changes which may affect ESDS classification.

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table in figure 2 herein. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table 15 in figure 2 herein. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

c. C_{IN}, C_{OUT}, and C_{PD} shall be measured only for initial qualification and after process or design changes which may affect capacitance. C_{IN} and C_{OUT} shall be measured between the designated terminal and GND at a frequency of 1 MHz. C_{PD} shall be tested in accordance with the latest revision of JEDEC Standard No. 20 and table I herein. For C_{IN}, C_{OUT}, and C_{PD}, test all applicable pins on five devices with zero failures.

For C_{IN} and C_{OUT}, a device manufacturer may qualify devices by functional groups. A specific functional group shall be composed of function types, that by design, will yield the same capacitance values when tested in accordance with table I herein. The device manufacturer shall set a functional group limit for the C_{IN} and C_{OUT} tests. The device manufacturer may then test one device function from a functional group to the limits and conditions specified herein. All other device functions in that particular functional group shall be guaranteed, if not tested, to the limits and conditions specified in table I herein. The device manufacturer shall submit to DESC-EC the device functions listed in each functional group and the test results for each device tested.

d. Ground and V_{CC} bounce tests are required for all device classes. These tests shall be performed only for initial qualification, after process or design changes which may affect the performance of the device, and any changes to the test fixture. V_{OLP}, V_{OLV}, V_{OHP}, and V_{OHV} shall be measured for the worst case outputs of the device. All other outputs shall be guaranteed, if not tested, to limits established for the worst case outputs. The worst case outputs tested are to be determined by the manufacturer. Test 5 devices assembled in the worst case package type supplied to this document. All other package types shall be guaranteed, if not tested, to limits established for the worst case package. The package type to be tested shall be determined by the manufacturer. The device manufacturer will submit to DESC-EC data that shall include all measured peak values for each device tested and detailed oscilloscope plots for each V_{OLP}, V_{OLV}, V_{OHP}, and V_{OHV} from one sample part per function. The plot shall contain the waveforms of both a switching output and the output under test.

Each device manufacturer shall test product on the fixtures they currently use. When a new fixture is used, the device manufacturer shall inform DESC-EC of this change and test the 5 devices on both the new and old test fixtures. The device manufacturer shall then submit to DESC-EC data from testing on both fixtures that shall include all measured peak values for each device tested and detailed oscilloscope plots for each V_{OLP}, V_{OLV}, V_{OHP}, and V_{OHV} from one sample part per function. The plot shall contain the waveforms of both a switching output and the output under test.

For V_{OLP}, V_{OLV}, V_{OHP}, and V_{OHV}, a device manufacturer may qualify devices by functional groups. A specific functional group shall be composed of function types, that by design, will yield the same capacitance values when tested in accordance with table I herein. The device manufacturer shall set a functional group limit for the V_{OLP}, V_{OLV}, V_{OHP}, and V_{OHV} tests. The device manufacturer may then test one device function from a functional group to the limits and conditions specified herein. All other device functions in that particular functional group shall be guaranteed, if not tested, to the limits and conditions specified in table I herein. The device manufacturer shall submit to DESC-EC the device functions listed in each functional group and the test results, along with the oscilloscope plots, for each device tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control of the device manufacturer's TRB in accordance with MIL-I-38535 and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-I-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	---	1	1
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 9 1/	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 2/
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3, 7, 8	1, 2, 3, 7, 8
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3, 7, 8	1, 2, 3, 7, 8
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be M, D, R, and H and RHA levels for device class M shall be M and D.

a. End-point electrical parameters shall be as specified in table II herein.

b. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-I-38535, appendix A, for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-I-38535 and MIL-STD-1331, and as follows:

GND	Ground zero voltage potential.
I_{CC}	Quiescent supply current.
I_{IL}	Input current low.
I_{IH}	Input current high.
T_C	Case temperature.
T_A	Ambient temperature.
V_{CC}	Positive supply voltage.
C_{IN}	Input terminal-to-GND capacitance.
C_{OUT}	Output terminal-to-GND capacitance.
C_{PD}	Power dissipation capacitance.
V_{IC+}	Positive input clamp voltage.
V_{IC-}	Negative input clamp voltage.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the three major microcircuit requirements documents (MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The three military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all three documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings.	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.