11. ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Condition	Ratings	Unit
Supply voltage	V_{DD}		-0.3 to +7.0	V
	V_{LOAD}		V_{DD}-40 to V_{DD}+0.3	V
	V_{PRE}		V_{DD}-12 to V_{DD}+0.3	V
Input voltage	V_I		-0.3 to V_{DD}+0.3	V
Output voltage	V_O	Other than display output pins	-0.3 to V_{DD}+0.3	V
	V_{OD}	Display output pins	V_{DD}-40 to V_{DD}+0.3	V
High-level output current	I_{OH}	1 pin other than display output pin	-15	mA
		1 pin of S0 to S9	-15	mA
		1 pin of T0 to T15	-30	mA
		Total of pins other than display output pins	-20	mA
		Total of display output pins	-120	mA
Low-level output current	I_L	1 pin	17	mA
		Total of all pins	60	mA
Total dissipation (Note 1) mW	P	Plastic QFP	450	mW
		Plastic shrink DIP	600	
Operating temperature	T_{opt}		-40 to +85	°C
Storage temperature	T_{stg}		-65 to +150	°C

Operating Voltage (Ta = -10 to +70°C)

Item	Condition	MIN.	MAX.	Unit
CPU (Note 2)		(Note 3)	6.0	V
FIP controller		4.5	6.0	V
Other hardware peripherals (Note 2)		2.7	6.0	V

Note 1. Calculation of total dissipation

Power is dissipated at the following three places in the uPD75268CW/GF and the sum of power dissipated at these places must not exceed the rated total power dissipation P_T, and, preferably, should be kept to within 80% of P_T.

① Power dissipated by CPU = V_{DD} (max.) x I_{DD1} (max.)

② Power dissipated by output pins (differs depending on whether ordinary signals or display signals are output. Add the power dissipated when the maximum current is allowed to flow into each output pin to the power dissipated by 1 and 2 .)

③ Power dissipated by pull-down resistor internally connected by a mask option.

Example: When a 9-segment x 11-digit FIP and four LEDs are used at V_{DD} = 5V+10% at a 4.19 MHz oscillation frequency, a current of up to 3 mA flows through the segment pins, up to 15 mA through the timing pins, and up to 10 mA through the LED output pins.

① Power dissipated by CPU = 5.5 V x 9.0 mA = 49.5 mW

② Power dissipated by:

segment pins = 2 V x 3 mA x 9 pins = 54 mW

timing pins = 2 V x 15 mA = 30 mW

LED output pins = (10/15 x 2 V) x 10 mA x 4 pins = 53 mW

③ Power dissipated by pull-down resistors = (30 + 5.5 V)^2/40 kΩ x 10 pins = 315 mW

Therefore,
PT = ① + ② + ③ = 501.5 mW

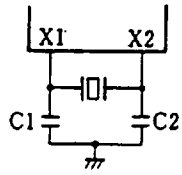
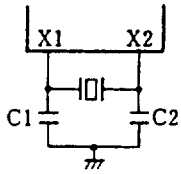
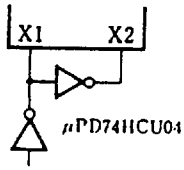
Because the permissible total power dissipation of the shrink DIP version of the microcomputer is 600 mW, the power dissipation of 501.5 mW calculated in the above example is permissible. With the QFP version, however, it should be reduced to less than 450 mW, which is the rated power dissipation of the FLAT package. To reduce the power dissipation, decrease the number of internally-connected pull-down resistors. Therefore, in the above example, the power dissipation can be reduced down to 344 mW by internally connecting the pull-down resistors to only 11 digit output pins and 4 segment output pins and by connecting external pull-down resistors to the other digit and segment pins.

2. Excluding the system clock oscillation circuit and FIP controller.

3. The operating voltage range differs depending on the cycle time. Refer to AC Characteristics.

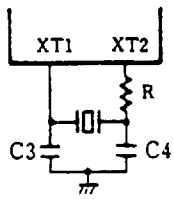
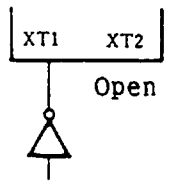
Main System Clock Oscillation Characteristics

(Ta = -40 to +85°C, V_{DD} = 2.7 to 6.0V)

Oscillator	Recommended constants	Item	Conditions	MIN.	TYP.	MAX.	Unit
(Note 3) Ceramic resonator		(Note 1) Oscillation frequency (f_{XX})	VDD = oscillation voltage range	2.0		5.0	MHz
		(Note 2) Oscillation stabilization time	After V_{DD} reaches the minimum value in the oscillator operating voltage range			4	ms
(Note 3) Crystal resonator		(Note 1) Oscillation frequency (f_{XX})		2.0	4.19	5.0	MHz
		(Note 2) Oscillation stabilization time	V_{DD} = 4.5 to 6.0V			10	ms
						30	ms
External clock		(Note 1) X1 input frequency (f_X)		2.0		5.0	MHz
		X1 input high/low level width (t_{XH}, t_{XL})		100		250	ns

Subsystem Clock Oscillator Characteristics

(Ta = -40 to +85°C, V_{DD} = 2.7 to 6.0V)

Oscillator	Recommended constants	Item	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		(Note 1) Oscillation frequency (f_{XT})		32	32.768	35	kHz
		(Note 2) Oscillation stabilization time	V_{DD}=4.5 to 6.0V		1.0	2	s
						10	s
External clock		XT1 input frequency (f_{XT})		32		100	kHz
		XT1 input high/low level width (t_{XTH}, t_{XTL})		10		32	us

Note 1: The oscillation frequency and input frequency are indicated only to express the characteristics of the oscillator. Refer to the AC characteristics for instruction execution time.

2: The oscillation stabilization time is the time required for the oscillator to stabilize after V_{DD} is applied or after the STOP mode is released.

3: Use of the following oscillators is recommended.

Capacitance (Ta = 25°C, V_{DD} = 0V)

Item		Symbol	Condition	MIN.	TYP.	MAX.	Units
Input capacitance		C_{IN}	f=1 MHz with pins other than that measured at 0V			15	pF
Output capacitance	Other than display output pins	C_{OUT}				15	pF
	Display output pins					35	pF
Input/output capacitance		C_{IO}				15	pF

Recommended oscillator circuit constant

Main system clock: ceramic resonator (Ta = -40 to +85°C)

Manufacturer	Product	External capasitance (pF)		Oscillation voltage range (V)		Remark
		C1	C2	MIN.	MAX.	
Kyocera	KBR-2.0MS KBR-4.0MS	47 33	47 33	2.7	6.0	
Murata Manufacturing	CSA 2.00MG CSA 4.19MG	30	30	2.7	6.0	
	CST 2.00MG CST 4.19MGW	Not offered	Not offered			C-contained type

Subsystem clock: 32.768kHz Crystal resonator (Ta = -10 to +60°C)

Manufacturer	Product	External circuit constant			Oscillation voltage range		Remark
		C3 (pF)	C4 (pF)	R (kΩ)	MIN. (V)	MAX. (V)	
Kinseki	P-3	15	22	330	2.7	6.0	

DC Characteristics (Ta = -40 to +85°C, V_{DD}=2.7 to 6.0V)

Item	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
High-level input voltage	V_{IH1}	Other than below		$0.7V_{DD}$		V_{DD}	V
	V_{IH2}	Ports 0 and 1, and $\overline{RESET}$		$0.75V_{DD}$		V_{DD}	V
	V_{IH3}	X1, X2, XT1		V_{DD}-0.4		V_{DD}	V
	V_{IH4}	Port 6	V_{DD}=4.5 to 6.0V	$0.65V_{DD}$		V_{DD}	V
				$0.7V_{DD}$		V_{DD}	V
Low-level input voltage	V_{IL1}	Other than below		0		$0.3V_{DD}$	V
	V_{IL2}	Ports 0, 1, 6 and $\overline{RESET}$		0		$0.2V_{DD}$	V
	V_{IL3}	X1, X2, XT1		0		0.4	V
High-level output voltage	V_{OH}	All output pins	V_{DD}=4.6 to 6.0V, I_{OH}=-1mA	V_{DD}-1.0			V
			I_{OH}=-100uA	V_{DD}-0.5			V
Low-level output voltage	V_{OL}	Ports 4 and 5	V_{DD}=4.5 to 6.0V, I_{OL}=15mA		0.4	2.0	V
		All output pins	V_{DD}=4.5 to 6.0V, I_{OL}=1.6mA			0.4	V
			I_{OL}=400uA			0.5	
High-level input leakage current	I_{LIH1}	Other than X1, X2, and XT1	V_{IN}= V_{DD}			3	uA
	I_{LIH2}	X1, X2, XT1				20	uA
Low-level input leakage current	I_{LIL1}	Other than X1, X2, and XT1	V_{IN}= 0 V			-3	uA
	I_{LIL2}	X1, X2, XT1				-20	uA

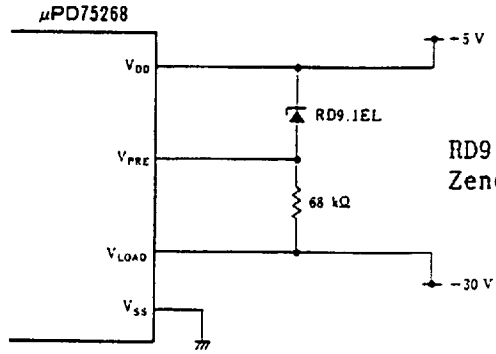
(Cont'd)

Item	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
High-level output leakage current	I_{LOH}	All output pins	$V_{OUT}=V_{DD}$				3	uA
Low-level output leakage current	I_{LOL1}	Other than display output pins	V_{OUT}= 0 V				-3	uA
	I_{LOL2}	display output pins	$V_{OUT}=V_{LOAD}=V_{DD}-35V$				-10	uA
Display output current	I_{OD}	S0-S9	V_{DD}= 4.5 to 6.0V V_{OD}= V_{DD}-2V	(Note 1) $V_{PRE}=V_{DD}$ -9±1V	-3	-5.5		mA
				V_{PRE}=0V	-1.5	-3.5		mA
		T0-T15		(Note 1) V_{PRE}=VDD -9+1V	-15	-22		mA
				V_{PRE}=0V	-7	-15		mA
Internal pull-down resistor (mask option)	R_{P6}	Port 6 $V_{IN}=V_{OD}$	V_{DD}=4.5 to 6.0V		20	80	200	kΩ
					20		1000	kΩ
	R_L	Display output pins	$V_{DD}-V_{LOAD}$=35V		25	70	135	kΩ

(Cont'd)

Item	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
(Note 2) Supply current	I_{DD1}	4.19MHz crystal oscil-lator C1=C2 =15pF	(Note 3) V_{DD}=5V±10%		3.0	9.0	mA
			(Note 4) V_{DD}=3V±10%		0.55	1.5	mA
	I_{DD2}		HALT mode V_{DD}=5V±10%		600	1800	uA
			V_{DD}=3V±10%		200	600	uA
	I_{DD3}	(Note 5) 32 kHz crysral oscil-lator	V_{DD}=3V±10%		40	120	uA
	I_{DD4}		HALT mode V_{DD}=3V±10%		5	15	uA
	I_{DD5}	XT1=0V STOP mode	V_{DD}=5V±10%		0.5	20	uA
			V_{DD}=3V±10%		0.1	10	uA

Note 1: Use of the following external circuit is recommended.



RD9.1EL: Zener diode (NEC)
Zener voltage: 8.29 to 9.30 V

2: Excluding the current following through the internal pull-down resistor.

3: When the processor clock control register (PCC) is set to 0011 and operated in the high-speed mode.

4: When the PCC register is set to 0000 and operated in the low-speed mode.

5: When the system clock control register (SCC) is set to 1001 and operated on the subsystem clock with oscillation of the main system clock stopped.

AC Characteristics (Ta = -40 to +85°C, V_{DD} = 2.7 to 6.0 V)

AC Characteristics (Ta = -40 to +85°C, V_{DD} = 2.7 to 6.0 V)

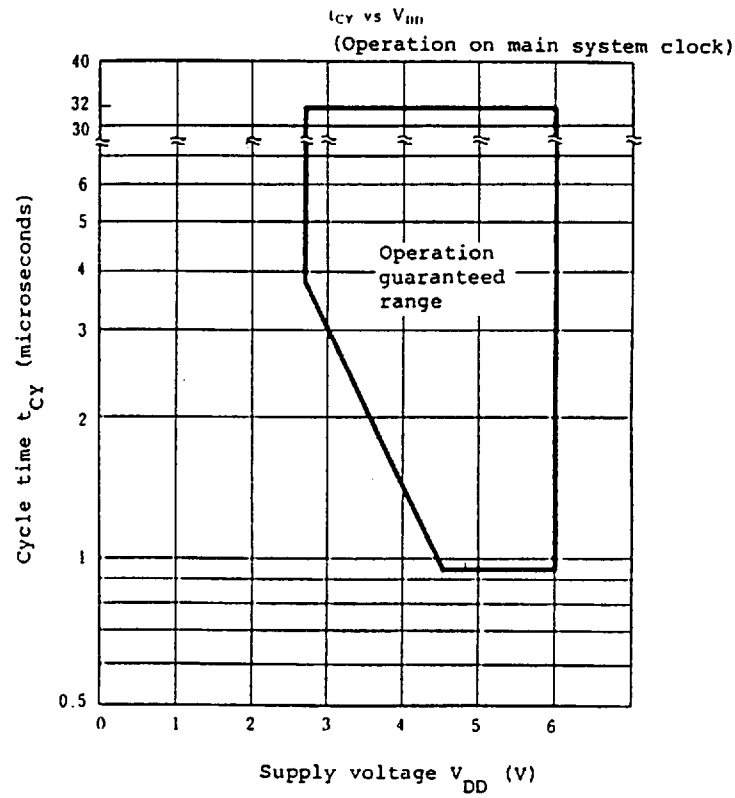
Item	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
(Note 1) Cycle time (minimum instruction execution time	t_{CY}	Operation on main system	V_{DD}=4.5 to 6.0V	0.95		32	us
				3.8		32	us
		Operation on sub-system clock		114	122	125	us
TI0 input frequency	f_{TI}	V_{DD}=4.5 to 6.0V		0		0.6	MHz
				0		165	kHz
TI0 input high & low-level width	t_{THI}, t_{TIL}	V_{DD}=4.5 to 6.0V		0.83			us
				3			us
$\overline{SCK}$ cycle time	t_{KCY}	V_{DD}=4.5 to 6.0V	Input	0.8			us
			Output	0.95			us
			Input	3.2			us
			Output	3.8			us
$\overline{SCK}$ high & low-level width	t_{KH}, t_{KL}	V_{DD}=4.5 to 6.0V	Input	0.4			us
			Output	$t_{KCY}/2-50$			ns
			Input	1.6			us
			Output	$t_{KCY}/2-150$			ns
SI setup time (vs. $\overline{SCK}$ ↑)	t_{SIK}			100			ns
SI hold time (vs. $\overline{SCK}$ ↑)	t_{KSI}			400			ns
$\overline{SCK}$ ↓ – SO output delay time	t_{KSO}					300	ns
						1000	ns

(Cont'd)

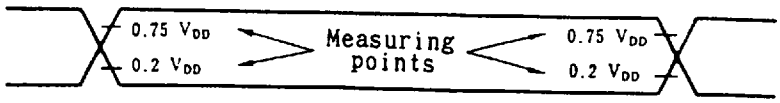
Item	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Interrupt input low & high-leevel width	t_{INTH}, t_{INTL}		INT0	(Note 2)			us
			INT1	$2t_{CY}$			us
			INT2,4	10			us
$\overline{RESET}$ low-level width	t_{RSL}			10			us

Note 1: The cycle time (minimum instruction execution time) is determined by the oscillation frequency of the oscillator connected to the microcomputer, system clock control register (SCC), and processor clock control register (PCC). The chart on the right shows the characteristics of cycle time t_{CY} vs. supply voltage V_{DD} when the microcomputer operates on the main system clock.

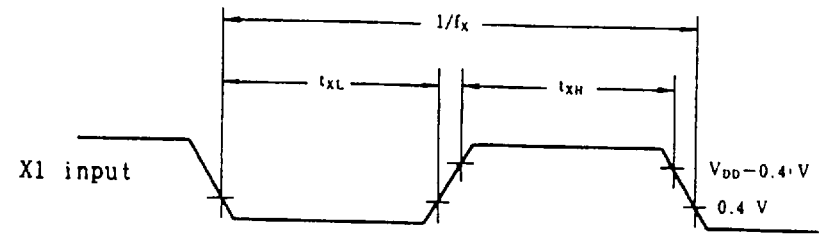
2: $2t_{CY}$ or $128/f_{XX}$, depending on the setting of the interrupt mode register (IM0)

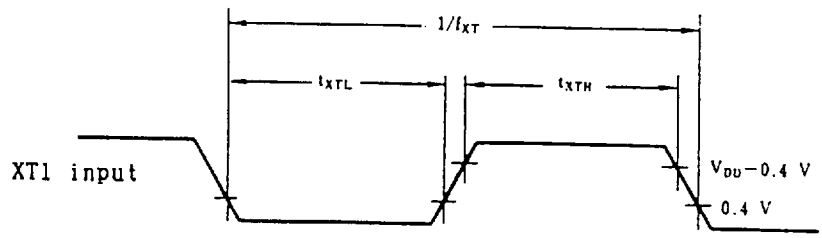


AC Timing Measured Values (excluding X1 and XT1 input pins)

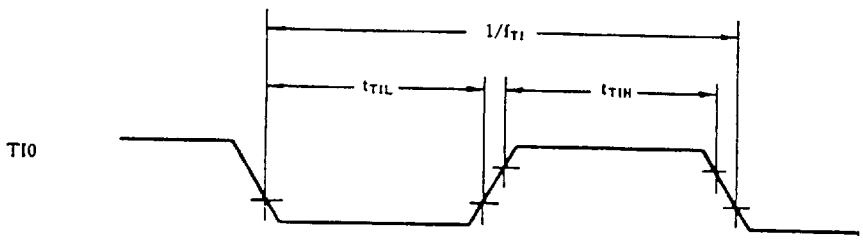


Clock Timing

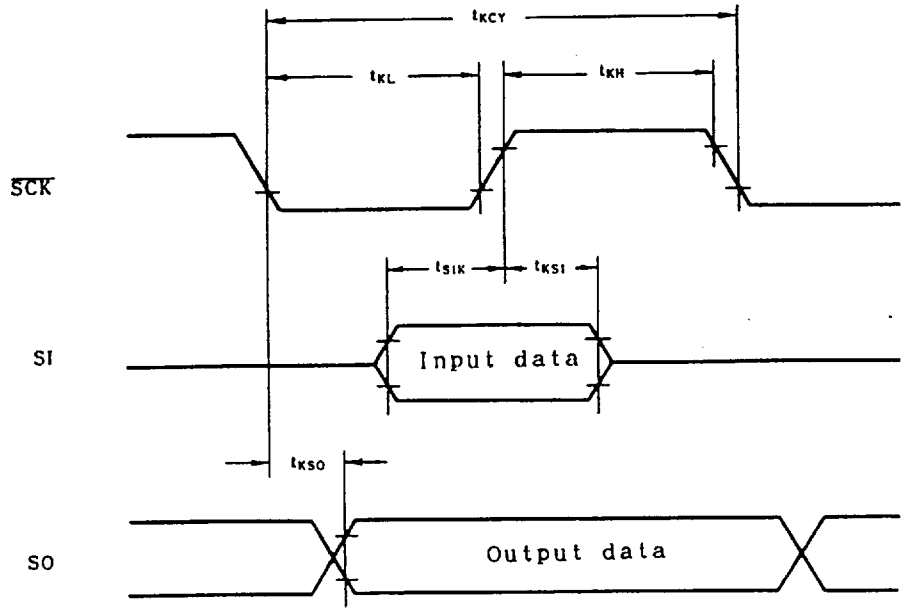




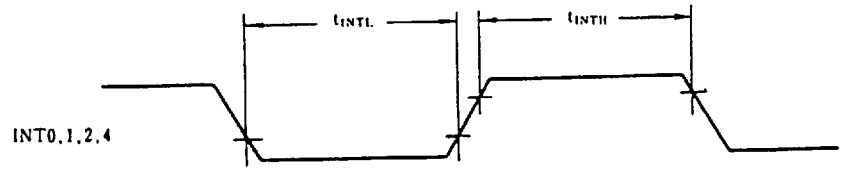
TI0 Timing



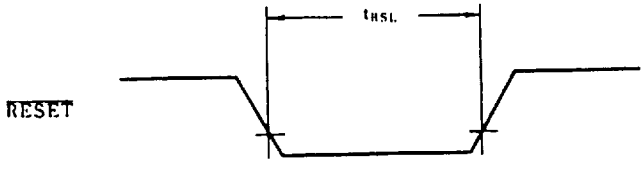
Serial Transfer Timing



Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



Data memory STOP mode low voltage data retention characteristic
(Ta = -40 to +85°C)

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention voltage	V_{DDDR}		2.0		6.0	V
Data retention current (Note1)	I_{DDDR}	V_{DDDR}=2.0V		0.1	10	uA
Release signal set time	t_{SREL}		0			us
Oscillation stabilization wait time (Note2)	t_{WAIT}	Release by $\overline{RESET}$ input		$2^{17}/f_X$		ms
		Release by interrupt request		Note3		ms

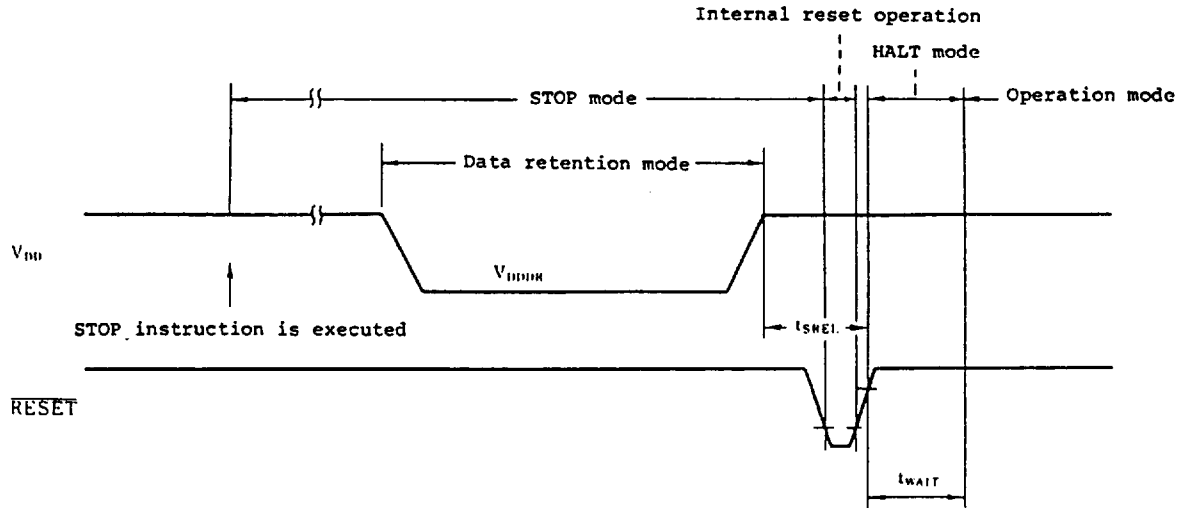
Note 1: Excluding current flowing through the internal pull-down resistors and power-ON reset circuit (Mask option).

2: Oscillation stabilization wait time is the time during which the CPU is stopped to prevent it unstable operation when oscillation is started.

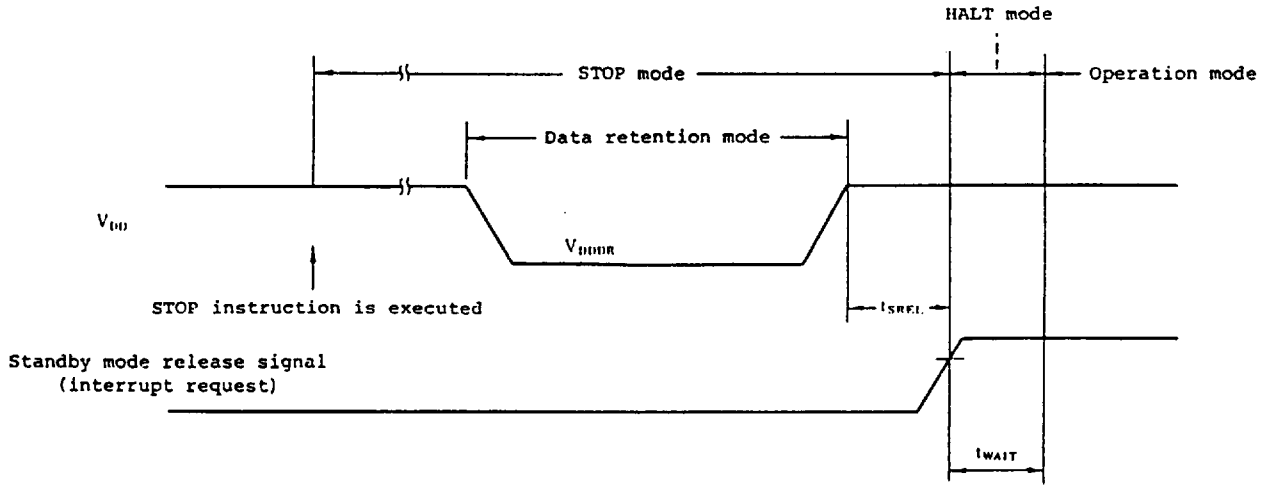
3: Depends on the setting of the basic interval timer mode register (BTM), as follows:

BTM3	BTM2	BTM1	BTM0	WAIT time ( ) indicates f_{XX}=4.19MHz
-	0	0	0	$2^{20}/f_{XX}$ (Approximately 250 ms)
-	0	1	1	$2^{17}/f_{XX}$ (Approximately 31.3 ms)
-	1	0	1	$2^{15}/f_{XX}$ (Approximately 7.82 ms)
-	1	1	1	$2^{13}/f_{XX}$ (Approximately 1.95 ms)

Data Retention Timing (when STOP mode is released by $\overline{\text{RESET}}$)

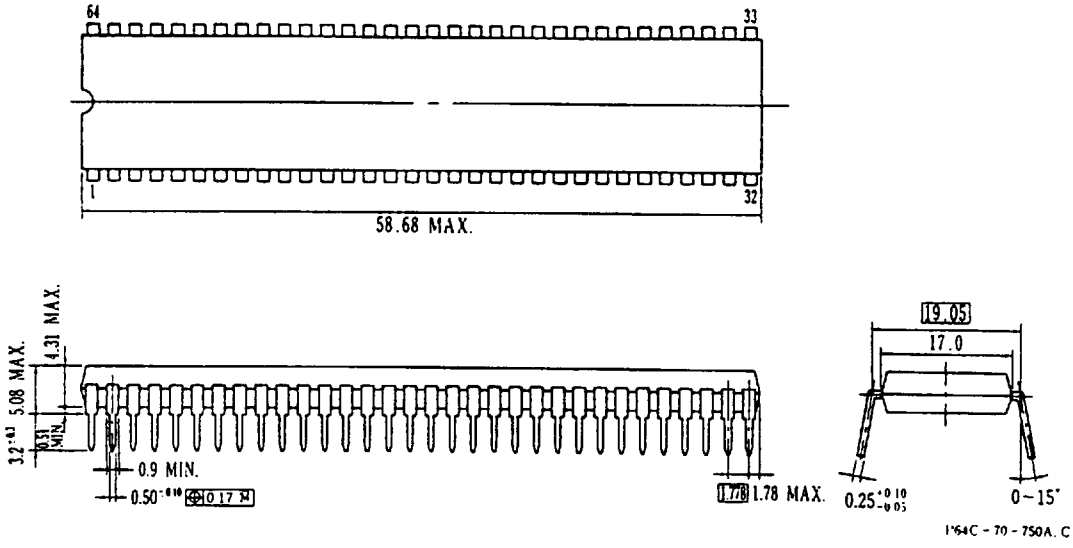


Data Retention Timing
(Standby release signal: when STOP mode is released by interrupt signal)

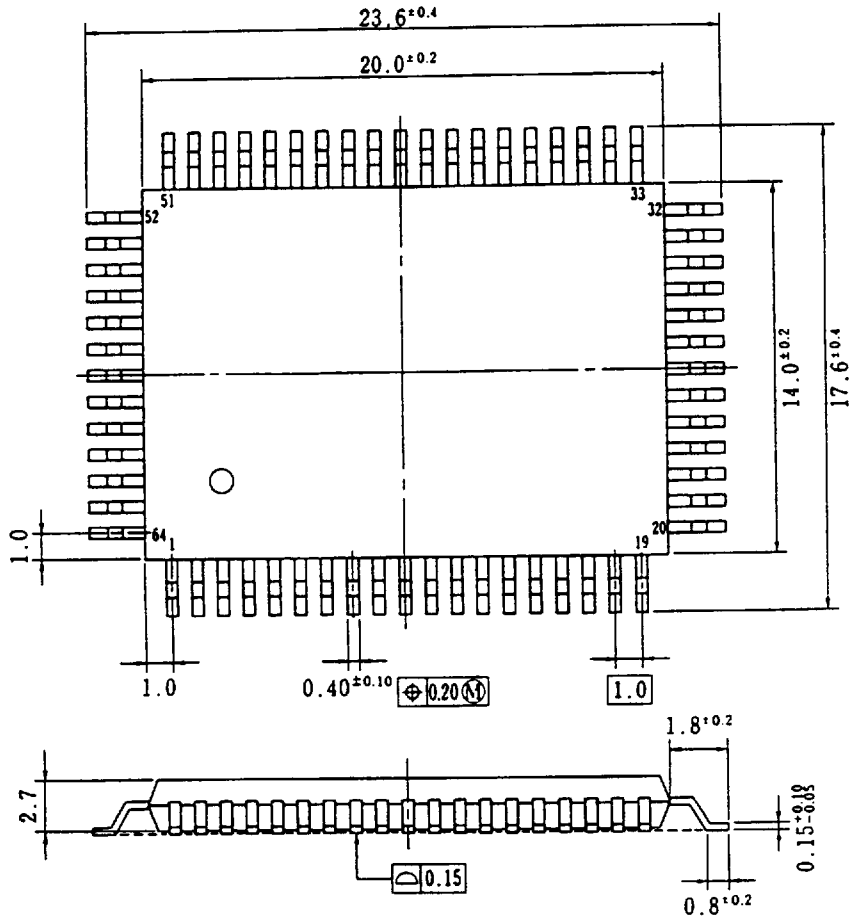


12. EXTERNAL DIMENSIONS

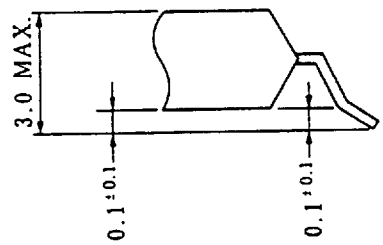
64-Pin Plastic Shrink DIP (750 mil) Dimensions (Unit: mm)



64-Pin Plastic QFP (14 x 20) Dimensions (Unit: mm)

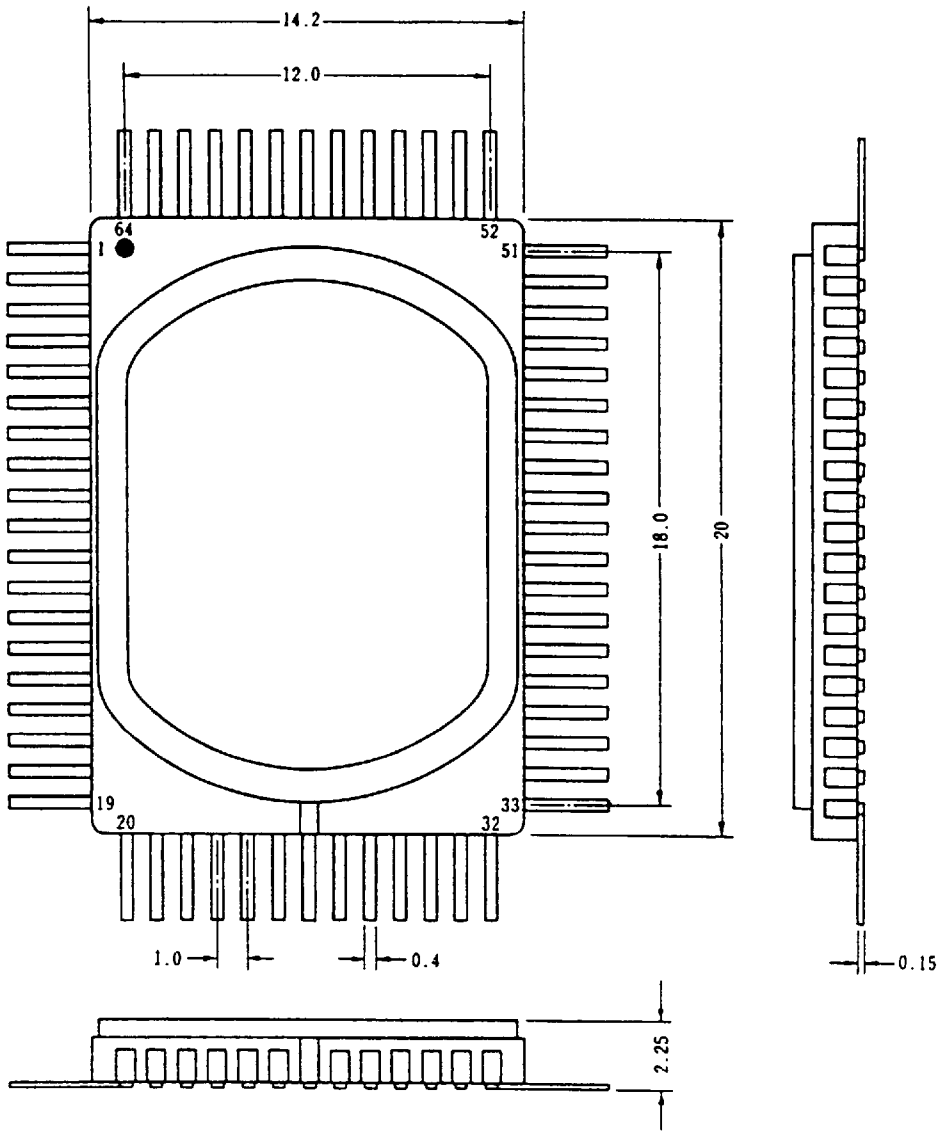


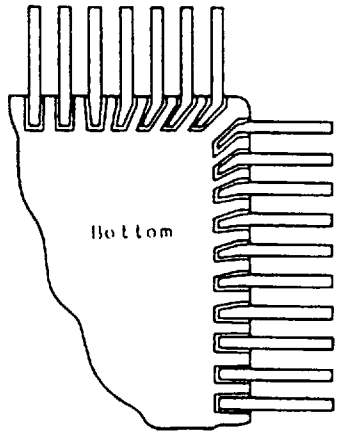
Detailed pin configuration



P64GF-100-3B8, 3BE-1

64-Pin Ceramic QFP for ES (reference) (Unit: mm)





Note 1. The metal cap is connected to pin 26 and is thus at positive potential.

2. The leads are diagonally molded into the bottom of the package.

3. The length of the leads may vary slightly because the tolerances for the lead cutting process are not critical/not highly controlled.