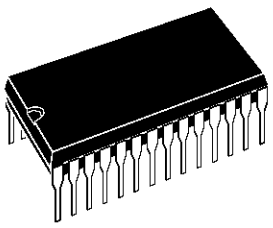
SGS-THOMSON MICROELECTRONICS

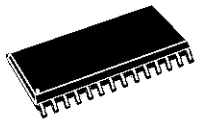
ST72E94
ST72T94

8-BIT HCMOS MCU WITH 6K EPROM, EEPROM AND 16-BIT TIMER WITH INPUT CAPTURE AND OUTPUT COMPARE

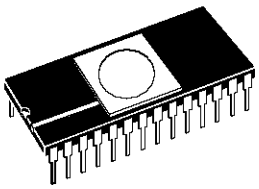
- 3.0 to 5.5V Supply Operating Range
- 4MHz Maximum Clock Frequency
- Fully Static operation
- -40° to +85°C Operating Temperature Range
- Run, Wait, Stop and RAM Retention modes
- User EPROM: 6,144 bytes
- Data RAM: 224 bytes
- EEPROM: 256 bytes
- 28 pin Dual-in-Line and SO plastic packages for ST72T94 OTP version
- 28 pin Ceramic Dual-in-Line package for ST72E94 EPROM version
- 22 Bidirectional I/O lines
- 6 Interrupt Wake-Up programmable input lines
- 16-bit Timer with Input Capture and dual Output Compare
- 2V RAM Data Retention mode
- Master Reset and Power-On Reset
- Compatible with ST7294 (6K) and ST7293 (3.25K) ROM devices
- 8-bit Data Manipulation
- 63 Basic Instructions
- 17 main Addressing Modes
- 8x8 Unsigned Multiply instruction
- True Bit Manipulation
- Complete Development Support on PC/DOS Real-Time Emulator
- Full Software Package (Cross-Assembler, Debugger)



PDIP28



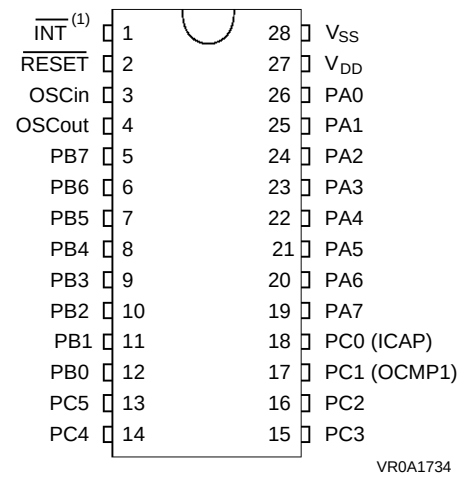
PSO28



CDIP28W

(See end of Datasheet for Ordering Information)

Figure 1. Pin Description



Note 1. This pin is also the V_{PP} input for EPROM based devices

1 GENERAL DESCRIPTION

1.1 INTRODUCTION

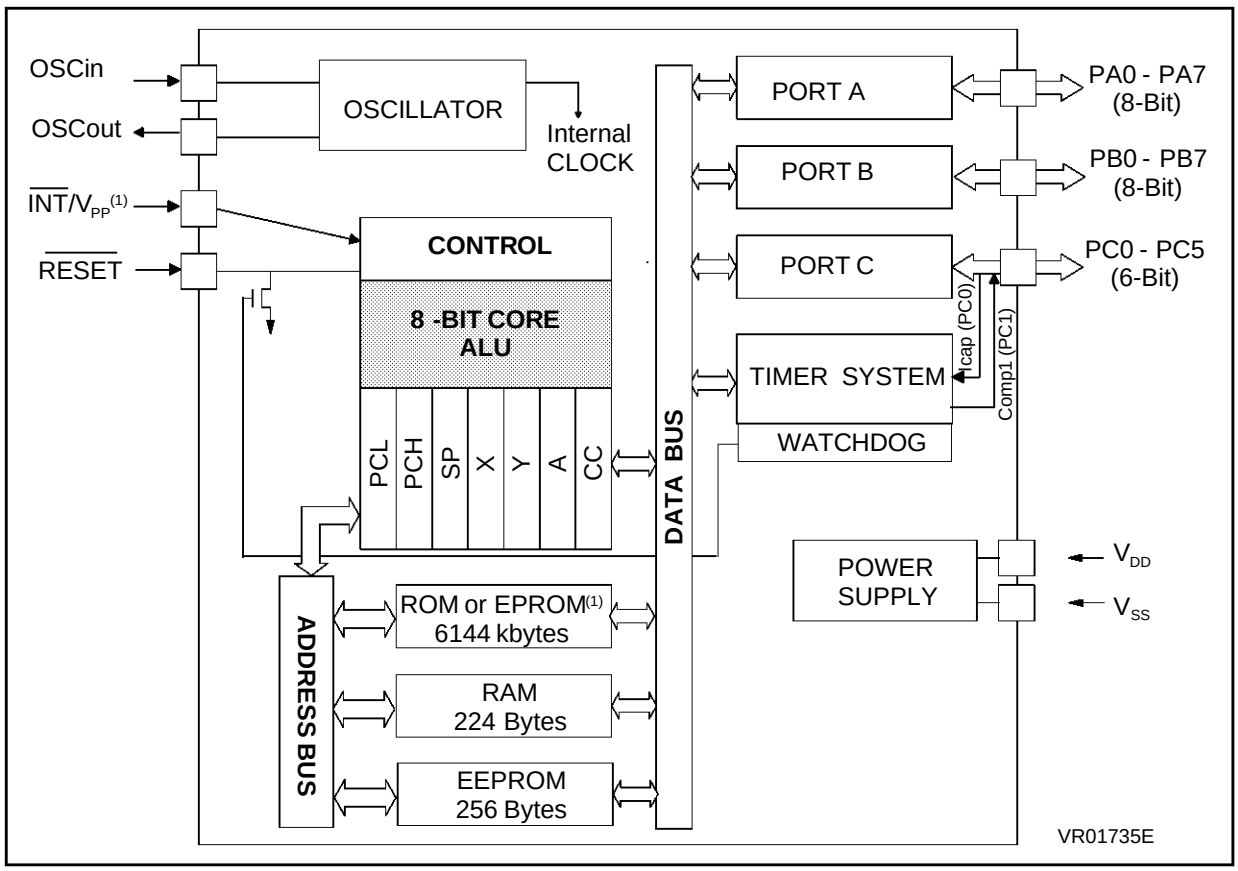
The ST72E94 and ST72T94 (following mentioned as ST72E94) are EPROM members with EEPROM of the ST72 family of microcontrollers, in windowed ceramic (E) and plastic OTP (T) packages respectively, completely developed and produced by SGS-THOMSON Microelectronics using a n-well proprietary HCMOS process. The EPROM parts are fully compatible with their ROM versions and this datasheet will thus provide only information specific to the EPROM based devices.

THE READER IS ASKED TO REFER TO THE DATASHEET OF THE ST7294 AND ST7293 ROM-BASED DEVICES FOR FURTHER DETAILS.

The ST72E94 is an user-programmable and erasable device. It is best suited for development. The ST72T94 is a One-Time Programmable device (OTP). It offers the best cost/flexibility trade-off for prototyping and preseries as well as most low to medium volume applications.

The ST72E94 and ST72T94 are HCMOS microcontrollers from the ST72 family. They are based around an 8-bit core industry standard and offers an enhanced instruction set. The processor runs with an external clock at 4 MHz with a 5V supply and 2MHz with a 3V supply. Due to the fully static design of this device, operation down to DC is possible. Under software control the ST72E94 and ST72T94 can be placed in WAIT or HALT mode thus reducing power consumption. The enhanced instruction set and addressing modes afford real programming potential. In addition to standard 8 bit data management the ST72E94 and ST72T94 feature true bit manipulation, 8x8 unsigned multiplication and indirect addressing modes. The devices include an on-chip oscillator, CPU, EPROM, RAM, EEPROM, I/O, and one timer with 1 input capture and 2 output compare systems.

Figure 2. ST72E94 Block Diagram



Note 1. EPROM version only

1.2 PIN DESCRIPTION

V_{DD}. Power supply.

V_{SS}. Ground.

OSCin, OSCout. Oscillator input and output pins. These pins are to be connected to a parallel resonant crystal or ceramic resonator. An external clock source can also be input through OSCin.

$\overline{\text{RESET}}$. The active low input signal forces the initialisation of the MCU. This event is the first priority interrupt. This pin is switched output low when the Watchdog has released. It could be used to reset external peripherals.

$\overline{\text{INT}}$/V_{PP}. is the external interrupt signal. Software configuration allows four triggering modes. In the EPROM programming mode, this pin acts as the programming voltage input V_{PP}.

ICAP (PC0). Input capture signal going to the TIMER system. This signal, according to a mask option, can be an ICAP pin or PC0 pin. When PC0 is defined as ICAP, the internal pull-up resistor is not connected.

OCMP1 (PC1). Output compare signal coming from the TIMER system. This output signal, according to a mask option, can be an OCMP1 pin (for output compare 1 of the timer) or PC1 pin. When PC1 is defined as OCMP1, the internal pull-up resistor is not connected.

PA0-PA7, PB0-PB7, PC0-PC5. These 22 lines are standard I/O lines, programmable as either input or output.

– PORT A. 8 Standard I/O lines, bit programmable, accessed through DDRA and DRA Registers. According to a mask option, the outputs can be defined as a standard push-pull output port or as an open drain output port. According to another mask option, a pull-up resistor can be added on each line when it is defined as an input.

– PORT B. 8 Standard I/O lines bit programmable accessed through DDRB and DRB Registers. According to another mask option, a pull-up resistor can be added on each line when it is defined as an input.

– PORT C. 6 Standard I/O lines accessed through DDRC and DRC Registers. According to a mask option, these 6 lines can become 6 falling edge sensitive interrupt lines all linked to a single interrupt vector or 6 standard input ports tied to V_{DD} through an internal pull-up resistor. These negative edge sensitive interrupt lines can wake-up the ST72E94 from WAIT or HALT mode. This feature allows to build low power applications when the ST72E94 can be waken-up from keyboard push.

PIN DESCRIPTION (Continued)

Table 1. ST72E94 Pin Configuration

Name	Function	Description	Pin Assignment
$\overline{INT}/V_{PP}$	I	Interrupt / EPROM Programming Voltage	1
$\overline{RESET}$	I/O	Reset	2
OSCin	I	Oscillator	3
OSCout	O	Oscillator	4
PB7	I/O	Standard Port (bit programmable)	5
PB6	I/O	Standard Port (bit programmable)	6
PB5	I/O	Standard Port (bit programmable)	7
PB4	I/O	Standard Port (bit programmable)	8
PB3	I/O	Standard Port (bit programmable)	9
PB2	I/O	Standard Port (bit programmable)	10
PB1	I/O	Standard Port (bit programmable)	11
PB0	I/O	Standard Port (bit programmable)	12
PC5	I/O	Standard Port (falling edge interrupt line)	13
PC4	I/O	Standard Port (falling edge interrupt line)	14
PC3	I/O	Standard Port (falling edge interrupt line)	15
PC2	I/O	Standard Port (falling edge interrupt line)	16
PC1 (OCMP1)	I/O	Standard Port (falling edge interrupt line or timer output compare)	17
PC0 (ICAP)	I/O	Standard Port (falling edge interrupt line or timer input capture)	18
PA7	I/O	Standard Port (bit programmable)	19
PA6	I/O	Standard Port (bit programmable)	20
PA5	I/O	Standard Port (bit programmable)	21
PA4	I/O	Standard Port (bit programmable)	22
PA3	I/O	Standard Port (bit programmable)	23
PA2	I/O	Standard Port (bit programmable)	24
PA1	I/O	Standard Port (bit programmable)	25
PA0	I/O	Standard Port (bit programmable)	26
V_{DD}	I/O	Power Supply	27
V_{SS}	I/O	Ground	28

1.3 MEMORY MAP

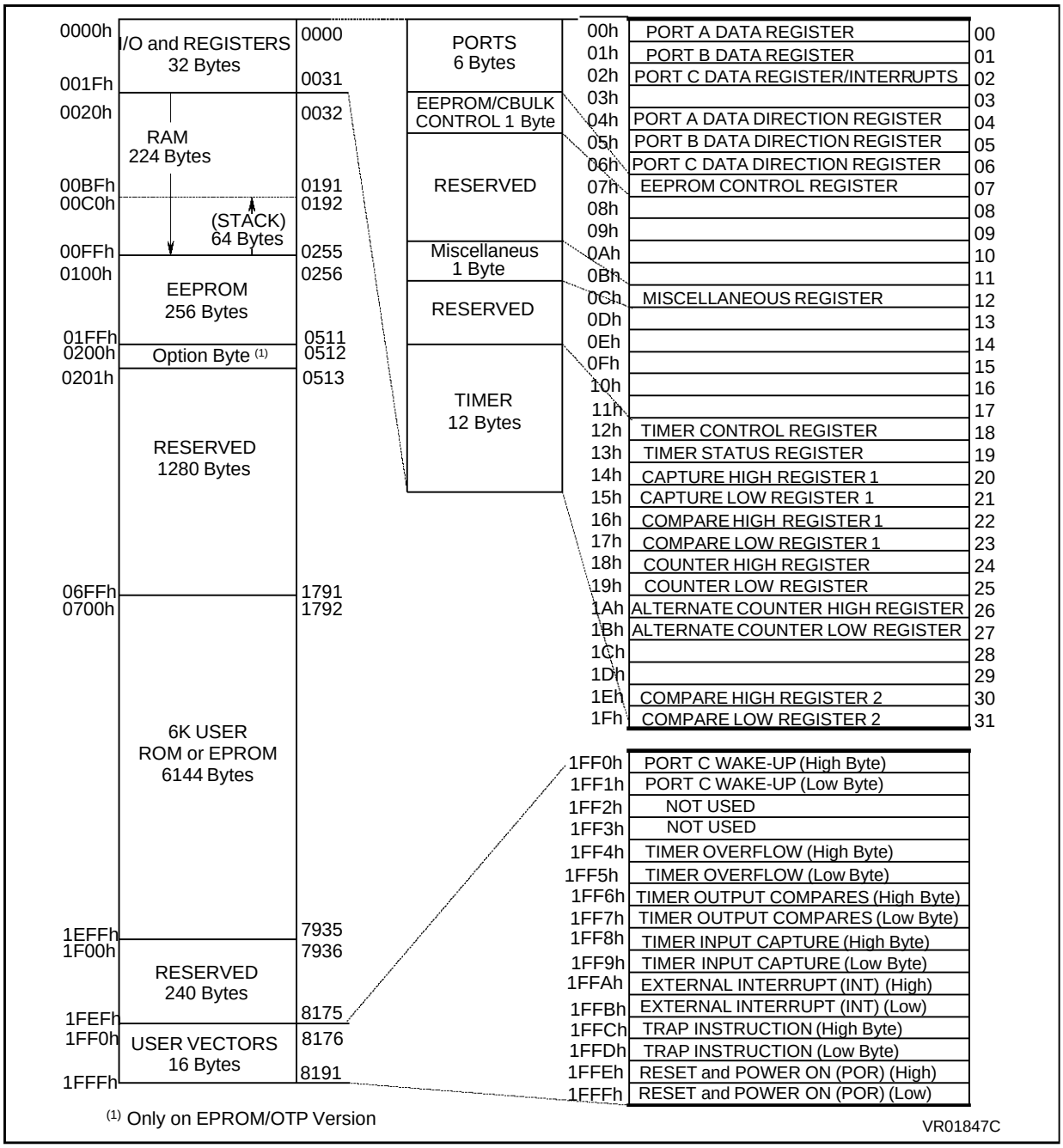
As shown in Figure 3, the MCU is capable of addressing 8192 bytes of memory and I/O registers. In the ST72E94, 7696 of these bytes are user accessible.

Note:
In the ST7293 only 3.25K bytes are user accessible. This should be taken into account by the user when programming the ST72E94 to emulate the ST7293.

The locations consist of 32 bytes of I/O registers (only 20 are used), 224 bytes of RAM, 256 bytes of EEPROM and 6Kbytes of user ROM. The RAM space includes 64 bytes for the stack from 0FFh to 0C0h. Programs that only use a small part of the allocated stack locations for interrupts and/or subroutine stacking purpose can use the remaining bytes as standard RAM locations.

The highest address bytes contains the user defined reset and interrupt vectors.

Figure 3. Memory Map



1.4 OPTION BYTE

An additional mode is used to configure the part for programming of the EPROM. This is set by a +12.5 voltage applied to the $\overline{INT}/V_{PP}$.

The EPROM memory may be programmed by using the EPROM Programming Boards (EPB) available from SGS-THOMSON.

The ROM devices of the ST72 family can be configured through mask options. In EPROM devices, most mask options are replaced by EPROM bits grouped in the Option Byte. The configuration of the device is made by programming the Option Byte.

The Option Byte is not in the user memory space. The Option Byte is accessed only if the device is in programming mode and location 0200h is addressed. The EPB provides all the functionality to select and program the Option Byte.

7							0
WIW	WDMS	PBIP	PCWS	PC1S	PC0S	PA0S	PAIP

b7 = **WIW**: *Watchdog in Wait.*
1 : Watchdog suspended during Wait
0 : Watchdog active during Wait

b6 = **WDMS**: *Watchdog Enable Mode*.
1 : Watchdog in Software Select Mode
0 : Watchdog in auto-enable Mode

b5 = **PBIP**: *Port B Input Pull-up.*
1 : Pull-up enabled or Port B (when Input)
0 : No Pull-up on Port B

b4 = **PCWS**: *Port C Wake-up Select.*
1 : Port C I/O functions enabled
0 : Port C Interrupt Wake-up Inputs enabled

b3 = **PC1S**: *PC1 Select.*
1 : Timer OCMP1 connected to pin 17
0 : PC1 I/O function connected to pin 17

b2 = **PC0S**: *PC0 Select.*
1 : Timer ICAP connected to pin 18
0 : PC0 I/O function connected to pin 18

b1 = **PA0S**: *Port A Output Select*.
1 : Port A Output is Push-pull
0 : Port A Output is Open-drain

b0 = **PAIP**: *Port A Input Pull-up.*
1 : Pull-up enabled on Port A (when Input)
0 : No Pull-up on Port A

1.5 EPROM ERASURE (ST72E94 ONLY)

The ST72E94 is erased by exposure to high intensity UV light through the transparent window. This exposure discharges the floating gate to its initial state through induced photo current.

It is recommended that the ST72E94 be kept out of direct sunlight because the UV content of sunlight can cause temporary functional failure. Extended exposure to room level fluorescent lighting will also cause erasure. An opaque coating (paint, tape, label, etc...) should be placed over the package window if the product is to be operated under these lighting conditions. Covering the window also reduces IDD in stop mode due to photo diode currents.

An Ultraviolet source of wave length 2537 Å yielding a total integrated dosage of 15 Watt-sec/cm is required to erase the ST72E94. This device will be erased in 15 to 20 minutes if an UV lamp with a 12mW/cm power rating is placed 1 inch from the lamp without filters.

1.6 VOLTAGE RANGE

The ST72E94 and ST72T94 operate with a minimum supply voltage of 3.0V when the ST7294 operates from 2.5V.

2 ELECTRICAL CHARACTERISTICS

2.1 ABSOLUTE MAXIMUM RATINGS

The ST72E94/T94 devices contain circuitry to protect the inputs against damage due to high static voltage or electric field. Nevertheless it is advised to take normal precautions and to avoid applying to this high impedance voltage circuit any voltage higher than the maximum rated voltages. It is recommended for proper operation that V_{IN} and V_{OUT} be constraint to the range:

$$V_{SS} \leq V_{IN} \text{ and } V_{OUT} \leq V_{DD}$$

To enhance reliability of operation, it is recommended to configure unused I/Os as inputs and to connect them to an appropriate logic voltage level such as V_{SS} or V_{DD}.

All the voltage in the following tables are referenced to V_{SS}.

Stresses above those listed as “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Rating (Voltage Referenced to V_{SS})

Symbol	Ratings	Value	Unit
V_{DD}	Supply Voltage	-0.3 to +6V	V
V_{IN}	Input Voltage	V_{SS} -0.3 to V_{DD} +0.3	V
IV_{DD} - IV_{SS}	Total current into VSS/VDD pins	50/20	mA
I	Current drain per pin excluding V_{DD} and V_{SS}	20	mA
T_A	Operating Temperature Range	T_L to T_H 0 to +70	°C
T_{STG}	Storage Temperature Range	-65 to +150	°C

2.2 POWER CONSIDERATIONS

T_J, the average chip-junction temperature in Celsius can be calculated from the following equation:

$$T_J = T_A + (P_D \times \theta J_A) \quad (1)$$

Where:

– T_A is the Ambient Temperature in °C,

– θJ_A is the Package Thermal Resistance, Junction-to-Ambient in °C/W,

– P_D the sum of P_{INT} and $P_{I/O}$,

– P_{INT} equals I_{CC} time V_{CC}, Watts-Chip Internal Power

– $P_{I/O}$ the Power Dissipation on Input and Output Pins, User Determined.

For most applications $P_{I/O} < P_{INT}$ and can be neglected.

$P_{I/O}$ may be significant if the device is configured to drive Darlington bases or sink LED Loads.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Therefore:

$$K = P_D \times (T_A + 273°C) + \theta J_A \times P_D^2 \quad (3)$$

Where K is constant pertaining to the particular part, K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

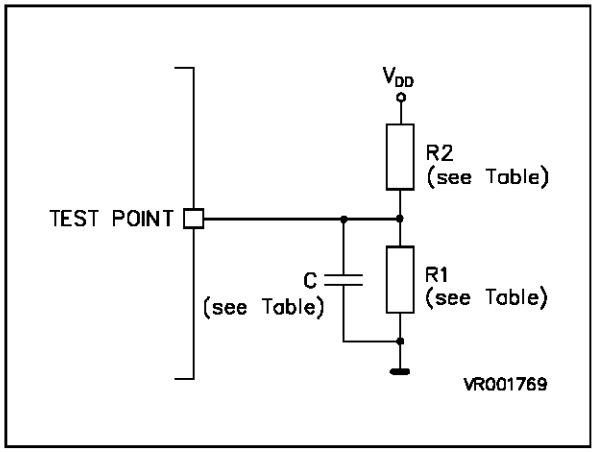
Thermal Characteristics

Symbol	Characteristics	Value	Unit
θJA	Thermal Resistance PDIP28 PSO28	 55 75	°C/W

Equivalent Test Load

V_{DD} = 3V			
Pins	**R1**	**R2**	**C**
PA0-PA7 PB0-PB7 PC0-PC5	10.91kΩ	6.32kΩ	50pF
V_{DD} = 4.5V			
Pins	**R1**	**R2**	**C**
PA0-PA7 PB0-PB7 PC0-PC5	3.26kΩ	2.38kΩ	50pF

Test Diagram



2.3 DC ELECTRICAL CHARACTERISTICS (T_A = -40°C to +85°C unless otherwise specified)

Symbol	Test Conditions	Min.	Typ.	Max.	Unit
V_{OL} V_{OH}	Output Voltage, Iload 10.0µA	 V_{DD}-0.1		0.1	V
V_{OH}	Output High Voltage I LOAD =0.8mA, PA0-PA7,PB0-PB7,PC0-PC5	V_{DD}-0.8			V
V_{OL}	Output Low Voltage I LOAD =1.6 mA, PA0-PA7,PB0-PB7,PC0-PC5,$\overline{\text{RESET}}$			0.4	V
V_{IH}	Input High Voltage PA0-PA7,PB0-PB7,PC0-PC5, $\overline{\text{INT}}$, $\overline{\text{RESET}}$	0.7xV_{DD}		V_{DD}	V
V_{IL}	Input Low Voltage PA0-PA7,PB0-PB7,PC0-PC5, $\overline{\text{INT}}$, $\overline{\text{RESET}}$	V_{SS}		0.2xV_{DD}	V
V_{RM}	Data Retention Mode (0 to 70°C)	2			V
I_{IL}	I/O Ports Hi-Z Leakage Current PA0-PA7,PB0-PB7, PC0-PC5			± 10	µA
I_{IN}	Input Current: $\overline{\text{RESET}}$, $\overline{\text{INT}}$, ICAP			± 1	µA
C_{OUT}	Capacitance: Ports (as Input or Output)			12	pF
C_{IN}	$\overline{\text{RESET}}$, $\overline{\text{INT}}$, ICAP			8	pF
R_{PU}	PORT A, B, C (1), V_{DD} = 3.5V, V_{IN} = 0V	125	250	500	kΩ

Note 1. When option is chosen

2.4 AC ELECTRICAL CHARACTERISTICS (T_A = -40°C to +85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{DD}	Operating Supply Voltage	RUN Mode HALT Mode EEPROM Write EEPROM Read	3.0 2.0 3.0 3.0		5.5	V
I_{DD}	Supply Current (1) (2) (3)	RUN Mode V_{DD}=5V,f_{OSC}=4MHz V_{DD}=3.0V,f_{OSC}=455KHz WAIT Mode V_{DD}=5V,f_{OSC}=4MHz V_{DD}=3.0V,f_{OSC}=455KHz HALT MODE V_{DD}=5V,T_A=70°C		 1.8 0.9 1	 2.5 0.7 1.5 500 10	 mA mA mA mA µA

Notes:

1. RUN (Operating) IDD, WAIT I_{DD} measured using external square wave clock all inputs 0.2V from rail, no DC load, less than 50pF on all outputs, CI = 20pF on OSCout.
2. WAIT, HALT all I/O configured as inputs, V_{IL} = 0.2V, V_{IH} = V_{DD} -0.2V.
3. HALT, OSCin = V_{SS}.

2.5 Control Timing (T_A = -40°C to +85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
f_{OSC}	Frequency of Operation	V_{DD}=5V V_{DD}=3.0V	DC DC		4 2	MHz
t_{ILCH}	HALT Mode Recovery Startup Time	Crystal Oscillator			50	ms
t_{RL}	External RESET Input Pulse Width		1.5			t_{CYC}
t_{PORL}	Power RESET Output		4096			t_{CYC}
t_{DOGL}	Watchdog RESET Output Pulse Width		1.5			
t_{DOG}	Watchdog Time-out		6144		7168	t_{CYC}
t_{ILIH}	Interrupt Pulse Width INT PORTC		 125 125			ns
t_{ILIL}	Interrupt Pulse Period		(1)			t_{CYC}
t_{OXOV}	Crystal Oscillator Startup Time				50	ms
t_{DDR}	Supply Rise Time	10% to 90%	0.01		100	ms

Note 1. The minimum period t_{ILIL} should not be less than the number of cycle times it takes to execute the interrupt service routine plus 21 cycles.

2.6 EEPROM

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
T_{WEE}	EEPROM Write Time	0 to 70°C		2	8	ms
Endurance	EEPROM Write/Erase Cycles	Q_A Lot Acceptance Criteria	300.000	> 1 million		cycles
Retention	EEPROM Data Retention	T_A = 55°C	10			Years

3 GENERAL INFORMATION

SGS-THOMSON offers ST7 devices in EPROM and OTP as well as in the ROM version. This range of product options provides the ST7 user with maximum of flexibility for his application needs.

The OTP rather than the ROM version of the ST7 is recommended when the customer's quantity requirement is relatively small on a given code - e.g. less than 10 thousand pieces. But the OTP solution is also popular even for volumes when the customer has a need for reduced leadtime, whether pre-production, an unforecasted increase in demand, or a quick program change. And the OTP is often preferred by those customers who have several codes running concurrently since they need purchase and stock only one vendor sales type.

However, it must be understood that the ROM and OTP follow different production flows and that the difference between these flows, in particular the method by which final electrical test is performed, may have an impact on the customer.

The basic production flow is as follows:

– Wafer diffusion

– Electrical test of dice (wafer sort)

– Assembly (encapsulation)

– Final electrical test

For ROM parts, the customer program is included at a specific mask of the wafer. Therefore, all of the product's functionality is present in both the die and the assembled product and this functionality can be fully evaluated at both wafer sort and final electrical test. SGS-THOMSON fully tests the ROM version's functionality at both wafer sort and final test, thus ensuring conformance to the electrical specification and a low reject rate.

But for OTPs there exists an additional feature that must be tested: programmability.The program memory of an OTP should be seen as a collection of fuses that will be blown during programming. These fuses can be "recovered" by lightening the die with UV light. This recovery is no longer possible once the OTP die has been encapsulated in an opaque plastic package. The programmability and data retention can only be fully tested at wafer sort.

At this step the dice are electrically tested and the memory is programmed to verify programmability. Then the wafers are placed in high temperature bake in order to provoke any possible memory retention defects. They are then retested to check data retention. After this test, UV light is used to "recover" the fuses and the good dice are assembled.

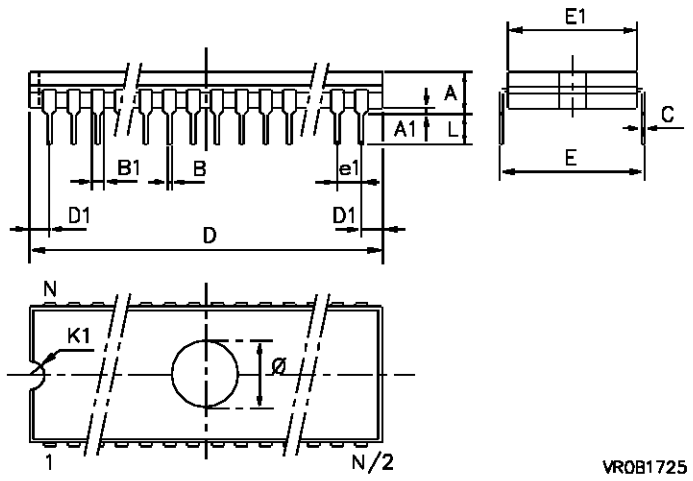
Although the programmability of the OTP dice is verified as fully functional at probe test, the die encapsulation process has the potential to affect this function in the finished product. It is therefore necessary that in addition to electrical final test, a programmability test be made. However since UV light cannot be used to erase an OTP's programmed byte once the die has been encapsulated it is then impossible to write a test pattern and thus to check 100% of the user program area. For this reason the final test is limited to a reserved number of bytes which are programmed and then verified.

As the programmability of the OTP cannot be fully tested once the die has been encapsulated, unlike the ROM or EPROM versions, a customer should find a programming reject rate below 1.0% and a data retention reject rate below 0.5% when programming is performed using qualified programming tools. Apart from the programmability, the OTP has the same reject as EPROM and ROM versions.

In order to lower the reject levels for programmability and data retention, SGS-THOMSON is continually pursuing technology improvements in areas such as soft die handling, low stress compounds, and passivation layer enhancements.

3.1 PACKAGE MECHANICAL DATA

Figure 4. 28-Ceramic Dual In Line Package, 600-mil Width



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			5.71			0.225
A1	0.50		1.78	0.020		0.070
B	0.40		0.55	0.016		0.022
B1	1.17		1.42	0.046		0.056
C	0.22		0.31	0.009		0.012
D			38.10			1.50
D1	1.52		2.49	0.060		0.098
E	-	-	-	-	-	-
E1	13.05		13.36	0.514		0.526
L	3.00			0.118		
e1	2.29		2.79	0.090		0.110
∅	6.86		7.36	0.270		0.290
	Number of Pins					
N	28					

3.2 ORDERING INFORMATION

ORDERING INFORMATION TABLE

Sales Types	ROM Size	Temperature Range	Package
ST72T94C6B6	6K	-40°C to +85°C	PDIP28
ST72T94C6M6			PSO28
ST72E94C6F0		25°C	CDIP28