



義隆電子股份有限公司

ELAN MICROELECTRONICS CORP.

EM78805A

8-BIT MICRO-CONTROLLER

Version 1.5

ELAN MICROELECTRONICS CORP.
No. 12, Innovation 1st RD., Science-Based Industrial Park
Hsin Chu City, Taiwan, R.O.C.
TEL: (03) 5639977
FAX: (03)5782037(SL) 5780617 (SA2)



User Application Note

1. ROM, OTP, ICE

ROM	OTP	ICE
EM78805A	EM78P806	ICE806

2. Main Function Difference

	EM78805A	EM78P806
Operation voltage	2.2 ~ 3.6V	2.5V ~ 5.5V



I. General Description

The EM78805A is an 8-bit CID (Call Identification) RISC type microprocessor with low power , high speed CMOS technology . Integrated onto a single chip are on_chip watchdog (WDT) , RAM , ROM , programmable real time clock /counter , internal interrupt , power down mode , LCD driver , Tone generator and tri-state I/O . The EM78805A/B provides a single chip solution to design a CID of calling message display .

II. Feature

CPU

- **Operating voltage range : 2.2V~3.6V**
- 8Kx 13 on chip ROM
- **1.1Kx 8 on chip RAM**
- **Up to 28 bi-directional tri-state I/O ports**
- 8 level stack for subroutine nesting
- 8-bit real time clock/counter (TCC) with 8-bit prescaler
- Two sets of 8 bit counters can be interrupt sources
- Selective signal sources and overflow interrupt
- Programmable free running on chip watchdog timer
- 99.9% single instruction cycle commands
- four modes (Main clock 3.579 , 1.79, 0.895 or 0.447MHz generated by internal PLL)
 1. Sleep mode : CPU and Main clock turn off, 32.768KHz clock turn off
 2. Idle mode : CPU and Main clock turn off, 32.768KHz clock turn on
 3. Green mode : Main clock turn off, CPU and 32.768KHz clock turn on
 4. Normal mode : Main clock turn on , CPU and 32.768KHz clock turn on
- Input port wake up function
- **7 interrupt source , 4 external , 3 internal**
- IO Port key scan function
- IO Port interrupt , pull high ,wake-up and open drain functions
- External Sub-Clock frequency is 32.768KHz
- Dual TONE Generators

LCD

- LCD operation voltage chosen by software
- Common driver pins : 16 (8 of 16 Common shared by I/O)
- Segment driver pins : 32 (12 of 32 Segment shared by I/O)
- 1/4 bias
- 1/8,1/16 duty

PACKAGE

- **64 pin QFP (EM78805AAQ, POVD disable) (EM78805ABQ, POVD enable) or 64 pin Chip (EM78805AH)**

III. Application

1. adjunct units
2. answering machines
3. feature phones



IV.Pin Configuration

	48	SEG32/P9.0	
	47	SEG23/P5.7	
	46	SEG22/P5.6	
	45	SEG21/P5.5	
	44	SEG20/P5.4	
	43	SEG19	
	42	SEG18	
	41	SEG17	
	40	SEG16	
	39	SEG15	
	38	SEG14	
	37	SEG13	
	36	SEG12	
	35	SEG11	
	34	SEG10	
	33	SEG9	
SEG33/P9.1	49		32 SEG8
SEG34/P9.2	50		31 SEG7
SEG35/P9.3	51		30 SEG6
SEG36/P9.4	52		29 SEG5
SEG37/P9.5	53		28 SEG4
SEG38/P9.6	54		27 SEG3
SEG39/P9.7	55		26 SEG2
RESET	56		25 SEG1
P70/INT0	57		24 SEG0
P71/INT1	58		23 TEST
P72/INT2	59		22 VSS
P73/INT3	60		21 COM0
P74	61		20 COM1
P75	62		19 COM2
P76	63		18 COM3
P77	64	●	17 COM4
1		TONE	
2		PLL	
3		XIN	
4		XOUT	
5		VDD	
6		COM15/P6.7	
7		COM14/P6.6	
8		COM13/P6.5	
9		COM12/P6.4	
10		COM11/P6.3	
11		COM10/P6.2	
12		COM9/P6.1	
13		COM8/P6.0	
14		COM7	
15		COM6	
16		COM5	

Fig.1 Pin Assignment

V.Functional Block Diagram

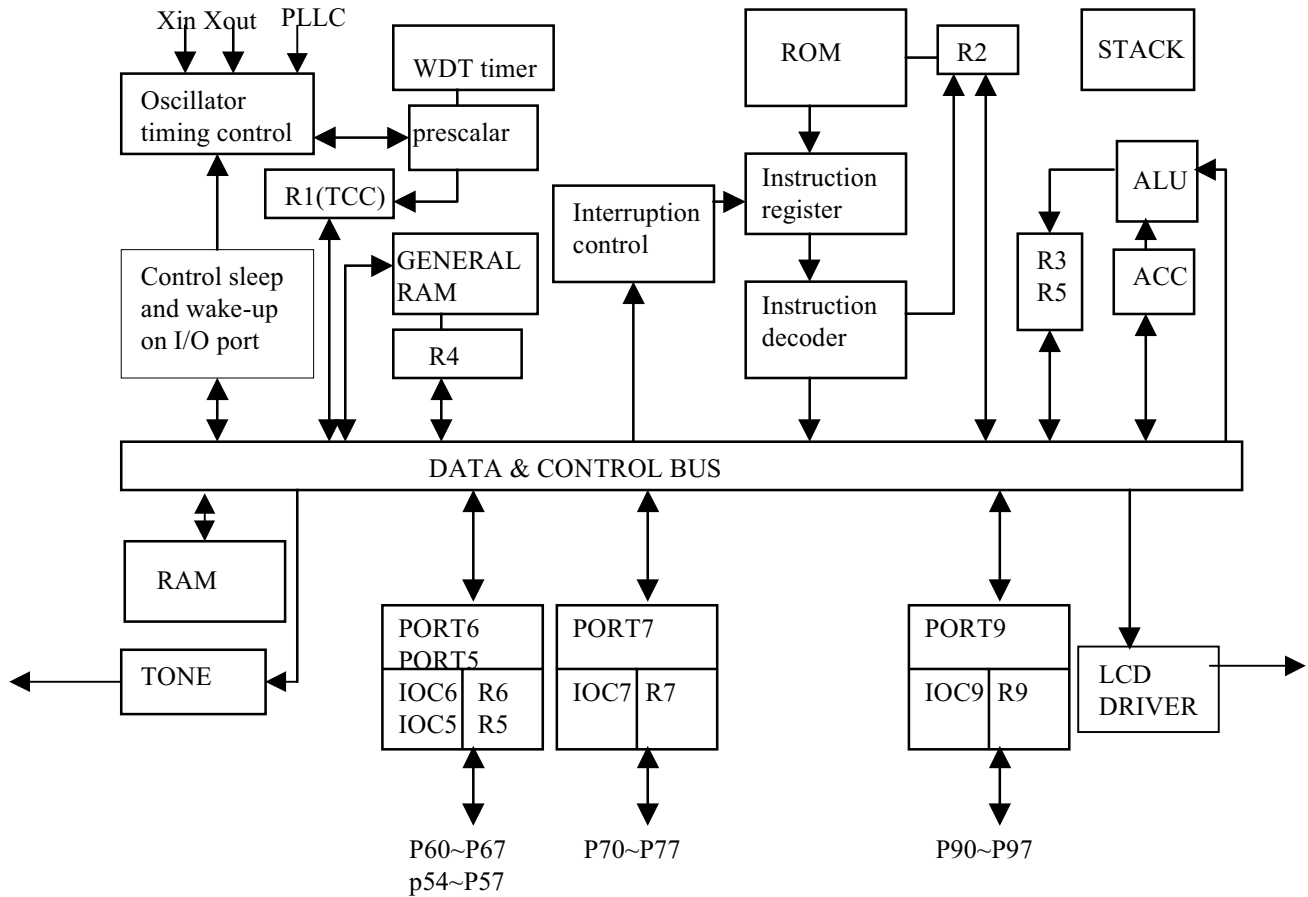


Fig.2 Block diagram



VI.Pin Descriptions

PIN	I/O	DESCRIPTION
VDD	POWER	digital power
AVDD		analog power
VSS	POWER	digital ground
AVSS		analog ground
Xtin	I	Input pin for 32.768 kHz oscillator
Xtout	O	Output pin for 32.768 kHz oscillator
COM0..COM7	O	Common driver pins of LCD drivers
COM8..COM15	O (PORT6)	
SEG0..SEG19	O	Segment driver pins of LCD drivers
SEG20..SEG23	O (PORT5)	
SEG24..SEG31	O (PORT8)	
SEG32..SEG39	O (PORT9)	
PLLC	I	Phase loop lock capacitor, 0.01u to 0.047u with AVSS
INT0..INT3	PORT7(0..3)	PORT7(0)~PORT7(3) signal can be interrupt signals.
P5.4 ~P.57	PORT5	PORT5 can be INPUT or OUTPUT port each bit. And shared with Segment signal.
P7.0 ~P7.7	PORT7	PORT7 can be INPUT or OUTPUT port each bit. Internal Pull high function. Key scan function. Bit6,7 open drain function
P6.0 ~P6.7	PORT6	PORT6 can be INPUT or OUTPUT port each bit. And shared with Common signal.
P9.0 ~P9.7	PORT9	PORT 9 can be INPUT or OUTPUT port each bit. And shared with Segment signal. Bit6,7 has wake-up function.
TEST	I	Test pin into test mode , normal low
TONE	O	Tone generator's output
RESET	I	

VII.Functional Descriptions

VII.1 Operational Registers

1. R0 (Indirect Addressing Register)

* R0 is not a physically implemented register. It is useful as indirect addressing pointer. Any instruction using R0 as register actually accesses data pointed by the RAM Select Register (R4).

2. R1 (TCC)

* Increased by an external signal edge applied to TCC , or by the instruction cycle clock.

Written and read by the program as any other register.

3. R2 (Program Counter)

* The structure is depicted in Fig.3

* Generates $8K \times 13$ on-chip ROM addresses to the relative programming instruction codes.

* "JMP" instruction allows the direct loading of the low 10 program counter bits.

* "CALL" instruction loads the low 10 bits of the PC, PC+1, and then push into the stack.

* "RET" ("RETL k", "RETI") instruction loads the program counter with the contents at the top of stack.

* "MOV R2,A" allows the loading of an address from the A register to the PC, and the ninth and tenth bits are cleared to "0".

- * "ADD R2,A" allows a relative address be added to the current PC, and contents of the ninth and tenth bits are cleared to "0".
- * "TBL" allows a relative address be added to the current PC, and contents of the ninth and tenth bits don't change. The most significant bit (A10~A12) will be loaded with the content of bit PS0~PS2 in the status register (R5) upon the execution of a "JMP", "CALL", "ADD R2,A", or "MOV R2,A" instruction.

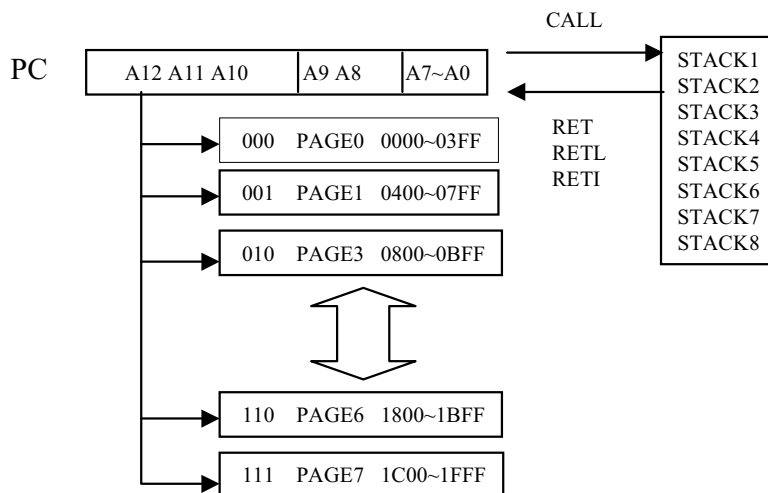


Fig.3 Program counter organization

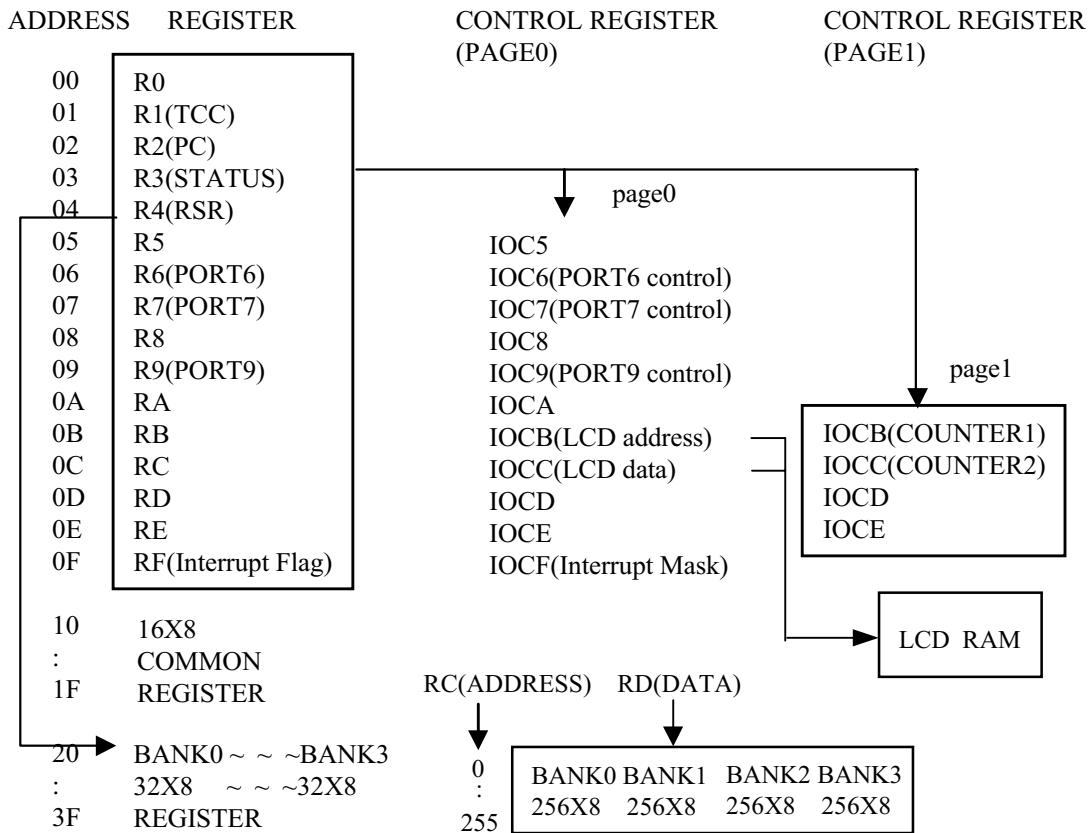


Fig.4 Data memory configuration

4. R3 (Status Register)

7	6	5	4	3	2	1	0
PAGE	P_TONE2	P_TONE1	T	P	Z	DC	C

- * Bit 0 (C) Carry flag
- * Bit 1 (DC) Auxiliary carry flag
- * Bit 2 (Z) Zero flag
- * Bit 3 (P) Power down bit. Set to 1 during power on or by a "WDTC" command and reset to 0 by a "SLEP" command.
- * Bit 4 (T) Time-out bit. Set to 1 by the "SLEP" and "WDTC" command, or during power up and reset to 0 by WDT timeout.

EVENT	T	P	REMARK
WDT wake up from sleep mode	0	0	
WDT time out (not sleep mode)	0	1	
/RESET wake up from sleep power up	1	0	
power up	1	1	
Low pulse on /RESET	x	x	x .. don't care

- *Bit5: Power control bit of Tone generator 1 . User can use this bit to power on the tone generator.
- *Bit6: Power control bit of Tone generator 2 . User can use this bit to power on the tone generator.

* This specification are subject to be changed without notice.



Tone frequency controlled by IOCD and IOCE.

R4(6,5)	Tone generator2	Tone generator1
00	Power off	Power off
01	Power off	Power on
10	Power on	Power off
11	Power on	Power on

* Bit 7 PAGE : change IOCB ~ IOCE to another page , 0/1 => page0 / page1

5. R4 (RAM Select Register)

- * Bits 0 ~ 5 are used to select up to 64 registers in the indirect addressing mode.
- * Bits 6 ~ 7 determine which bank is activated among the 4 banks.
- * See the configuration of the data memory in Fig. 5.

6. R5 (Program Page Select Register)

7	6	5	4	3	2	1	0
R57	R56	R55	R54	x	PS2	PS1	PS0

* Bit 0 (PS0) ~ Bit2 (PS2) Page select bits should be set before JMP or CALL instruction.
Page select bits

PS2	PS1	PS0	Program memory page (Address)
0	0	0	Page 0
0	0	1	Page 1
0	1	0	Page 2
0	1	1	Page 3
1	0	0	Page 4
1	0	1	Page 5
1	1	0	Page 6
1	1	1	Page 7

User can use PAGE instruction to change page. To maintain program page by user. Otherwise, user can use far jump (FJMP) or far call (FCALL) instructions to program user's code. And the program page is maintained by EMC's compiler. It will change user's program by inserting instructions within program.

***Bit3 : unused**

*Bit4 ~7: 4-bit I/O registers.

6. R6 ~ R9 (Port 6 ~ Port 9)

* R6, R7 and R9 are three 8-bit I/O registers for Port6, Port7 and Port9. **R8 is unaccess.**

7. RA

7	6	5	4	3	2	1	0
IDLE	/358E	CLK2	CLK1	x	x	x	x

* **Bit0~Bit3 : unused**

* Bit4~ Bit5: MAIN clock selection bits.

User can choose the main clock by CLK1 and CLK2. All the clock is list below.

CLK2, CLK1	MAIN clock	/358E	CPU's clock
0,0	0.447MHz	1	0.447MHz
0,1	0.895MHz	1	0.895MHz

1,0	1.79MHz	1	1.79MHz
1,1	3.579MHz	1	3.579MHz
0,0	X	0	32768HZ
0,1	X	0	32768HZ
1,0	X	0	32768HZ
1,1	X	0	32768HZ

* Bit6(read/write)(PLL enable signal)
0/1=DISABLE/ENABLE

The relation between 32.768kHz and 3.579MHz can see Fig.6

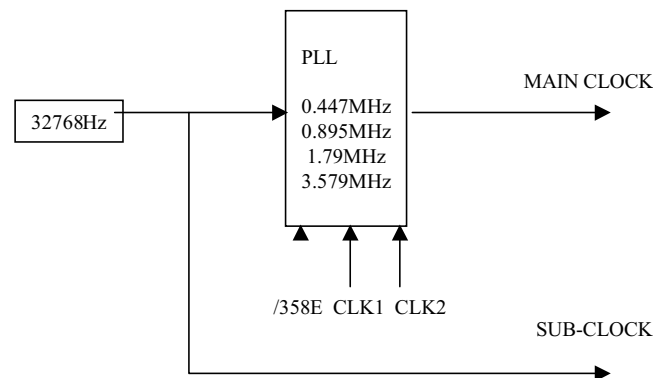


Fig.6 The relation between 32.768kHz and 3.579MHz .

* Bit7 IDLE: sleep mode selection bit

0/1=sleep mode/IDLE mode. This bit will decide SLEP instruction which mode to go.

These two modes can be waken up by TCC clock or Watch Dog or PORT9 and run from "SLEP" next instruction.

Wakeup signal	SLEEP mode	IDLE mode	GREEN mode	NORMAL mode
	RA(7,6)=(0,0) + SLEP	RA(7,6)=(1,0) + SLEP	RA(7,6)=(x,0) no SLEP	RA(7,6)=(x,1) no SLEP
TCC time out	X	Wake-up + Interrupt + Next instruction	Interrupt	Interrupt
WDT time out	RESET	Wake-up + Next instruction	RESET	RESET
Port96,97	RESET	Wake-up + Next instruction	X	X
PORT70~73	RESET	Wake-up + Interrupt + Next instruction	Interrupt	Interrupt

*P70 ~ P73 's wakeup function is controlled by IOCF(1,2,3) and ENI instruction.

*P70 's wakeup signal is a rising or falling signal defined by CONT REGISTER bit7.

*Port96,Port97 ,Port71,Port72 and Port73 's wakeup signal is a falling edge signal.

8. RB

7	6	5	4	3	2	1	0
x	x	x	x	LOW_BAT	CALL_2	/LPD	CALL_1

*Bit2,Bit0:"00" to "11" are four blocks of CALLER ID RAM area. User can use 1.0K RAM with RC ram address.

*Bit1(/LPD): Low battery detect disable/enable, 0/1= disable/enable

*Bit3(LOW_BAT):Low battery signal, 0/1 = battery voltage is low/normal.

If the battery voltage is under 2.5V then sends a '0' signal to RA register bit4 or a '1' signal to this Bit if VDD is over 2.6V.

The relation between /LPD,/POVD and /LOW_BAT can see Fig..7

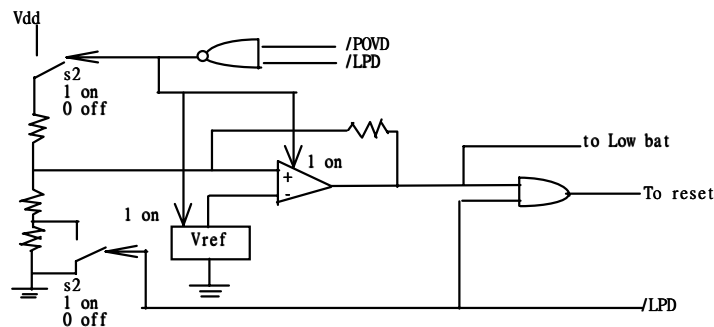


Fig.7 The relation between /LPD,/POVD

* Bit 4~ 7: unused

9. RC

7	6	5	4	3	2	1	0
CIDA7	CIDA6	CIDA5	CIDA4	CIDA3	CIDA2	CIDA1	CIDA0

* Bit 0 ~ Bit 7 select CALLER ID RAM address up to 256.

10. RD

* Bit 0 ~ Bit 8 are CALLER ID RAM data transfer register.

User can see RB register how to select CID RAM banks.

11. RE

7	6	5	4	3	2	1	0
x	/WDTE	/WUP97	/WUP96	x	LCD_C2	LCD_C1	LCD_M

* Bit0 (LCD_M):LCD_M decides the methods, including duty, bias, and frame frequency.

* Bit1~Bit2 (LCD_C#):LCD_C# decides the LCD display enable or blanking. change the display duty must set the "LCD_C2,LCD_C1" to "00".

LCD_C2,LCD_C1	LCD Display Control	LCD_M	duty	bias
0 0	Change duty	0	1/16	1/4
	Disable(turn off LCD)	1	1/8	1/4
0 1	Blanking	:	:	:
1 1	LCD display enable	:	:	:

* Bit3 : unused

* Bit4 (/WUP96, PORT9 bit6 Wake Up Enable): used to enable the wake-up function of PORT9 bit6 . (1/0=enable/disable)

* Bit5 (/WUP97, PORT9 bit7 Wake Up Enable): used to enable the wake-up function of PORT9 bit7 . (1/0=enable/disable)

* Bit6 (/WDTE, Watch Dog Timer Enable)

Control bit used to enable Watchdog timer.

(1/0=enable/disable)

* Bit7 : unused



12. RF (Interrupt Status Register)

7	6	5	4	3	2	1	0
x	x	C8_2	C8_1	INT2/INT3	INT1	INT0	TCIF

- * "1" means interrupt request, "0" means non-interrupt
- * Bit 0 (TCIF) TCC timer overflow interrupt flag. Set when TCC timer overflows .
- * Bit 1 (INT0) external INT0 pin interrupt flag .
- * Bit 2 (INT1) external INT1 pin interrupt flag .
- * Bit 3 (INT2/INT3) external INT2 and INT3 pin interrupt flag .
- * Bit 4 (C8_1) internal 8 bit counter interrupt flag .
- * Bit 5 (C8_2) internal 8 bit counter interrupt flag .
- * **Bit 6~7 : unused**
- * High to low edge trigger , Refer to the Interrupt subsection. (INT0 can be triggered by low to high signal , refer to CONT bit 7)
- * IOCF is the interrupt mask register. User can read and clear.

13. R10~R3F (General Purpose Register)

- * R10~R3F (Banks 0~3) all are general purpose registers.

VII.2 Special Purpose Registers

1. A (Accumulator)

- * Internal data transfer, or instruction operand holding
- * It's not an addressable register.

2. CONT (Control Register)

7	6	5	4	3	2	1	0
INT_EDGE	INT	TS	-	PAB	PSR2	PSR1	PSR0

- * Bit 0 (PSR0) ~ Bit 2 (PSR2) TCC/WDT prescaler bits.

PSR2	PSR1	PSR0	TCC Rate	WDT Rate
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

- * Bit 3 (PAB) Prescaler assignment bit.
0/1 : TCC/WDT
- * Bit 4 unused
- * Bit 5 (TS) TCC signal source
0: internal instruction cycle clock
1: 16.38KHz
- * Bit 6 : (INT)INT enable flag
0: interrupt masked by DISI or hardware interrupt
1: interrupt enabled by ENI/RETI instructions

- * Bit 7 : INT_EDGE
0:P70 's interruption source is a rising edge signal.
1:P70 's interruption source is a falling edge signal.

* CONT register is readable and writable.

3. IOC5

7	6	5	4	3	2	1	0
IOC54	IOC54	IOC54	IOC54	x	x	x	x

*Bit0 ~ Bit3 : unused

*Bit4~Bit7: I/O direction control registers of PORT5.

* "1" put the relative I/O pin into high impedance (input port), while "0" put the relative I/O pin as output.

4. IOC6 ~ IOC9 (I/O Port Control Register)

* IOC6, IOC7 and IOC9 are three I/O direction control registers.

* "1" put the relative I/O pin into high impedance (input port), while "0" put the relative I/O pin as output.

* **IOC8 is unaccess.**

5. IOCA

7	6	5	4	3	2	1	0
P9SH	P9SL	P6S	P5S	Bias3	Bias2	Bias1	SC

* Bit 0 :SC (SCAN KEY signal) 0/1 = disable/enable. Once you enable this bit , all of the LCD signal will have a low pulse during a common period. This pulse has 30us width. Please use the procedure to implement the key scan function.

- a. set port7 as input port
- b. set IOCD page0 port7 pull high
- c. enable scan key signal
- d. Once push a key . Set RA(6)=1 and switch to normal mode.
- e. Blank LCD. Disable scan key signal.
- f. Set P6S =0. Port6 sent probe signal to port7 and read port7. Get the key.
- g. Note!! A probe signal should be delay a instruction at least to another probe signal.
- h. Set P6S =1. Port6 as LCD signal. Enable LCD.

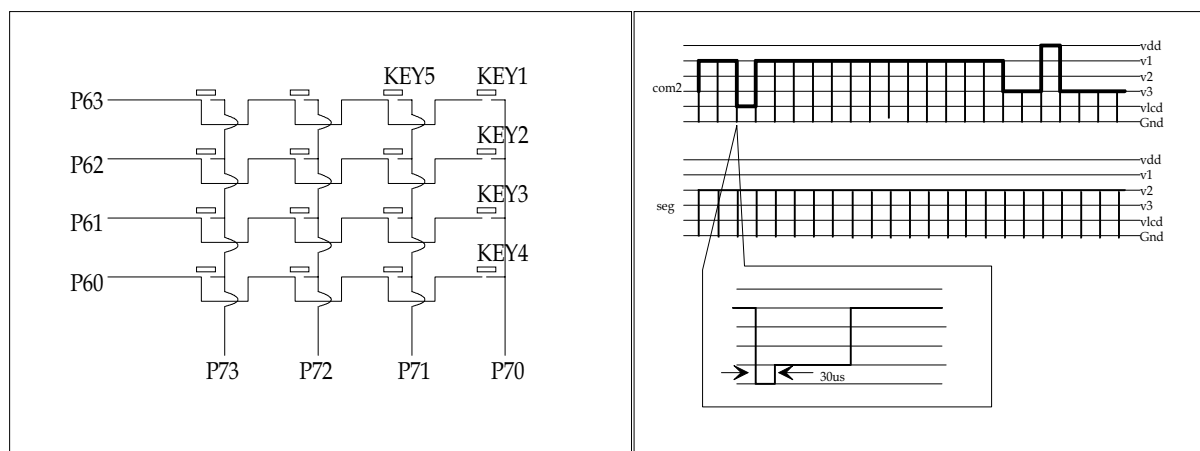


Fig.9 Key scan circuit



* Bit 3~1 (Bias3~Bias1) Control bits used to choose LCD operation voltage .

LCD operate voltage	Vop (VDD 3.3V)	VDD=3.3V
000	0.60VDD	1.98V
001	0.66VDD	2.18V
010	0.74VDD	2.44V
011	0.82VDD	2.71V
100	0.87VDD	2.87V
101	0.93VDD	3.07V
110	0.96VDD	3.17V
111	1.00VDD	3.3V

* Bit4: port5 nibble switch, 0/1= normal I/O port/SEGMENT output .

* Bit5:port6 switch , 0/1= normal I/O port/COMMON output

* Bit6:port9 low nibble switch , 0/1= normal I/O port/SEGMENT output . Bit7:port9 high nibble switch

6. IOCB (LCD ADDRESS)

PAGE0 : Bit6 ~ Bit0 = LCDA6 ~ LCDA0

The LCD display data is stored in the data RAM . The relation of data area and COM/SEG pin is as below:

COM15 ~ COM8	COM7 ~ COM0	
40H (Bit15 ~ Bit8)	00H (Bit7 ~ Bit0)	SEG0
41H	01H	SEG1
:	:	:
67H	27H	SEG39
:	:	Empty
7FH	3FH	Empty

PAGE1 : 8 bit up-counter (COUNTER1) preset and read out register . (write = preset) . After a interruption , it will count from "00".

7. IOCC (LCD DATA)

PAGE0 : Bit7 ~ Bit0 = LCD RAM data register

PAGE1 : 8 bit up-counter (COUNTER2) preset and read out register . (write = preset) After a interruption , it will count from "00".

8. IOCD

PAGE0 :

7	6	5	4	3	2	1	0
T17	T16	T15	T14	T13	T12	T11	T10

Tone generator 1 's frequency divider. Please Run in Normal mode .

Clock source = 111843Hz

T17~T10 = '11111111' => Tone generator1 will has 438Hz SIN wave output.

:

T17~T10 = '00000010' => Tone generator1 will has 55921Hz SIN wave output.

T17~T10 = '00000001' => Tone generator1 will has 111843Hz

T17~T10 = '00000000' => no used

PAGE1:

7	6	5	4	3	2	1	0
PH7	PH6	PH5	PH4	PH3	PH2	PH1	PH0



* Bit 0 ~ 7 (/PH#) Control bit used to enable the pull-high of PORT7(#) pin.

- 1: Enable internal pull-high
- 0: Disable internal pull-high

9. IOCE

PAGE0 :

7	6	5	4	3	2	1	0
T27	T26	T25	T24	T23	T22	T21	T20

Tone generator 2 's frequency divider. Please Run in Normal mode.

Clock source = 111843Hz

T27~T20 = '11111111' => Tone generator1 will has 438Hz SIN wave output.

:

T27~T20 = '00000010' => Tone generator1 will has 55921Hz SIN wave output.

T27~T20 = '00000001' => Tone generator1 will has 111843Hz SIN wave output.

T27~T20 = '00000000' => no used

TONE1(IOCD)	ROW FREQ.				
(0xA0)	699.02Hz	1	2	3	A
(0x91)	771.33Hz	4	5	6	B
(0X83)	853.76Hz	7	8	9	C
(0X77)	939.86Hz	*	0	#	D
		1202.6 (0X5D)	1331.5(0X54)	1471.7(0X4C)	1644.8(0X44)
		TONE2(IOCE)			

PAGE1 :

7	6	5	4	3	2	1	0
OP77	OP76	C2S	C1S	PSC2	PSC1	PSC0	x

* Bit0 : unused

* Bit3~Bit1: counter1 prescaler , reset=(0,0,0)

(PSC2,PSC1,PSC0)	Scaler
0,0,0	1:1
0,0,1	1:2
0,1,0	1:4
0,1,1	1:8
1,0,0	1:16
1,0,1	1:32
1,1,0	1:64
1,1,1	1:128

* Bit4:counter1 source , (0/1)=(32768Hz/MAIN clock if enable)

* Bit5:counter2 source , (0/1)=(32768Hz/MAIN clock if enable) scale=1:1

* Bit6:P76 opendrain control (0/1)=(disable/enable)

* Bit7:P77 opendrain control (0/1)=(disable/enable)

10. IOCF (Interrupt Mask Register)

7	6	5	4	3	2	1	0
x	x	C8_2	C8_1	INT2/INT3	INT1	INT0	TCIF

* Bit 0 ~ 5 interrupt enable bit.

- 0: disable interrupt
- 1: enable interrupt

* Bit 6,7 : unused

* IOCF Register is readable and writable.

VII.3 TCC/WDT Prescaler

There is an 8-bit counter available as prescaler for the TCC or WDT. The prescaler is available for the TCC only or WDT only at the same time.

- An 8 bit counter is available for TCC or WDT determined by the status of the bit 3 (PAB) of the CONT register.
- See the prescaler ratio in CONT register.
- Fig. 10 depicts the circuit diagram of TCC/WDT.
- Both TCC and prescaler will be cleared by instructions which write to TCC each time.
- The prescaler will be cleared by the WDTC and SLEP instructions, when assigned to WDT mode.
- The prescaler will not be cleared by SLEP instructions, when assigned to TCC mode.

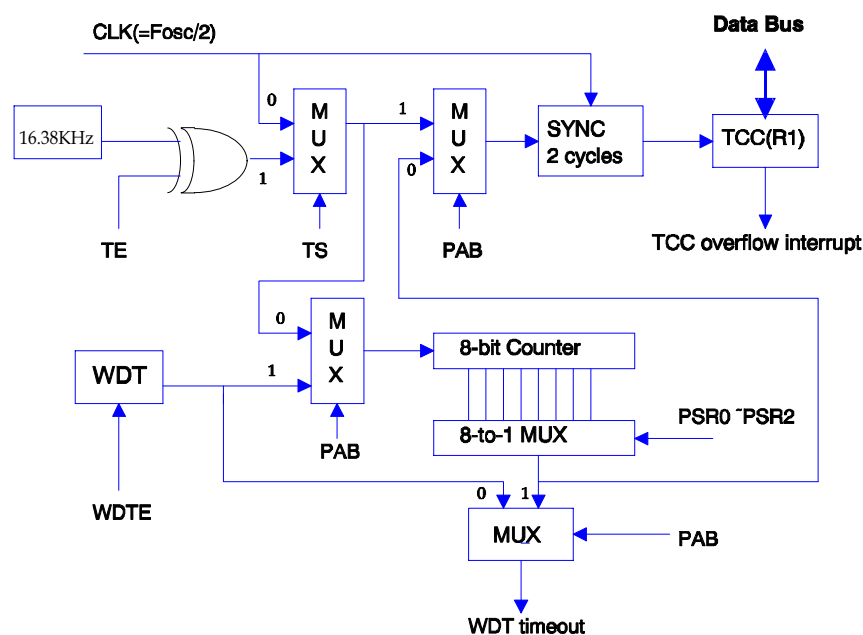


Fig.10 Block diagram of TCC WDT

VII.4 I/O Ports

The I/O registers, Port5 ~ Port 9, are bi-directional tri-state I/O ports. Port 7 can be pulled-high internally by software control. The I/O ports can be defined as "input" or "output" pins by the I/O control registers (IOC6 ~ IOC9) under program control. The I/O registers and I/O control registers are both readable and writable. The I/O interface circuit is shown in Fig.11.

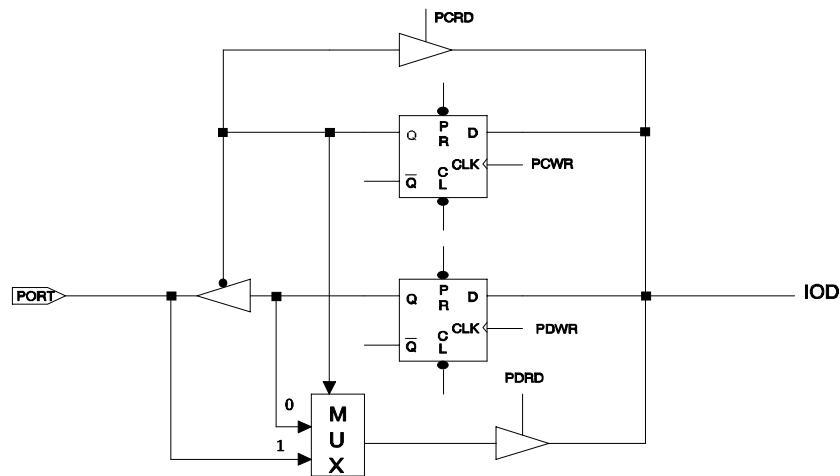


Fig.11 The circuit of I/O port and I/O control register

VII.5 RESET and Wake-up

The RESET can be caused by

- (1) Power on reset, or Voltage detector
- (2) WDT timeout. (if enabled and in GREEN or NORMAL mode)

Note that only Power on reset, or only Voltage detector in Case(1) is enabled in the system by CODE Option bit. If Voltage detector is disabled, Power on reset is selected in Case (1). Refer to Fig. 12.

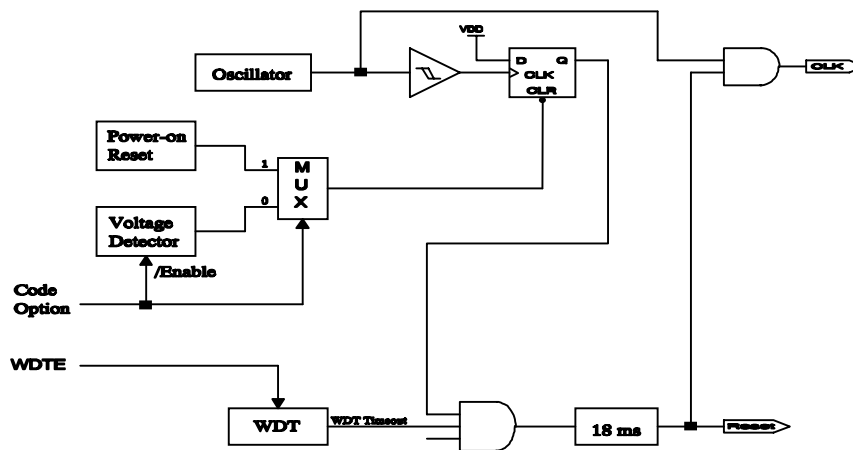


Fig.12 Block diagram of Reset of controller

Once the RESET occurs, the following functions are performed.

- The oscillator is running, or will be started.
- The Program Counter (R2) is set to all "0".
- When power on, the upper 3 bits of R3 and the upper 2 bits of R4 are cleared.
- The Watchdog timer and prescaler are cleared.
- The Watchdog timer is disabled.
- The CONT register is set to all "1"
- The other register (bit7..bit0)



R5 = "xxxx0000"	IOC5 = "1111xxxx"	
R6 = PORT	IOC6 = "11111111"	
R7 = PORT	IOC7 = "11111111"	
R8 = (unaccess)	IOC8 = (unaccess)	
R9 = PORT	IOC9 = "11111111"	
RA = "00000000"	IOCA = "00000000"	
RB = "00000000"	Page0 IOCB = "00000000"	Page1 IOCB = "00000000"
RC = "00000000"	Page0 IOCC = "0xxxxxxx"	Page1 IOCC = "00000000"
RD = "xxxxxxx"	Page0 IOCD = "00000000"	Page1 IOCD = "00000000"
RE = "x0000000"	Page0 IOCE = "00000000"	Page1 IOCE = "00000000"
RF = "xx000000"	IOCF = "xx000000"	

The controller can be awakened from SLEEP mode or IDLE mode (execution of "SLEP" instruction, named as SLEEP MODE or IDLE mode) by (1)TCC time out (IDLE mode only) (2) WDT time-out (if enabled) or, (3) external input at PORT9 (4)RINGTIME pin. The four cases will cause the controller wake up and run from next instruction in IDLE mode, reset in SLEEP mode. After wake-up, user should control WATCH DOG in case of reset in GREEN mode or NORMAL mode. The last three should be open RE register before into SLEEP mode or IDLE mode. The first one case will set a flag in RF bit0. And it will go to address 0x08 when TCC generate a interrupt.

VII.6 Interrupt

The CALLER ID IC has internal interrupts which are falling edge triggered, as followed : TCC timer overflow interrupt (internal), two 8-bit counters overflow interrupt.

If these interrupt sources change signal from high to low, then RF register will generate '1' flag to corresponding register if you enable IOCF register.

RF is the interrupt status register which records the interrupt request in flag bit. IOCF is the interrupt mask register. Global interrupt is enabled by ENI instruction and is disabled by DISI instruction. When one of the interrupts (when enabled) generated, will cause the next instruction to be fetched from address 008H. Once in the interrupt service routine the source of the interrupt can be determined by polling the flag bits in the RF register. The interrupt flag bit must be cleared in software before leaving the interrupt service routine and enabling interrupts to avoid recursive interrupts.

There are four external interrupt pins including INT0, INT1, INT2, INT3. And four internal counter interrupt available.

External interrupt INT0, INT1, INT2, INT3 signals are from PORT7 bit0 to bit3. If IOCF is enable then these signal will cause interrupt, or these signals will be treated as general input data.

After reset, the next instruction will be fetched from address 000H and the instruction inturrept is 001H and the hardware inturrept is 008H.

TCC will go to address 0x08 in GREEN mode or NORMAL mode after time out. And it will run next instruction from "SLEP" instruction and then go to address 0x08 in IDLE mode. These two cases will set a RF flag.

VII.7 Instruction Set

Instruction set has the following features:

- (1). Every bit of any register can be set, cleared, or tested directly.
- (2). The I/O register can be regarded as general register. That is, the same instruction can operates on I/O register.

The symbol "R" represents a register designator which specifies which one of the 64 registers (including operational registers and general purpose registers) is to be utilized by the instruction. Bits 6 and 7 in R4 determine the selected register bank. "b" represents a bit field designator which selects the number of the bit, located in the register "R", affected by the operation. "k" represents an 8 or 10-bit constant or literal value.



INSTRUCTION BINARY	HEX	MNEMONIC	OPERATION	STATUS AFFECTED
0 0000 0000 0000	0000	NOP	No Operation	None
0 0000 0000 0001	0001	DAA	Decimal Adjust A	C
0 0000 0000 0010	0002	CONTW	A → CONT	None
0 0000 0000 0011	0003	SLEP	0 → WDT, Stop oscillator	T,P
0 0000 0000 0100	0004	WDTC	0 → WDT	T,P
0 0000 0000 rrrr	000r	IOW R	A → IOCR	None
0 0000 0001 0000	0010	ENI	Enable Interrupt	None
0 0000 0001 0001	0011	DISI	Disable Interrupt	None
0 0000 0001 0010	0012	RET	[Top of Stack] → PC	None
0 0000 0001 0011	0013	RETI	[Top of Stack] → PC Enable Interrupt	None
0 0000 0001 0100	0014	CONTR	CONT → A	None
0 0000 0001 rrrr	001r	IOR R	IOCR → A	None
0 0000 0010 0000	0020	TBL	R2+A → R2 bits 9,10 do not clear	Z,C,DC
0 0000 01rr rrrr	00rr	MOV R,A	A → R	None
0 0000 1000 0000	0080	CLRA	0 → A	Z
0 0000 11rr rrrr	00rr	CLR R	0 → R	Z
0 0001 00rr rrrr	01rr	SUB A,R	R-A → A	Z,C,DC
0 0001 01rr rrrr	01rr	SUB R,A	R-A → R	Z,C,DC
0 0001 10rr rrrr	01rr	DECA R	R-1 → A	Z
0 0001 11rr rrrr	01rr	DEC R	R-1 → R	Z
0 0010 00rr rrrr	02rr	OR A,R	A ∨ VR → A	Z
0 0010 01rr rrrr	02rr	OR R,A	A ∨ VR → R	Z
0 0010 10rr rrrr	02rr	AND A,R	A & R → A	Z
0 0010 11rr rrrr	02rr	AND R,A	A & R → R	Z
0 0011 00rr rrrr	03rr	XOR A,R	A ⊕ R → A	Z
0 0011 01rr rrrr	03rr	XOR R,A	A ⊕ R → R	Z
0 0011 10rr rrrr	03rr	ADD A,R	A + R → A	Z,C,DC
0 0011 11rr rrrr	03rr	ADD R,A	A + R → R	Z,C,DC
0 0100 00rr rrrr	04rr	MOV A,R	R → A	Z
0 0100 01rr rrrr	04rr	MOV R,R	R → R	Z
0 0100 10rr rrrr	04rr	COMA R	/R → A	Z
0 0100 11rr rrrr	04rr	COM R	/R → R	Z
0 0101 00rr rrrr	05rr	INCA R	R+1 → A	Z
0 0101 01rr rrrr	05rr	INC R	R+1 → R	Z
0 0101 10rr rrrr	05rr	DJZA R	R-1 → A, skip if zero	None
0 0101 11rr rrrr	05rr	DJZ R	R-1 → R, skip if zero	None
0 0110 00rr rrrr	06rr	RRCA R	R(n) → A(n-1) R(0) → C, C → A(7)	C
0 0110 01rr rrrr	06rr	RRC R	R(n) → R(n-1) R(0) → C, C → R(7)	C
0 0110 10rr rrrr	06rr	RLCA R	R(n) → A(n+1) R(7) → C, C → A(0)	C
0 0110 11rr rrrr	06rr	RLC R	R(n) → R(n+1) R(7) → C, C → R(0)	C
0 0111 00rr rrrr	07rr	SWAPA R	R(0-3) → A(4-7) R(4-7) → A(0-3)	None

* This specification are subject to be changed without notice.



0	0111	01rr	rrrr	07rr	SWAP R	R(0-3) ↔ R(4-7)	None
0	0111	10rr	rrrr	07rr	JZA R	R+1 → A, skip if zero	None
0	0111	11rr	rrrr	07rr	JZ R	R+1 → R, skip if zero	None
0	100b	bbrr	rrrr	0xxx	BC R,b	0 → R(b)	None
0	101b	bbrr	rrrr	0xxx	BS R,b	1 → R(b)	None
0	110b	bbrr	rrrr	0xxx	JBC R,b	if R(b)=0, skip	None
0	111b	bbrr	rrrr	0xxx	JBS R,b	if R(b)=1, skip	None
1	00kk	kkkk	kkkk	1kkk	CALL k	PC+1 → [SP] (Page, k) → PC	None
1	01kk	kkkk	kkkk	1kkk	JMP k	(Page, k) → PC	None
1	1000	kkkk	kkkk	18kk	MOV A,k	k → A	None
1	1001	kkkk	kkkk	19kk	OR A,k	A ∨ k → A	Z
1	1010	kkkk	kkkk	1Akk	AND A,k	A & k → A	Z
1	1011	kkkk	kkkk	1Bkk	XOR A,k	A ⊕ k → A	Z
1	1100	kkkk	kkkk	1Ckk	RETL k	k → A, [Top of Stack] → PC	None
1	1101	kkkk	kkkk	1Dkk	SUB A,k	k-A → A	Z,C,DC
1	1110	0000	0001	1E01	INT	PC+1 → [SP] 001H → PC	None
1	1110	1000	0kkk	1E8k	PAGE k	K->R5	None
1	1111	kkkk	kkkk	1Fkk	ADD A,k	k+A → A	Z,C,DC

CODE Option Register

The IC has one CODE option register which is not part of the normal program memory. The option bits cannot be accessed during normal program execution.

7	6	5	4	3	2	1	0
-	-	-	-	-	-	/POVD	-

* Bit 0 : unused, must be "0".

* **Bit 0 : (/POVD) : Power on voltage detector.**

0: enable

1: disable

	2.0V POVD reset	1.6V power on reset	2.5V voltage detect no reset	sleep mode current
1	no	yes	no	1uA typical
0	yes	yes	yes	10uA typical

* Bits 1~7 : unused, must be "0"s.

VII.8 LCD Driver

The CALLER ID IC can drive LCD directly and has 60 segments and 16 commons that can drive 60*16 dots totally. LCD block is made up of LCD driver , display RAM, segment output pins , common output pins and LCD operating power supply pins.

Duty , bias , the number of segment , the number of common and frame frequency are determined by LCD mode register . LCD control register.

The basic structure contains a timing control which uses the basic frequency 32.768KHz to generate the proper timing for different duty and display access. RE register is a command register for LCD driver, the LCD display(disable, enable, blanking) is controlled by LCD_C and the driving duty and bias is decided by LCD_M and the display data is stored in data RAM which address and data access controlled by registers RC and RD.

* This specification are subject to be changed without notice.

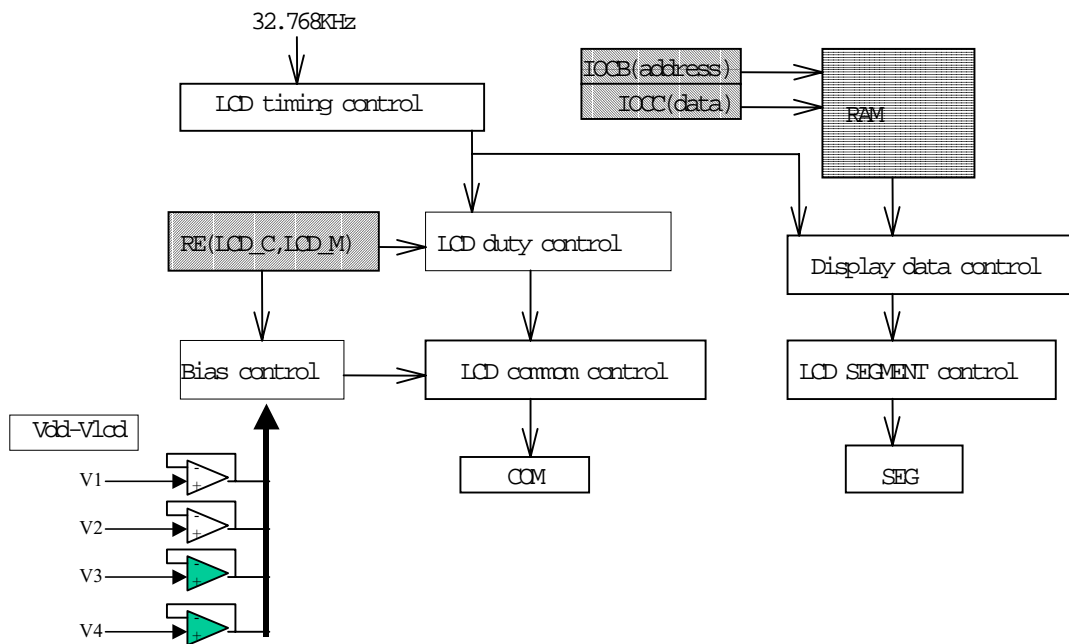


Fig.17 LCD DRIVER CONTROL

VII.8.1 LCD Driver Control

1. RE(LCD Driver Control)(initial state "00000000")

7	6	5	4	3	2	1	0
-	-	-	-	-	LCD_C2	LCD_C1	LCD_M

*Bit0 (LCD_M):LCD_M decides the methods, including duty, bias, and frame frequency.

*Bit1~Bit2 (LCD_C#):LCD_C# decides the LCD display enable or blanking. change the display duty must set the LCD_C to "00".

LCD_C2,LCD_C1	LCD Display Control	LCD_M	duty	bias
0 0	change duty Disable(turn off LCD)	0 1	1/16 1/8	1/4 1/4
0 1	Blanking	:	:	:
1 1	LCD display enable	:	:	:

VII.8.2 LCD display area

The LCD display data is stored in the data RAM . The relation of data area and COM/SEG pin is as below:

COM15 ~ COM8	COM7 ~ COM0	
40H (Bit15 ~ Bit8)	00H (Bit7 ~ Bit0)	SEG0
41H	01H	SEG1
:	:	:
:	:	:
67H	27H	SEG39
:	:	empty
7DH	3DH	empty
7EH	3EH	empty
7FH	3FH	empty

*IOCB(LCD Display RAM address)

7	6	5	4	3	2	1	0
-	LCDA6	LCDA5	LCDA4	LCDA3	LCDA2	LCDA1	LCDA0

Bit 0 ~ Bit 6 select LCD Display RAM address up to 127.

LCD RAM can be write whether in enable or disable mode and read only in disable mode.

*IOCC(LCD Display data) : Bit 0 ~ Bit 8 are LCD data.

VII.8.3 LCD COM and SEG signal

* COM signal : The number of COM pins varies according to the duty cycle used, as following: in 1/8 duty mode COM8 ~ COM15 must be open. in 1/16 duty mode COM0 ~ COM15 pins must be used.

	COM0	COM1	COM2	COM3	COM4	COM5	COM6	COM7	COM8	..	COM15
1/8	o	o	o	o	o	o	o	o	x	..	x
1/16	o	o	o	o	o	o	o	o	o	..	o

x:open,o:select

* SEG signal: The 60 segment signal pins are connected to the corresponding display RAM address 00h to 3Bh. The high byte and the low byte bit7 down to bit0 are correlated to COM15 to COM0 respectively .
When a bit of display RAM is 1, a select signal is sent to the corresponding segment pin, and when the bit is 0 , a non-select signal is sent to the corresponding segment pin.

*COM, SEG and Select/Non-select signal is shown as following:

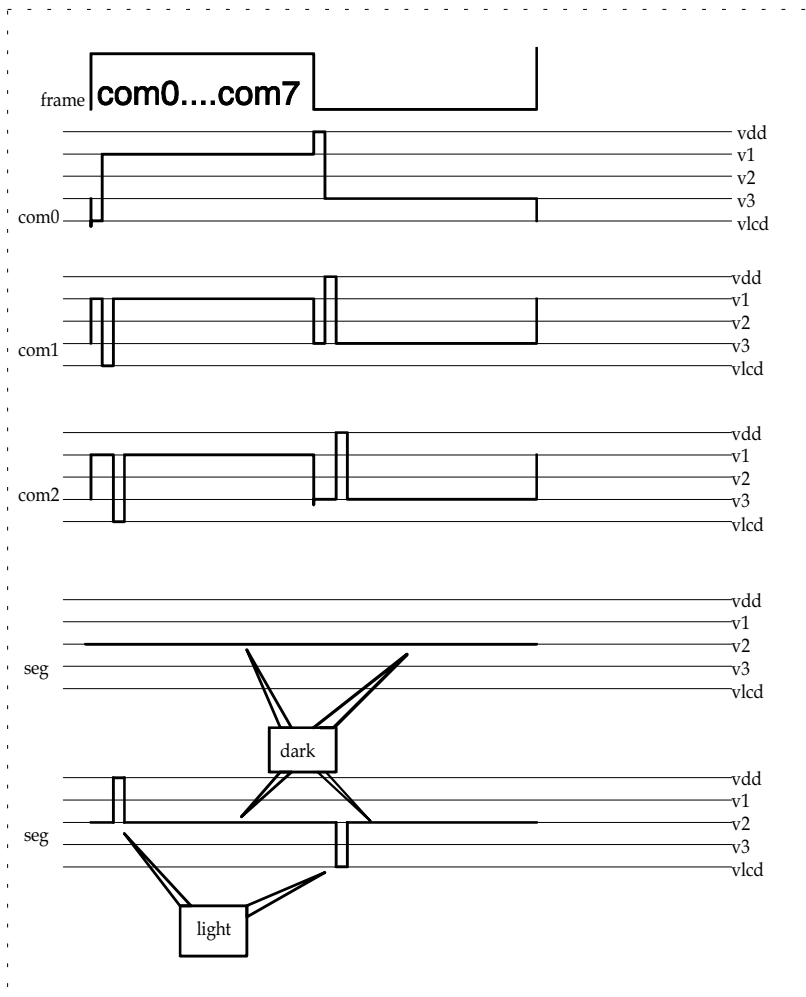


Fig.18 Lcd wave 1/4 bias , 1/8 duty

* This specification are subject to be changed without notice.

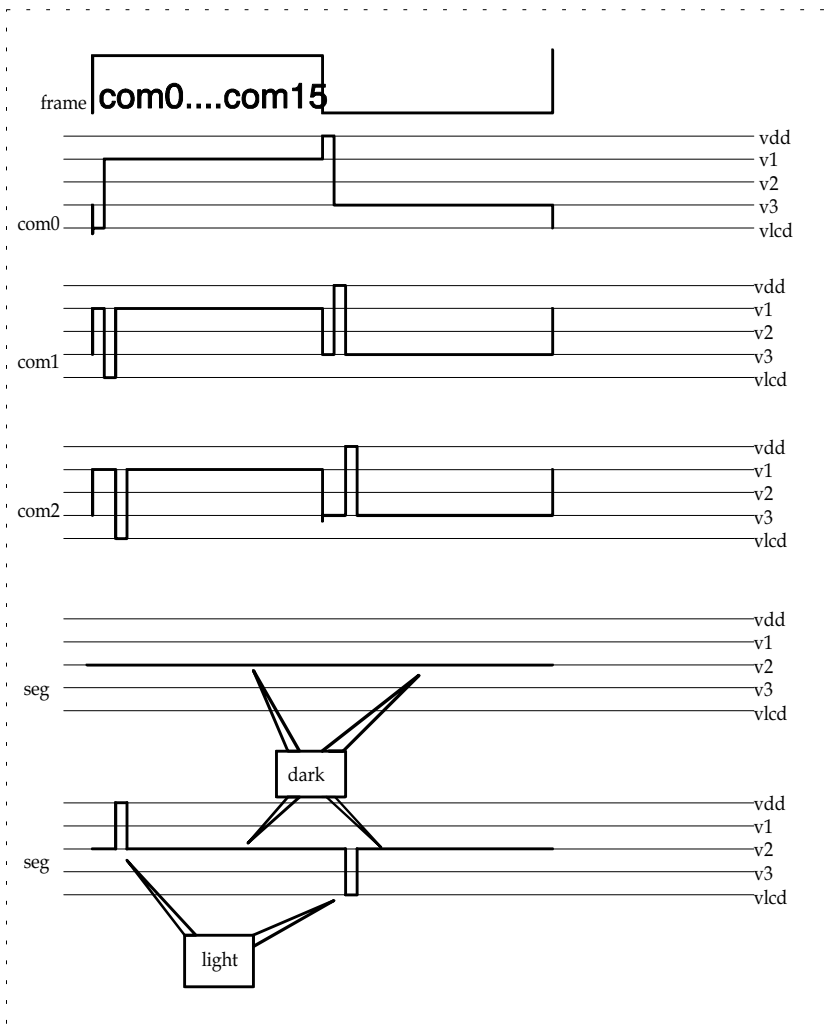


Fig.19 Lcd wave 1/4 bias , 1/16 duty



VIII. Absolute Operation Maximum Ratings

RATING	SYMBOL	VALUE	UNIT
DC SUPPLY VOLTAGE	Vdd	-0.3 To 3.6	V
INPUT VOLTAGE	Vin	-0.3 TO Vdd +0.3	V
OPERATING TEMPERATURE RANGE	Ta	0 TO 70	°C

IX DC Electrical Characteristic

(Ta=0°C ~ 70°C, VDD=3.3V±5%, VSS=0V)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
IIL1	Input Leakage Current for input pins	VIN = VDD, VSS			±1	µA
IIL2	Input Leakage Current for bi-directional pins	VIN = VDD, VSS			±1	µA
VIH	Input High Voltage		2.5			V
VIL	Input Low Voltage				0.8	V
VIHT	Input High Threshold Voltage	/RESET, TCC, RDET1	2.0			V
VILT	Input Low Threshold Voltage	/RESET, TCC, RDET1			0.8	V
VIHX	Clock Input High Voltage	OSCI	3.5			V
VILX	Clock Input Low Voltage	OSCI			1.5	V
VHscan	Key scan Input High Voltage	Port6 for key scan	3.5			V
VLscan	Key scan Input Low Voltage	Port6 for key scan			1.5	V
VOH1	Output High Voltage (port6,7,8)	IOH = -1.6mA	2.4			V
	(port9)	IOH = -6.0mA	2.4			V
VOL1	Output Low Voltage (port6,7,8)	IOL = 1.6mA			0.4	V
	(port9)	IOL = 6.0mA			0.4	V
Vcom	Com voltage drop	Io=+/- 50 uA	-	-	2.9	V
Vseg	Segment voltage drop	Io=+/- 50 uA	-	-	3.8	V
Vlcd	LCD drive reference voltage	Contrast adjustment				
IPH	Pull-high current	Pull-high active input pin at VSS		-10	-15	µA
ISB1	Power down current (SLEEP mode) POVD disable	All input and I/O pin at VDD, output pin floating, WDT disabled		1	2	µA
	Power down current (SLEEP mode) POVD enable			6	15	uA
ISB2	Low clock current (GREEN mode) POVD disable	CLK=32.768KHz, TONE block disable , All input and I/O pin at VDD, output pin floating, WDT disabled, LCD enable		30	45	µA
	Low clock current (GREEN mode) POVD enable			35	55	uA
ISB3	Low clock current (IDLE mode) POVD disable	CLK=32.768KHz, TONE block disable , All input and I/O pin at VDD, output pin floating, WDT disabled, LCD enable		25	40	µA
	Low clock current (IDLE mode) POVD enable			30	50	uA

* This specification are subject to be changed without notice.



ICC1	Operating supply current (CPU enable)	/RESET=High, CLK=3.579MHz, output pin floating		0.8	1.1	mA
Vref2	Tone generator reference voltage		0.5		0.7	VDD
Vmax	Tone1 signal strength	Root mean square voltage	130	155	180	mV
Vmax	Tone2 signal strength	Root mean square voltage	150	175	200	mV
Ibuf	One LCD bias buffer current			4	6	μA
Rbias	LCD bias resistor		300	400	500	KΩ

IX AC Electrical Characteristic

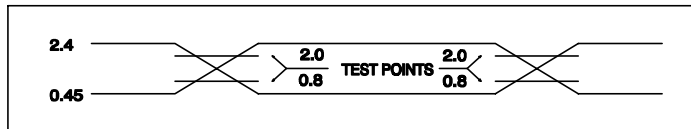
(Ta=0°C ~ 70°C, VDD=3.3V, VSS=0V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dclk	Input CLK duty cycle		45	50	55	%
Tins	Instruction cycle time	32.768kHz 3.579MHz		60 550		us ns
Tdrh	Device delay hold time			18		ms
Ttcc	TCC input period	Note 1	(Tins+20)/ N			ns
Twdt	Watchdog timer period	Ta = 25°C		18		ms

Note 1: N= selected prescaler ratio.

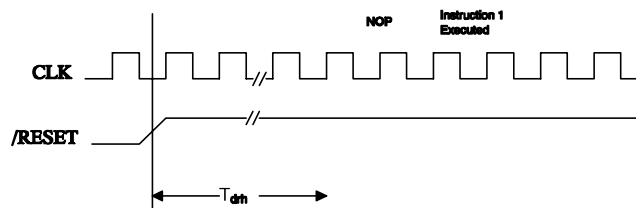
XI. Timing Diagrams

AC Test Input/Output Waveform



AC Testing: Input are driven at 2.4V for logic "1", and 0.45V for logic "0". Timing measurements are made at 2.0V for logic "1", and 0.8V for logic "0".

RESET Timing



TCC Input Timing

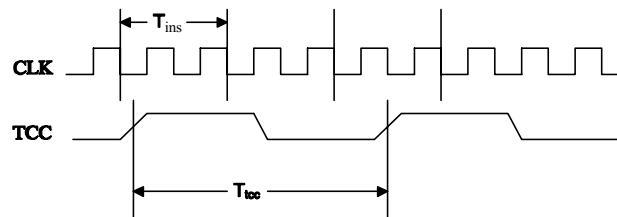


Fig.20 AC timing

XII. Application Circuit

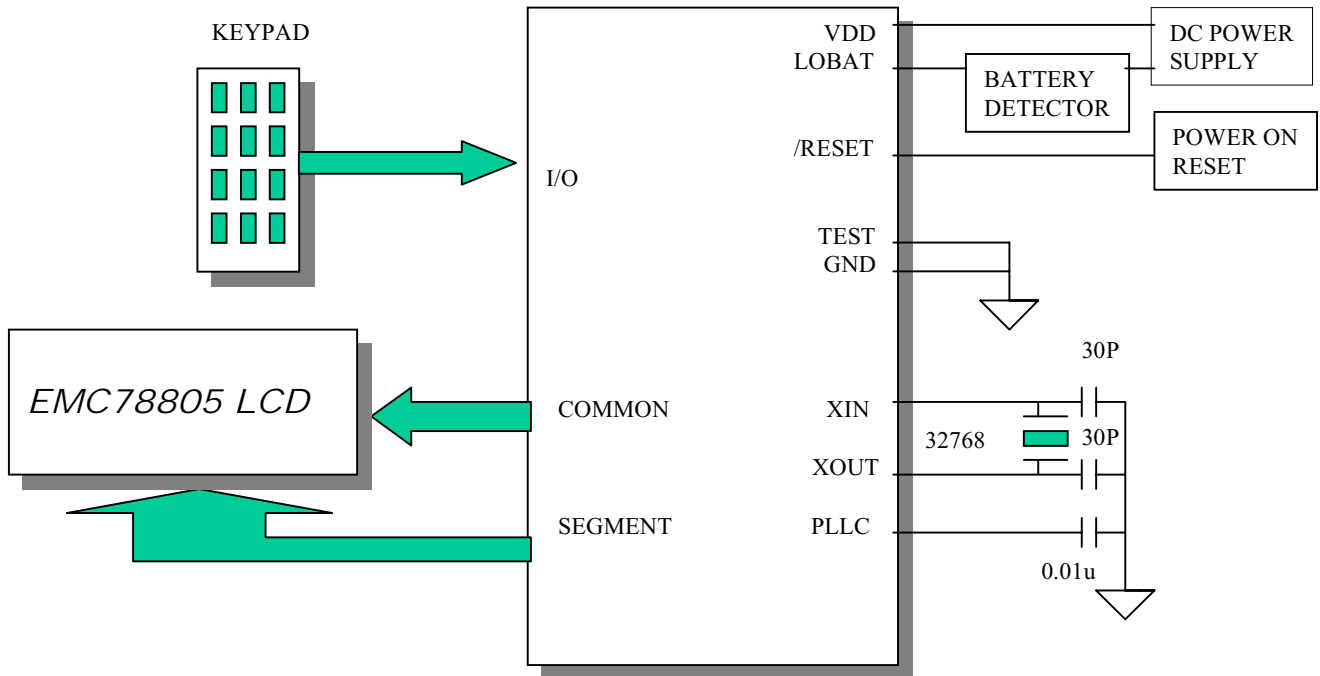


Fig.23 application circuit

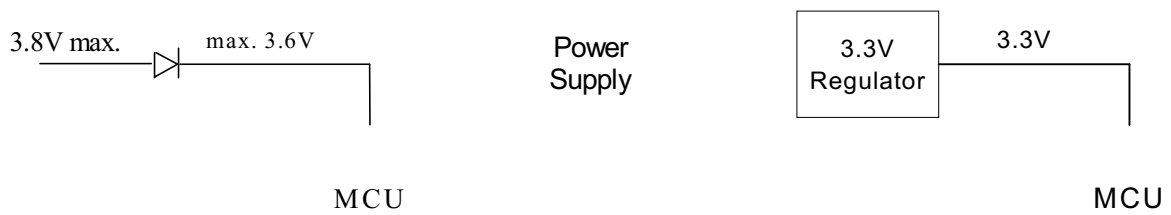


Fig.24 Power Concern in Application