SONY

CXP80316

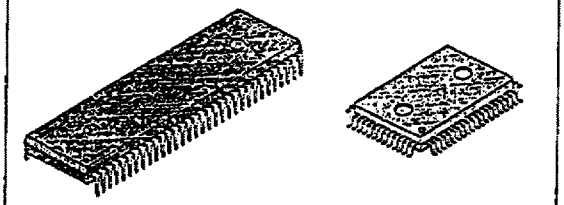
CMOS 8-bit Single Chip Microcomputer

Description

The CXP80316 is a CMOS 8-bit single chip microcomputer featuring on-chip integration of serial interface, timer/counter, 16-bit capture timer/counter, time base timer, and vector interruption circuit, besides the basic configuration of 8-bit CPU, ROM, RAM, and I/O port.

The CXP80316 also provides a power-on reset function and a sleep/stop function which enables lower power consumption.

64pin SDIP (Plastic) 64pin QFP (Platic)



Features

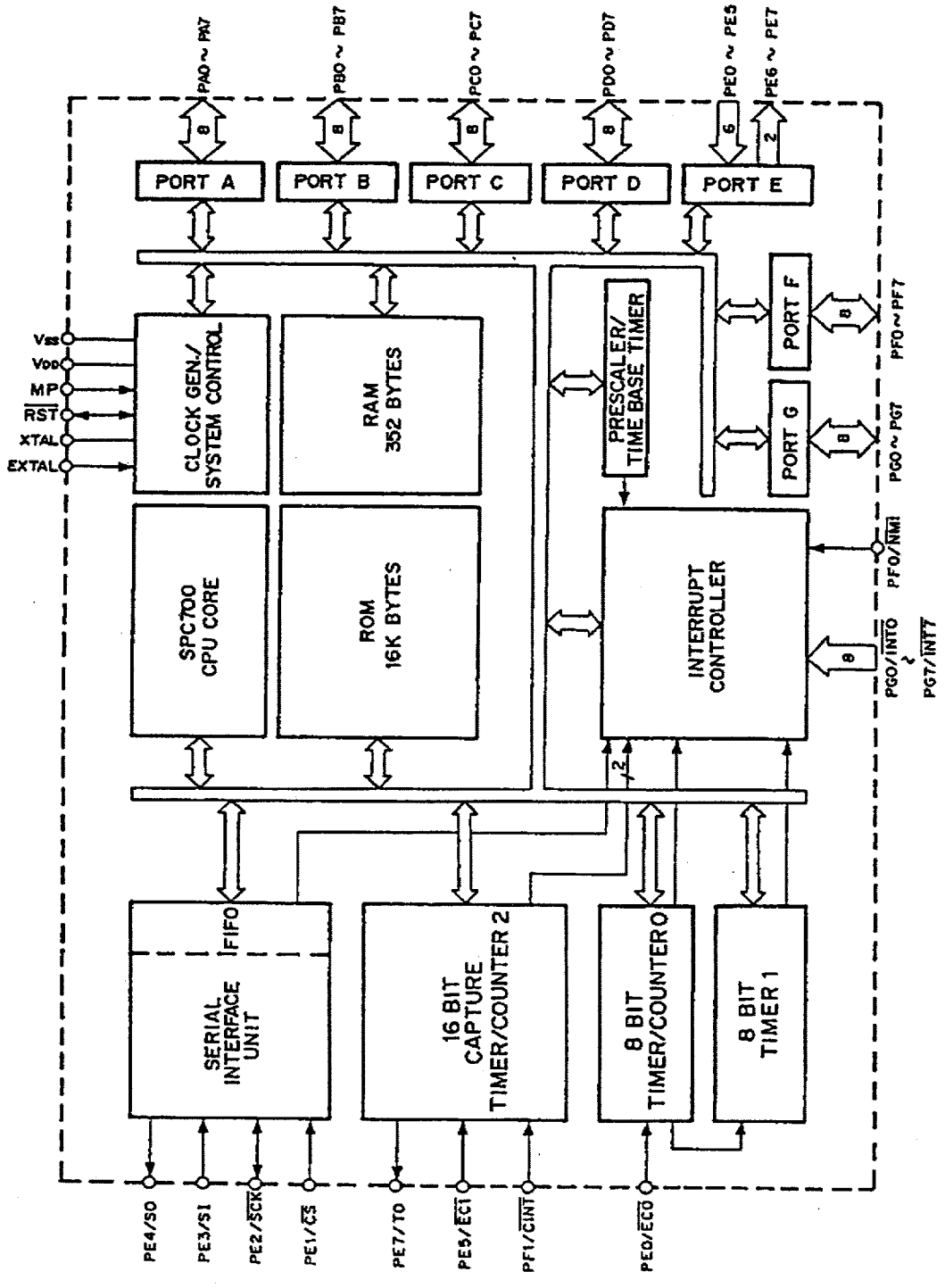
- Wide-range instruction system (213 instructions) to cover various types of data
  —16-bit arithmetic/multiplication and division/Boolean bit operation instructions
- Minimum instruction cycle 500ns at 8MHz operation
- Incorporated ROM capacity 16 Kbytes
- Incorporated RAM capacity 352 bytes
- Peripheral functions
  —Serial I/O with automatic transfer mode On-chip 8-bit, 8-stage FIFO for data (Auto transfer for 1 to 8 bytes)
  —Timer 8-bit timer, 8-bit timer/counter, 19-bit time base timer 16-bit capture timer/counter (Monostable multivibrator output, rectangular wave output possible)
- Interruption 15 factors, 15 vectors, multi-interruption possible
- Standby mode SLEEP/STOP
- Package 64-pin plastic SDIP/QFP
- Piggyback/evaluation chip CXP80300

Structure

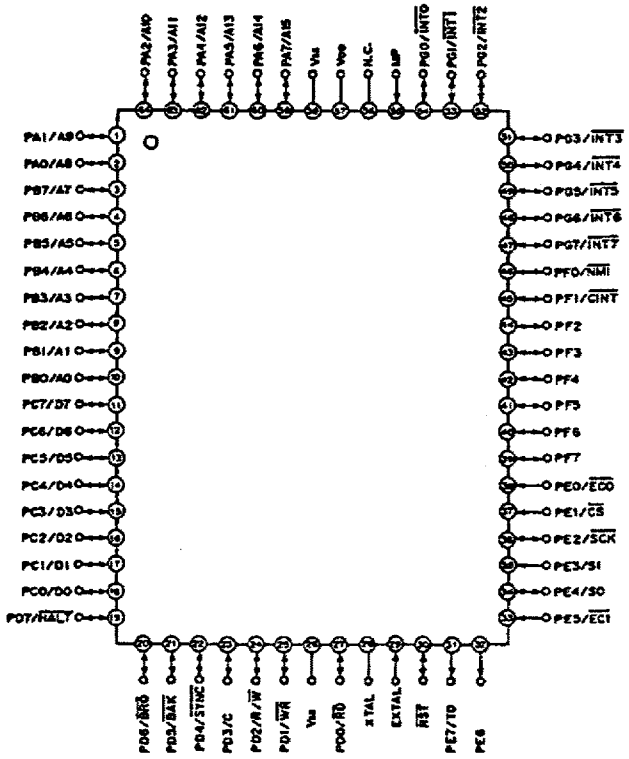
Silicon gate CMOS IC

E89528-HP

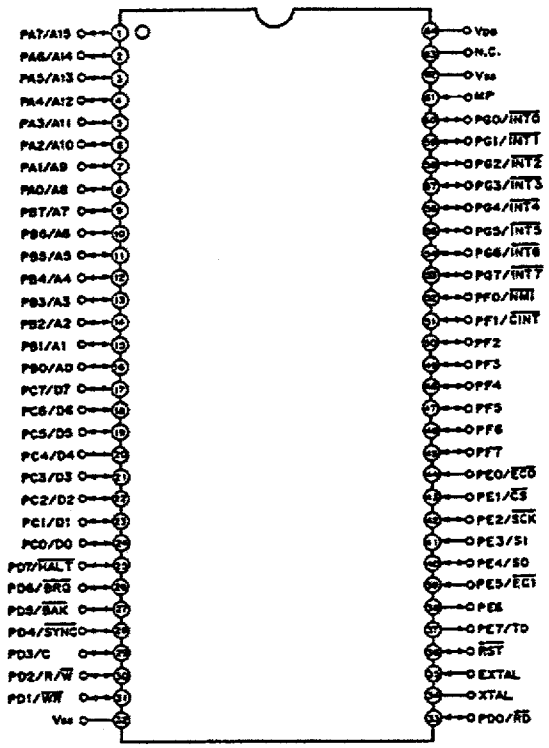
Block Diagram



Pin Configuration (Top View)



Note) 1. N.C. (Pin 56) must be connected to V_{DD}.
2. V_{SS} of both Pins 26 and 58 are grounded.

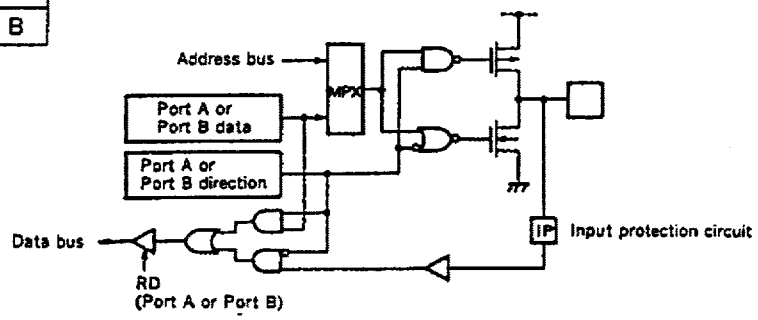
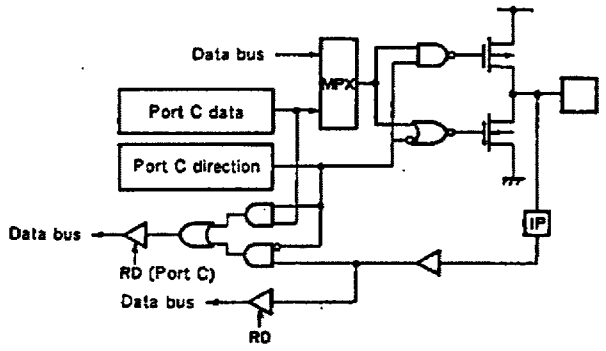
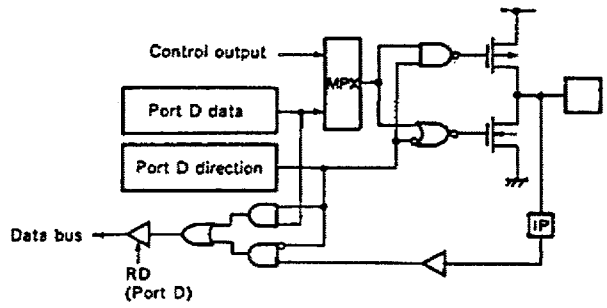
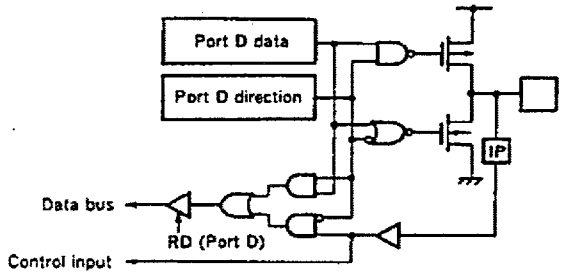


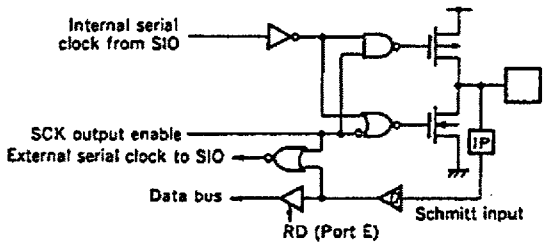
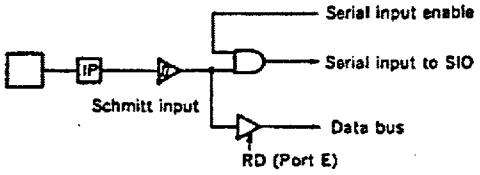
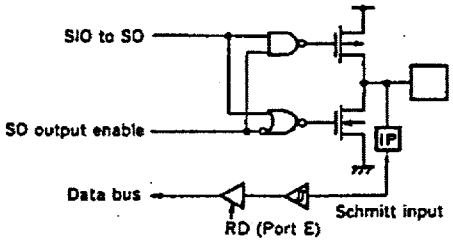
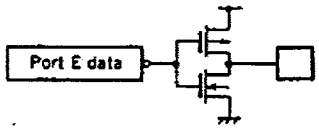
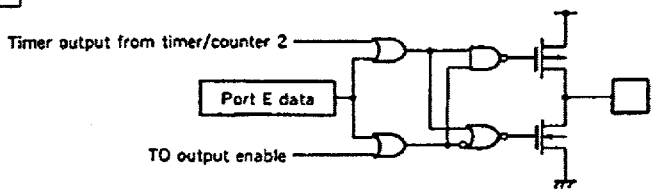
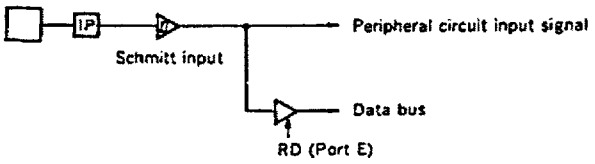
Note) 1. N.C. (Pin 63) must be connected to V_{DD}.
2. V_{SS} of both Pins 32 and 62 are grounded.

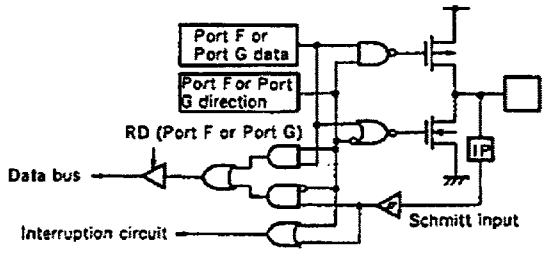
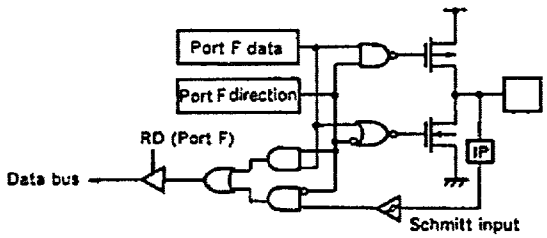
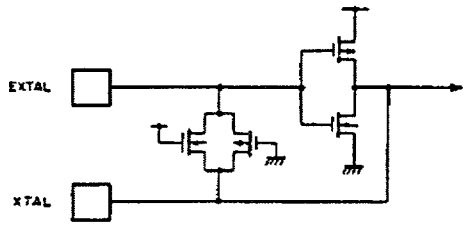
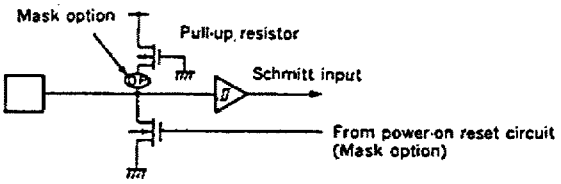
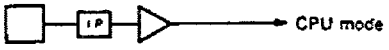
Pin Description

Symbol	I/O	Description	
PA0/A8 ⟆ PA7/A15	I/O/output	(Port A) 8-bit I/O port. I/O can be set in a unit of single bits. (8 pins)	Functions as an address bus to the external memory when in the memory extension mode and microprocessor mode. (16 pins)
PB0/A0 ⟆ PB7/A7	I/O/output	(Port B) 8-bit I/O port. I/O can be set in a unit of single bits. (8 pins)	
PC0/D0 ⟆ PC7/D7	I/O/I/O	(Port C) 8-bit I/O port. I/O can be set in a unit of single bits. (8 pins)	Functions as a data bus to the external memory when in the memory extension mode and microprocessor mode. (8 pins)
PD0/$\overline{RD}$	I/O/output	(Port D) 8-bit I/O port. I/O can be set in a unit of single bits. (8 pins)	Strobe signal for the external memory read operation. Enabled at "Low."
PD1/$\overline{WR}$	I/O/output		Strobe signal for the external memory write operation. Enabled at "Low."
PD2/R/$\overline{W}$	I/O/output		"High" when the machine cycle of the CPU is in read cycle, "Low" when in write cycle.
PD3/C	I/O/output		Timing signal output.
PD4/$\overline{SYNC}$	I/O/output		"Low" when CPU is in opecode fetch cycle.
PD5/$\overline{BAK}$	I/O/output		"Low" when CPU receives bus request ($\overline{BRQ}$). Simultaneously, the address output, data I/O, $\overline{RD}$, $\overline{WR}$, and R/$\overline{W}$ are in high impedance state.
PD6/$\overline{BRQ}$	I/O/input		Bus request input to CPU.
PD7/$\overline{HALT}$	I/O/input		Input to stop CPU operation.

Symbol	I/O	Description	
PE0/$\overline{ECO}$	Input/input	(Port E) 8-bit port. Lower 6 bits are inputs and upper 2 bits are outputs. (8 pins)	External event input to 8-bit timer/counter
PE1/$\overline{CS}$	Input/input		Chip select input to serial interface
PE2/$\overline{SCK}$	Input/I/O		I/O for serial clock
PE3/SI	Input/input		Serial data input
PE4/SO	Input/output		Serial data output
PE5/$\overline{EC1}$	Input/input		External event input to 16-bit timer/counter
PE6	Output		—
PE7/TO	Output/output		Timer output to 16-bit timer/counter
PF0/$\overline{NMI}$	I/O/input	(Port E) 8-bit I/O port. I/O can be set in a unit of single bits. (8 pins)	Non-maskable interruption request, active at falling edge
PF1/$\overline{CINT}$	I/O/input		External capture input to 16-bit timer/counter
PF2 $\sim$ PF7	I/O		—
PG0/$\overline{INT0}$ $\sim$ PG7/$\overline{INT7}$	I/O/input	(Port G) 8-bit I/O port. I/O can be set in a unit of single bits. (8 pins)	External interruption request, active at falling edge
EXTAL	Input	Connection to the crystal for the system clock oscillator. When externally supplying clock, input to EXTAL and set XTAL to open.	
XTAL	Output		
$\overline{RST}$	I/O	"Low" level active, system reset pin. $\overline{RST}$ is an I/O from which "Low" level is output when the built-in power on reset function operates at the rise of power on. (Mask option)	
MP	Input	Microprocessor mode input. Microprocessor mode when input at "High" level; single-chip mode when input at "Low" level.	
V_{DD}		Positive power supply	
V_{SS}		GND	

Pin	Circuit format	When reset
PA0/AS ⌇ PA7/A15 PB0/A0 ⌇ PB7/A7 16 pins	Port A Port B 	Hi-Z
PC0/D0 ⌇ PC7/D7 8 pins	Port C 	Hi-Z
PD0/$\overline{RD}$ PD1/$\overline{WR}$ PD2/R/$\overline{W}$ PD3/C PD4/$\overline{SYNC}$ PD5/$\overline{BAK}$ 6 pins	Port D 	Hi-Z
PD6/$\overline{BRQ}$ PD7/$\overline{HALT}$ 2 pins	Port D 	Hi-Z

Pin	Circuit format	When reset
PE2/$\overline{SCK}$ 1 pins	Port E 	Hi-Z
PE3/SI 1 pins	Port E 	Hi-Z
PE4/SO 1 pins	Port E 	Hi-Z
PE6 1 pins	Port E 	High level
PE7/TO 1 pins	Port E 	High level
PE0/$\overline{ECO}$ PE1/$\overline{CS}$ PE5/$\overline{ECI}$ 3 pins	Port E 	Hi-Z

Pin	Circuit format	When reset
PF0/$\overline{NMI}$ PF1/$\overline{CINT}$ PG0/$\overline{INT0}$ 〜 PG7/$\overline{INT7}$ 10 pins	Port F Port G 	Hi-Z
PF2 〜 PF7 6 pins	Port F 	Hi-Z
EXTAL XTAL 2 pins	 • Diagram shows the circuit composition during oscillation. • Feedback resistor is removed during stop.	Oscillation
$\overline{RST}$ 1 pins		Low levl
MP 1 pins		Hi-Z

Absolute Maximum Ratings (V_{SS} = 0V)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	V_{DD}	−0.3 to +7.0	V	
Input voltage	V_{IN}	−0.3 to +7.0*1	V	
Output voltage	V_{OUT}	−0.3 to +7.0*1	V	
High level output current	I_{OH}	−5	mA	
High level total output current	ΣI_{OH}	−50	mA	Total of all outputs
Low level output current	I_{OL}	15	mA	Current output per pin, excluding those of high currents
	I_{OLC}	20	mA	High current outputs*2
Low level total output current	ΣI_{OL}	130	mA	Total of all outputs
Operating temperature	T_{opr}	−20 to +75	°C	
Storage temperature	T_{stg}	−55 to +150	°C	
Allowable power dissipation	P_D	600	mW	QFP
		1000		SDIP

*1) V_{IN} and V_{OUT} should not exceed V_{DD} + 0.3V.
*2) The high current operation transistor is the N-ch transistor for PD.
Note) Usage exceeding the absolute maximum ratings may permanently impair the LSI. Also, normal operation should be conducted under the recommended operating conditions. Exceeding these conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions (V_{SS} = 0V)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V_{DD}	4.5	5.5	V	Guaranteed operation range
		2.5	5.5		Guaranteed data hold operation range during STOP
High level input voltage	V_{IH}	$0.7V_{DD}$	V_{DD}	V	*1
	V_{IHS}	$0.8V_{DD}$	V_{DD}	V	CMOS schmitt input*2
	V_{IHEX}	$V_{DD}-0.4$	$V_{DD}+0.3$	V	EXTAL*3
Low level input voltage	V_{IL}	0	$0.3V_{DD}$	V	*1
	V_{ILS}	0	$0.2V_{DD}$	V	CMOS schmitt input*2
	V_{ILEX}	−0.3	0.4	V	EXTAL*3
Operating temperature	T_{opr}	−20	+75	°C	

*1) Normal input port (Pins PA to PD), Pin MP
*2) Pins PE0 to PE5, PF, PG, and $\overline{RST}$
*3) Specifies only during external clock input.

DC Characteristics (Ta = −20 to +75°C, V_{SS} = 0V)

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA to PD, PE2,PE4,PE6,PE7, PF to PG, $\overline{RST}$*1 (V_{OL} only)	V_{DD}=4.5V I_{OH}=−0.5mA	4.0			V
			V_{DD}=4.5V I_{OH}=−1.2mA	3.5			V
Low level output voltage	V_{OL}		V_{DD}=4.5V I_{OL}=1.8mA			0.4	V
			V_{DD}=4.5V I_{OL}=3.6mA			0.6	V
		PD	V_{DD}=4.5V I_{OL}=12.0mA			1.5	V
Input current	I_{IHE}	EXTAL	V_{DD}=5.5V V_{IH}=5.5mA	0.5		40	μA
	I_{ILE}		V_{DD}=5.5V I_{IL}=0.4V	−0.5		−40	μA
	I_{ILR}	$\overline{RST}$*2	V_{DD}=5.5V I_{IL}=0.4V	−1.5		−400	μA
I/O leak current	I_{IZ}	PA to PG, $\overline{NMI}$, $\overline{RST}$*2, MP	V_{DD}=5.5V V_I=0, 5.5V			±3	μA
Supply current	I_{DD}	V_{DD}	Operation mode (1/2 frequency demultiplier clock) 8MHz crystal oscillation (C_1 = C_2 = 15pF) All outputs open V_{DD} = 5.5V		20	40	mA
	I_{DDSL}		SLEEP mode		1	5	mA
	V_{DDST}		STOP mode			10	μA
Input capacity	C_{IN}	Excluding V_{DD} and V_{SS}	1MHz clock All pins at 0V, except measured pins		10	20	PF

*1) $\overline{RST}$ specifies only when the power-on reset circuit has been selected by mask option.
*2) $\overline{RST}$ specifies for input current when the pull-up resistance has been selected, and leak current when no resistance has been selected.

AC Characteristics

(1) Clock timing (Ta = −20 to +75°C, V_{DD} = 4.5 to 5.5V, V_{SS} = 0V)

Item	Symbol	Pin	Conditions	Min.	Max.	Unit
System clock frequency	f_C	XTAL EXTAL	Fig. 1, Fig. 2	1	8	MHz
System clock input pulse width	f_{XL} t_{XH}	EXTAL	Fig. 1, Fig. 2 External clock drive	50		ns
System clock input rise time, fall time	t_{CR} t_{CF}	EXTAL	Fig. 1, Fig. 2 External colck drive		200	ns
Event count input clock pulse width	t_{EH}, t_{EL}	$\overline{EC0}$ $\overline{EC1}$	Fig. 3	*1 t_{sys}+50		ns
Event count input clock rise time, fall time	t_{ER}, t_{EF}	$\overline{EC0}$ $\overline{EC1}$	Fig. 3		20	ms

*1) t_{sys} indicates the three values below according to the upper two bits (CPU clock selection) of the clock control register (address: $00FE_H$).
t_{sys}[ns] = 2000/fc (upper two bits = "00"), 4000/fc (upper two bits = "01"), 16000/fc (upper two bits = "11")

Fig. 1 Clock timing

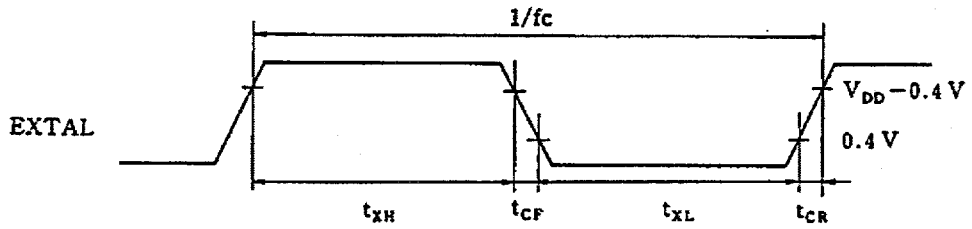


Fig. 2 Clock applying condition

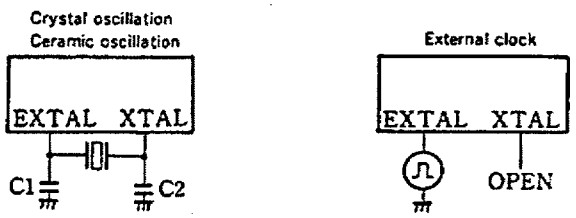
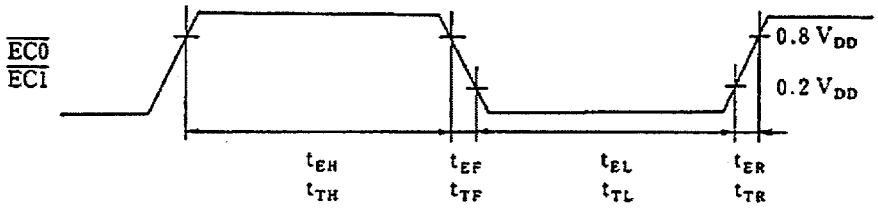


Fig. 3 Event count clock timing



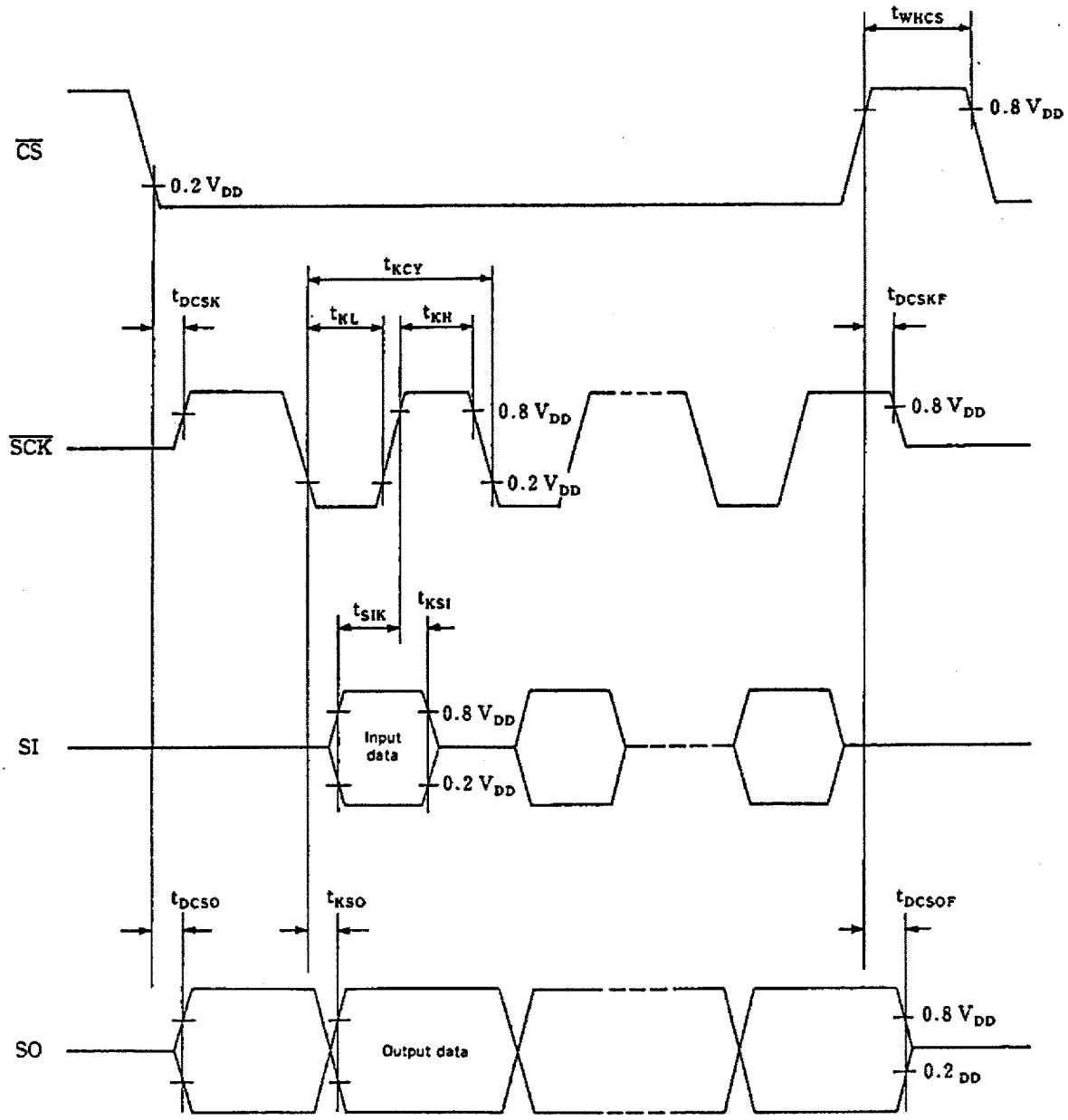
(2) Serial transfer (Ta = −20 to +75°C, V_{DD} = 4.5 to 5.5V, V_{SS} = 0V)

Item	Symbol	Pin	Conditions	Min.	Max.	Unit
$\overline{CS}$ ↓ → $\overline{SCK}$ delay time	t_{DCSK}	$\overline{SCK}$	Chip select transfer mode ($\overline{SCK}$ = output mode)		t_{sys}+200	ns
$\overline{CS}$ ↑ → $\overline{SCK}$ floating delay time	t_{DCSKF}	$\overline{SCK}$	Chip select transfer mode ($\overline{SCK}$ = output mode)		t_{sys}+200	ns
$\overline{CS}$ ↓ → SO delay time	t_{DCSO}	SO	Chip select transfer mode		t_{sys}+200	ns
$\overline{CS}$ ↑ → SO floating delay time	t_{DCSOF}	SO	Chip select transfer mode		t_{sys}+200	ns
$\overline{CS}$ high level width	t_{WHCS}	$\overline{CS}$	Chip select transfer mode	t_{sys}+200		ns
$\overline{SCK}$ cycle time	t_{KCY}	$\overline{SCK}$	Input mode	$2t_{sys}$+200		ns
			Output mode	8000/fc		ns
$\overline{SCK}$ high, low level width	t_{KH}	$\overline{SCK}$	Input mode	t_{sys}+100		ns
	t_{KL}		Output mode	4000/fc−50		ns
SI input set up time (for $\overline{SCK}$ ↑)	t_{SIK}	SI	$\overline{SCK}$ input mode	100		ns
			$\overline{SCK}$ output mode	200		ns
SI input hold time (for $\overline{SCK}$ ↑)	t_{KIS}	SI	$\overline{SCK}$ input mode	t_{sys}+200		ns
			$\overline{SCK}$ output mode	100		ns
$\overline{SCK}$ ↓ → SO delay time	t_{KSO}	SO	$\overline{SCK}$ input mode		t_{sys}+200	ns
			$\overline{SCK}$ output mode		100	ns

Note 1) t_{sys} indicates the three values below according to the upper two bits (CPU clock selection) of the clock control register (address : $00FE_H$).
t_{sys}[ns] = 2000/fc (upper two bits = "00"), 4000/fc (upper two bits = "01"), 16000/fc (upper two bits = "11")

Note 2) The load condition for $\overline{SCK}$ output mode and SO output delay time is 50 pF + 1TTL.

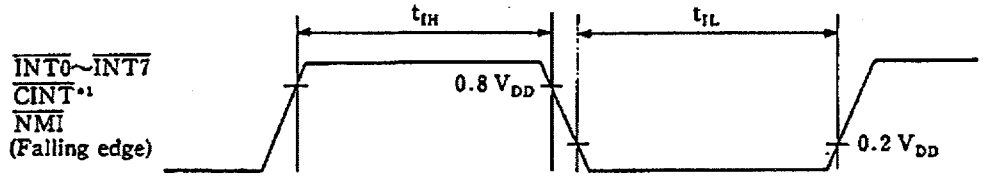
Fig. 4 Serial transfer timing



(3) Interruption, reset input (Ta = −20 to +75°C V_{DD} = 4.5 to 5.5V, V_{SS} = 0V)

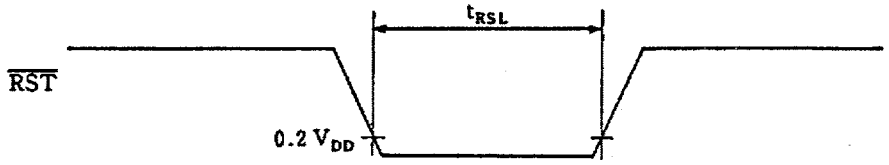
Item	Symbol	Pin	Conditions	Min.	Max.	Unit
External interruption high, low level width	t_{IH} t_{IL}	$\overline{INT0}$ to $\overline{INT7}$ $\overline{CINT}$ $\overline{NMI}$		1		μs
Reset input low level width	t_{RSL}	$\overline{RST}$		8/fc		μs

Fig. 5 Interruption input timing



*1) $\overline{CINT}$ input enables rise/fall switching using Bit 4 of the mode register for timer/counter 2. (Rising edge input when Bit 4 = "0," falling edge input when Bit 4 = "1")

Fig. 6 $\overline{RST}$ input timing



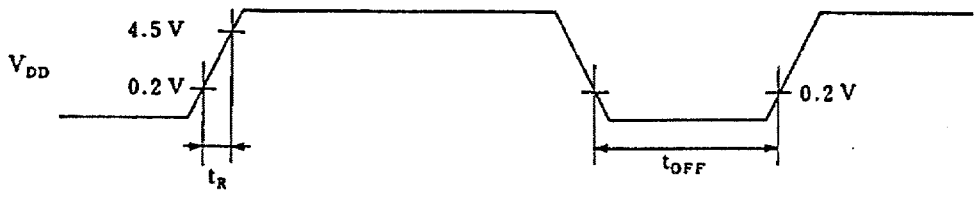
(4) Power-on reset

Power-on reset * (Ta = −20 to +75°C, V_{DD} = 4.5 to 5.5V, V_{SS} = 0V)

Item	Symbol	Pin	Conditions	Min.	Max.	Unit
Power supply rise time	t_R	V_{DD}	Power-on reset	0.05	50	ms
Power supply cut-off time	t_{OFF}		Repetitive power-on reset	1		ms

*Specifies only when the power-on reset function has been selected.

Fig. 7 Power-on reset



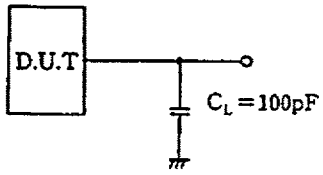
The power supply should be raised smoothly.

(5) Memory extension mode, microprocessor mode input/output timing

(Ta = −20 to +75°C, V_{DD} = 4.5 to 5.5V, V_{SS} = 0V)

Item	Symbol	Pin	Conditions	Min.	Max.	Unit
Control clock output (C) high, low level width	t_{CWL} t_{CWH}	C	Fig. 8	90		ns
High address (A15 to A8) output delay time	t_{CAHD}	A15 to A8			80	ns
Low address (A7 to A0) output delay time	t_{CALD}	A7 to A0			80	ns
Data (D7 to D0) output delay time	t_{CWD}	D7 to D0			$\frac{1}{2}t_{CYC}$ +75	ns
Data (D7 to D0) output hold time	t_{WDHD}				15	ns
Data (D7 to D0) input set-up time	t_{RDS}			80		ns
Data (D7 to D0) input hold time	t_{RDHD}			15		ns
Read pulse ($\overline{RD}$) output delay time	t_{RDD}	$\overline{RD}$			$\frac{1}{4}t_{CYC}$ +27.5	ns
Write pulse ($\overline{WD}$) output delay time	t_{WRD}	$\overline{WR}$			$\frac{1}{2}t_{CYC}$ +5	ns
Read/write pulse (R/$\overline{W}$) output delay time	t_{RWD}	R/$\overline{W}$			50	ns
Sync pulse ($\overline{SYNC}$) output delay time	t_{SYD}	$\overline{SYNC}$			50	ns

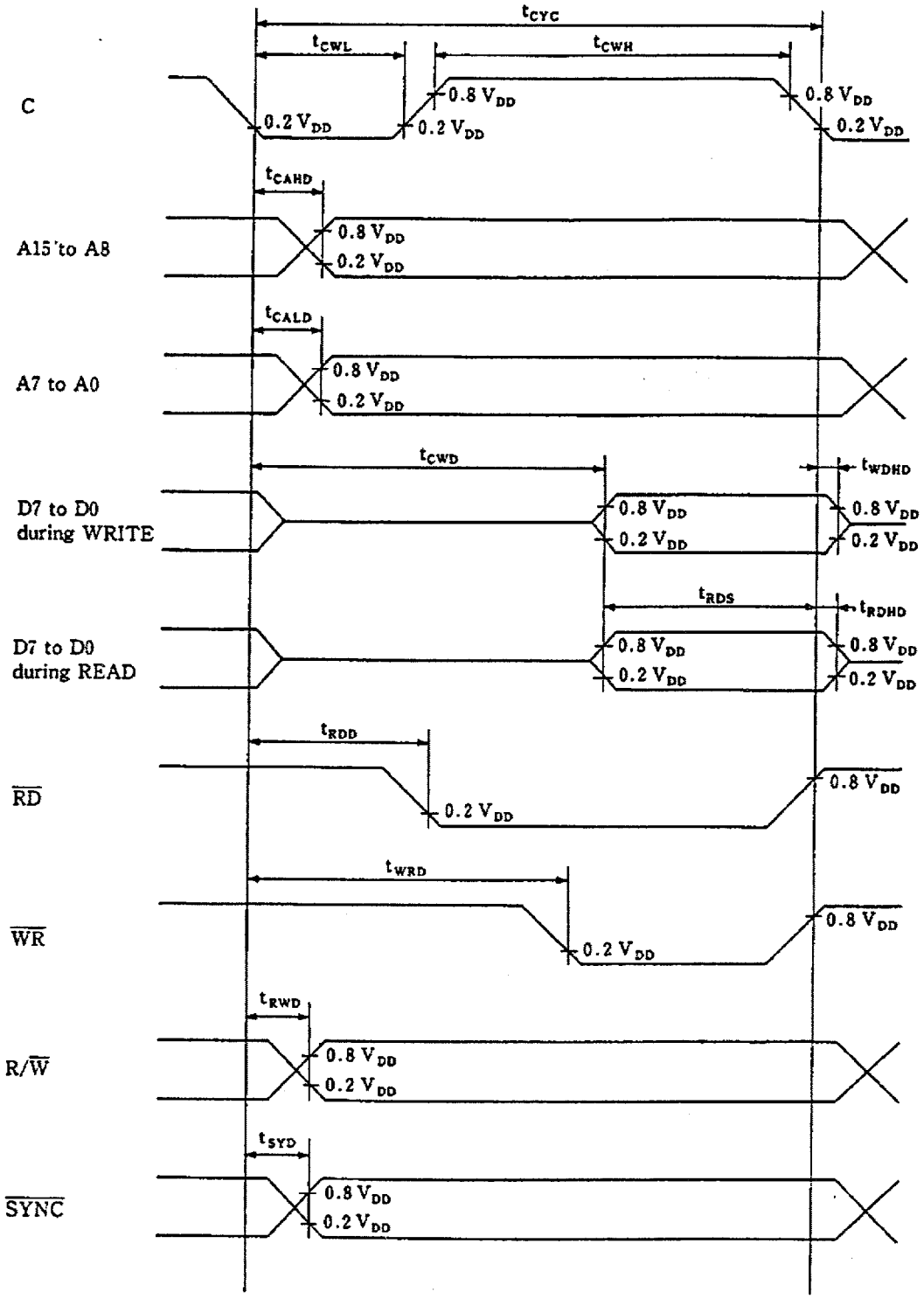
Fig. 8 Load conditions



(For all of Pins A0 to A15, D0 to D7, C, $\overline{RD}$, $\overline{WR}$, R/$\overline{W}$, $\overline{SYNC}$, $\overline{BAK}$.)

Note) t_{sys} indicates the four values below according to Bits 5 and 4 (bus cycle selection during external memory access) of the clock control register (address: $00FE_H$).
t_{sys}[ns] = 2000/fc (Bits 5, 4 = "00"), 4000/fc (Bits 5, 4 = "01"), 8000/fc (Bits 5, 4 = "10"), 16000/fc (Bits 5, 4 = "11")

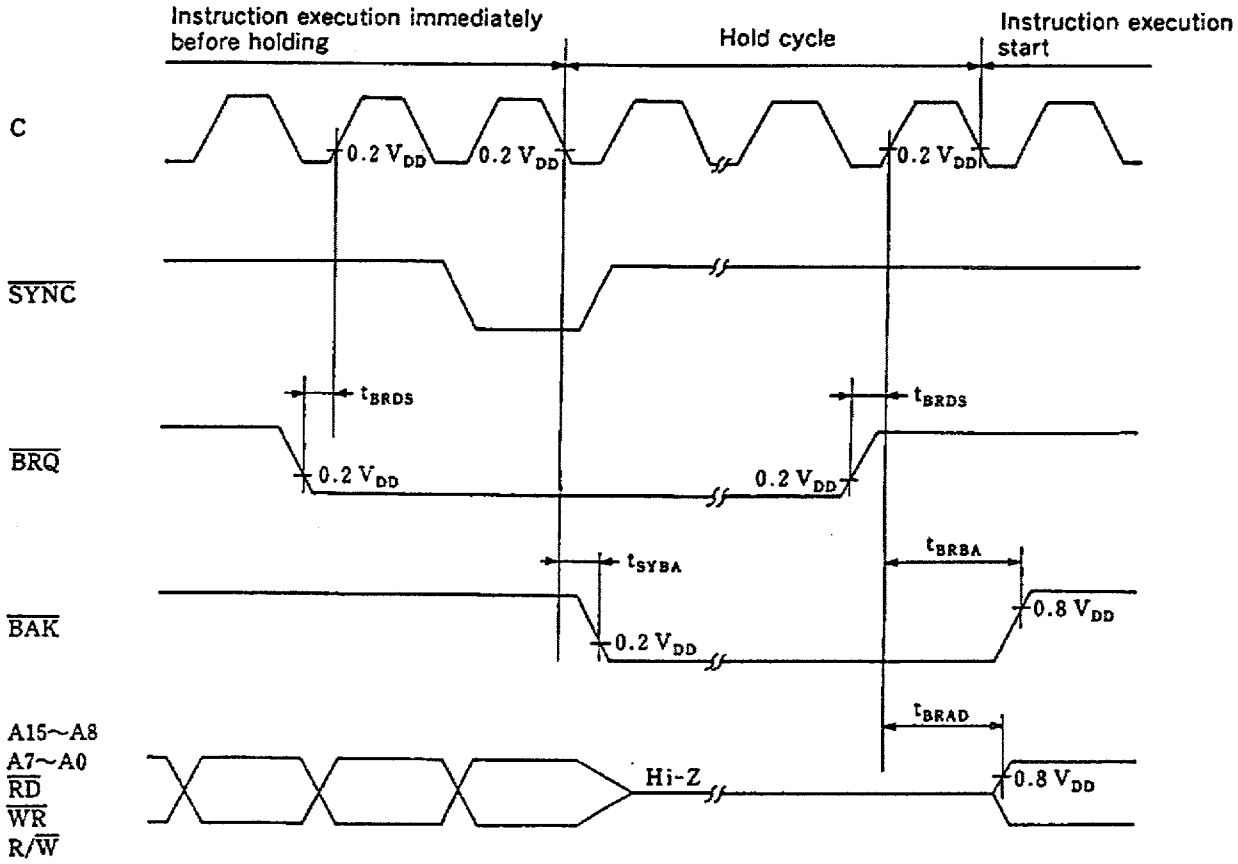
Fig. 9 Memory extension mode, microprocessor mode input/output timing



(6) Bus hold timing (Ta = −20 to +75°C, V_{DD} = 4.5 to 5.5V, V_{SS} = 0V, fC = 8MHz)

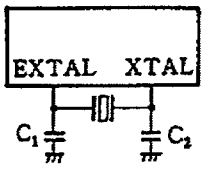
Item	Symbol	Pin	Conditions	Min.	Max.	Unit
Bus request ($\overline{BRQ}$) set-up time	t_{BRDS}	$\overline{BRQ}$	Fig. 8	100		ns
Bus acknowledge ($\overline{BAK}$) delay time	t_{SYBA}	$\overline{BAK}$			50	ns
Bus acknowledge ($\overline{BAK}$) releasing delay time	t_{BRBA}				220	ns
Bus line, control signal releasing delay time	t_{BRAD}	A15 to A8 A7 to A0 D7 to D0 $\overline{RD}$, $\overline{WR}$, R/$\overline{W}$			210	ns

Fig. 10 Bus hold timing



Appendix

Fig. 11 SPC700 series recommended oscillation circuit



Manufacturer	Model	Frequency range (MHz)	C_1, C_2 (pF)
MURATA MFG CO., LTD.	CSA6.00MG010	6.00	30
	CSA8.00MT	8.00	30

Manufacturer	Model	Frequency range (MHz)	C_1, C_2 (pF)
FUJI SANGYO CO., LTD.	HC-49/U-03	6.00	12
		8.00	12
KINSEKI LTD.	HC-49/U-S	6.00	22
		8.00	22
CITIZEN WATCH CO., LTD.	CSA-309	6.144	10
		8.000	10

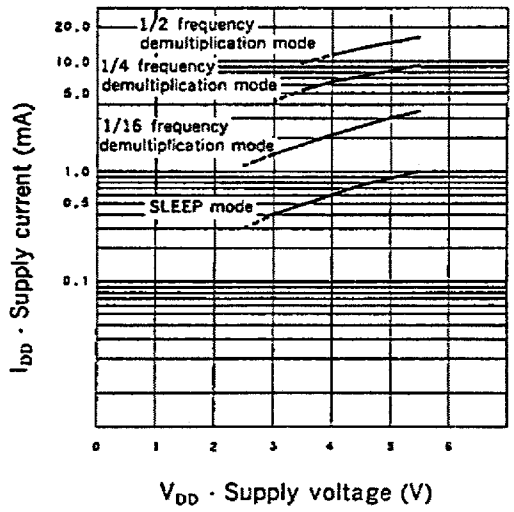
Mask option table

Item	Content	
Reset pin pull-up resistor	Non existent	Existent
Power-on reset circuit	Non existent	Existent

Fig. 12 Characteristic curves

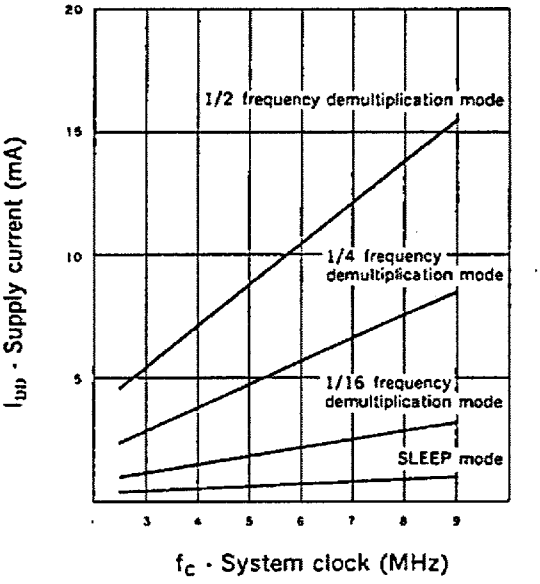
I_{DD} vs. V_{DD}

(f_C=8MHz, Ta=25°C, Typical)



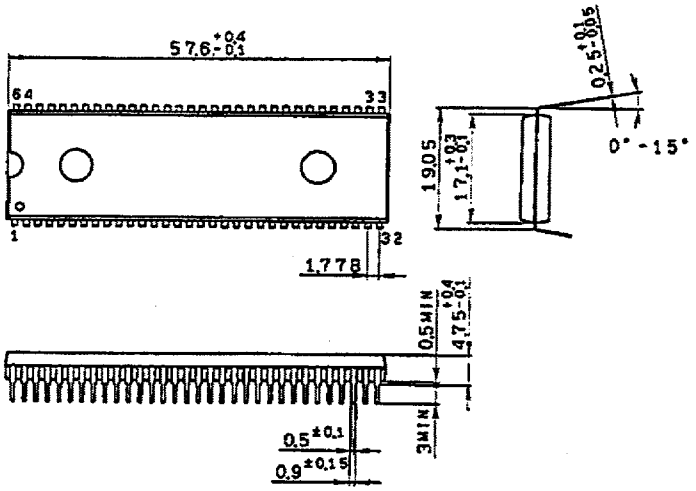
I_{DD} vs. f_C

V_{DD}=5V, Ta=25°C, typical)



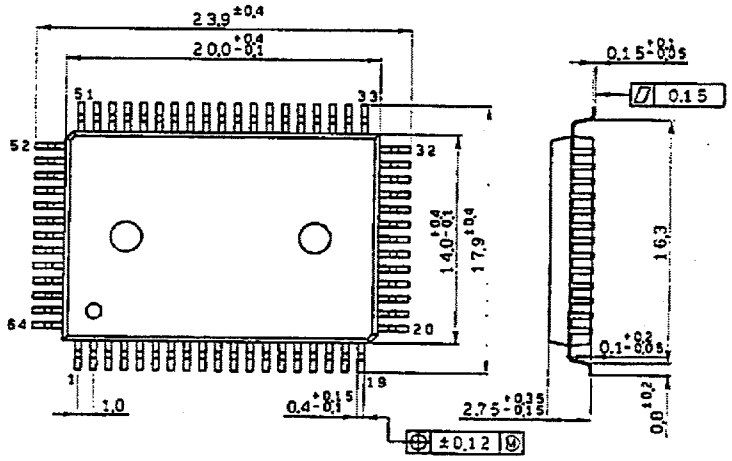
Package Outline Unit: mm

64pin SDIP (Plastic) 750mil 8.6g



SONY NAME	SDIP-64P-01
EIAJ NAME	SDIP064-P-0750-A
JEDEC CODE	———

64pin QFP (Plastic) 1.5g



SONY NAME	QFP-64P-L01
EIAJ NAME	*QFP064-P-1420-A
JEDEC CODE	———