ANALOG DEVICES

CMOS 16-Bit, 468.75 kHz, Sigma-Delta ADC

AD7721

FEATURES
16-Bit Sigma-Delta ADC
468.75 kHz Output Word Rate (OWR)
No Missing Codes
Low-Pass Digital Filter
High Speed Serial Interface
Linear Phase
229.2 kHz Input Bandwidth
Power Supplies: AV_{DD}, DV_{DD}: +5 V ± 5%
Standby Mode (70 μW)
Parallel Mode (12-Bit/312.5 kHz OWR)

## FUNCTIONAL BLOCK DIAGRAM

GENERAL DESCRIPTION

The AD7721 is a complete low power, 12-/16-bit, sigma-delta ADC. The part operates from a +5 V supply and accepts a differential input of 0 V to 2.5 V or ± 1.25 V. The analog input is continuously sampled by an analog modulator at twice the clock frequency eliminating the need for external sample-and-hold circuitry. The modulator output is processed by two finite impulse response (FIR) digital filters in series. The on-chip filtering reduces the external antialias requirements to first order in most cases. Settling time for a step input is 218.4 μs while the group delay for the filter is 109.2 μs when the master clock equals 15 MHz.

The AD7721 can be operated with input bandwidths up to 229.2 kHz. The corresponding output word rate is 468.75 kHz. The part can be operated with lower clock frequencies also. The sample rate, filter corner frequency, settling time, group delay and output word rate will be reduced also, as these are proportional to the external clock frequency. The maximum clock frequencies in parallel mode and serial mode are 10 MHz and 15 MHz respectively.

Use of a single bit DAC in the modulator guarantees excellent linearity and dc accuracy. Endpoint accuracy is ensured by on-chip calibration of offset and gain. This calibration procedure minimizes the part's zero-scale and full-scale errors.

The output data is accessed from the output register through a serial or parallel port. This offers easy, high speed interfacing to modern microcontrollers and digital signal processors. The serial interface operates in internal clocking (master) mode, the AD7721 providing the serial clock.

CMOS construction ensures low power dissipation while a power-down mode reduces the power consumption to only 100 μW.
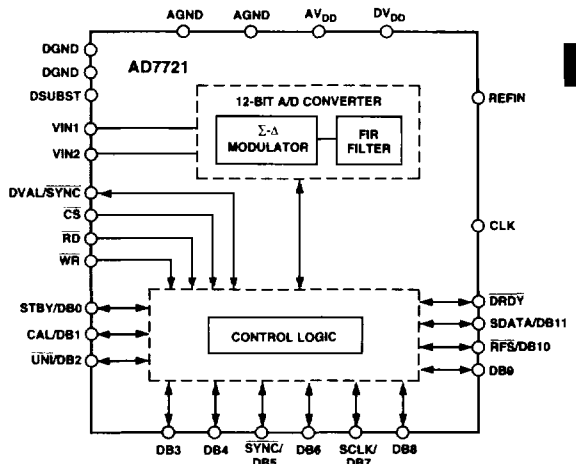
PIN CONFIGURATION
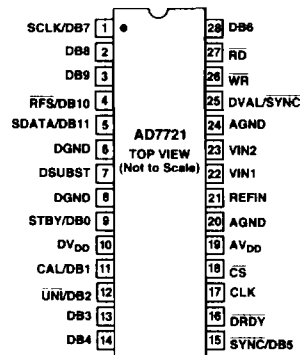
ORDERING GUIDE

Model	Temperature Range	Package Option*
AD7721AN	−40°C to +85°C	N-28
AD7721AR	−40°C to +85°C	R-28
AD7721SQ	−55°C to +125°C	Q-28

*N = Plastic DIP; R = 0.3" Small Outline IC (SOIC); Q = Cerdip. For outline information see Package Information section.

Parameter	A Version	S Version	Units	Test Conditions/Comments
SERIAL MODE ONLY				
STATIC PERFORMANCE				
Resolution	16	16	Bits	
Minimum Resolution for Which No Missing Codes Is Guaranteed	12	12	Bits min	Guaranteed 12 Bits Monotonic
Differential Nonlinearity	±8	±8	LSB typ	
Integral Nonlinearity	±16	±16	LSB max	16-Bit Operation
DC CMRR	70	70	dB min	Bipolar Mode
Offset Error[2]				
Unipolar Mode	±3.66	±3.66	mV max	Typically 0.61 mV
Bipolar Mode	±3.66	±3.66	mV max	Typically 0.61 mV
Full-Scale Error[2, 3]				
Unipolar Mode	±4.88	±4.88	mV max	Typically 0.61 mV
Bipolar Mode	±4.88	±4.88	mV max	Typically 1.22 mV
Unipolar Offset Drift	0.05	0.05	mV/°C typ	
Bipolar Offset Drift	0.04	0.04	mV/°C typ	
ANALOG INPUTS				
Signal Input Span (VIN1–VIN2)				
Bipolar Mode	±V_{REFIN}/2	±V_{REFIN}/2	Volts max	$\overline{UNI}$ = V_{IH}
Unipolar Mode	0 to V_{REFIN}	0 to V_{REFIN}	Volts max	$\overline{UNI}$ = V_{IL}
Maximum Input Voltage	AV_{DD}	AV_{DD}	Volts	
Minimum Input Voltage	0	0	Volts	
Input Sampling Capacitance	1.6	1.6	pF typ	
Input Sampling Rate	2 f_{CLK}	2 f_{CLK}	MHz	Guaranteed by Design
Differential Input Impedance	20.8	20.8	kΩ typ	With 15 MHz on CLK Pin
REFERENCE INPUTS				
V_{REFIN}	2.4 to 2.6	2.4 to 2.6	V min/V max	
REFIN Input Current	200	200	μA typ	
DYNAMIC SPECIFICATIONS				
Signal to (Noise + Distortion)	74	74	dB min	Input Bandwidth 0 kHz to 210 kHz
Total Harmonic Distortion	−78	−78	dB max	Input Bandwidth 0 kHz to 229.2 kHz
Frequency Response				
0 kHz–210 kHz	±0.05	±0.05	dB max	
229.2 kHz	−3	−3	dB min	
259.01 kHz to 14.74 MHz	−72	−72	dB min	
CLOCK				
CLK Duty Ratio	45 to 55	45 to 55	% max	For Specified Operation
V_{CLKH}, CLK High Voltage	0.7 × DV_{DD}	0.7 × DV_{DD}	V min	CLK Uses CMOS Logic
V_{CLKL}, CLK Low Voltage	0.3 × DV_{DD}	0.3 × DV_{DD}	V max	
LOGIC INPUTS				
V_{INH}, Input High Voltage	2.0	2.0	V min	
V_{INL}, Input Low Voltage	0.8	0.8	V max	
I_{INH}, Input Current	10	10	μA max	
C_{IN}, Input Capacitance	10	10	pF max	
LOGIC OUTPUTS				
V_{OH}, Output High Voltage	4.0	4.0	V min	$|I_{OUT}|$ ≤ 200 μA
V_{OL}, Output Low Voltage	0.4	0.4	V max	$|I_{OUT}|$ ≤ 1.6 mA
POWER SUPPLIES				
AV_{DD}	4.75/5.25	4.75/5.25	V min/V max	
DV_{DD}	4.75/5.25	4.75/5.25	V min/V max	
I_{DD} (Total from AV_{DD}, DV_{DD})	28.5	28.5	mA max	Digital Inputs Equal to 0 V or DV_{DD}
Power Consumption	150	150	mW max	Active Mode
Power Consumption	100	100	μW max	Standby Mode

NOTES
[1]Operating temperature range is as follows: A Version: 40°C to +85°C; S Version: 55°C to +125°C.
[2]Applies after calibration at temperature of interest.
[3]Full-scale error applies to both positive and negative full-scale error. The ADC gain is calibrated w.r.t. the voltage on the REFIN pin.

Specifications subject to change without notice.