

**NEC****MOS INTEGRATED CIRCUIT** **$\mu$ PD42S4260AL, 424260AL**

**3.3 V OPERATION 4 M-BIT DYNAMIC RAM**  
**256 K-WORD BY 16-BIT, FAST PAGE MODE, BYTE READ/WRITE MODE**

**Description**

The  $\mu$ PD42S4260AL, 424260AL are 262,144 words by 16 bits CMOS dynamic RAMs. The fast page mode and byte read/write mode capability realize high speed access and low power consumption.

Besides, the  $\mu$ PD42S4260AL can execute  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  self refresh.

These are packaged in 44-pin plastic TSOP (II) and 40-pin plastic SOJ.

**Features**

- 262,144 words by 16 bits organization
- Single +3.3 V  $\pm$ 0.3 V power supply
- Fast access and cycle time

Part number	Power consumption Active (MAX.)	Access time (MAX.)	R/W cycle time (MIN.)	Fast page mode cycle time (MIN.)
$\mu$ PD42S4260AL-A60, 424260AL-A60	288 mW	60 ns	110 ns	40 ns
$\mu$ PD42S4260AL-A70, 424260AL-A70	252 mW	70 ns	130 ns	45 ns

- The  $\mu$ PD42S4260AL can execute  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  self refresh

Part number	Refresh cycle	Refresh	Power consumption at standby (MAX.)
$\mu$ PD42S4260AL	512 cycles / 128 ms	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh	0.288 mW (CMOS level input)
$\mu$ PD424260AL	512 cycles / 8 ms	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh	1.8 mW (CMOS level input)

The information in this document is subject to change without notice.

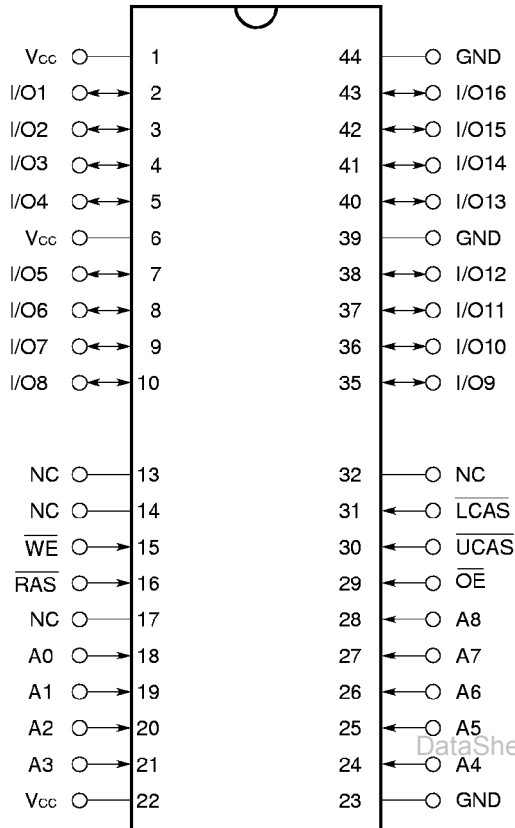
## Ordering Information

Part number	Access time (MAX.)	Package	Refresh
$\mu$ PD42S4260ALG5-A60-7JF	60 ns	44-pin Plastic TSOP (II) (400 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh
$\mu$ PD42S4260ALG5-A70-7JF	70 ns		
$\mu$ PD42S4260ALLE-A60	60 ns	40-pin Plastic SOJ (400 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh
$\mu$ PD42S4260ALLE-A70	70 ns		
$\mu$ PD424260ALG5-A60-7JF	60 ns	44-pin Plastic TSOP (II) (400 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh
$\mu$ PD424260ALG5-A70-7JF	70 ns		
$\mu$ PD424260ALLE-A60	60 ns	40-pin Plastic SOJ (400 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh
$\mu$ PD424260ALLE-A70	70 ns		

**Pin Configurations (Marking Side)**

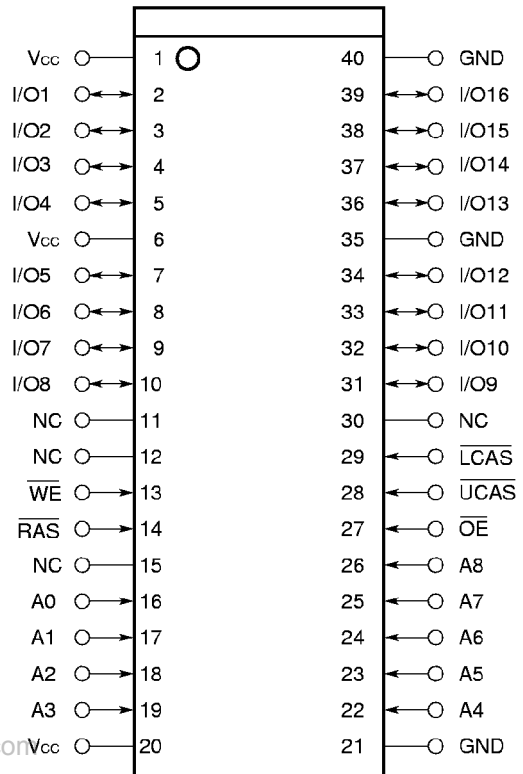
**44-pin Plastic TSOP (II) (400 mil)**

μPD42S4260ALG5-7JF  
 μPD424260ALG5-7JF



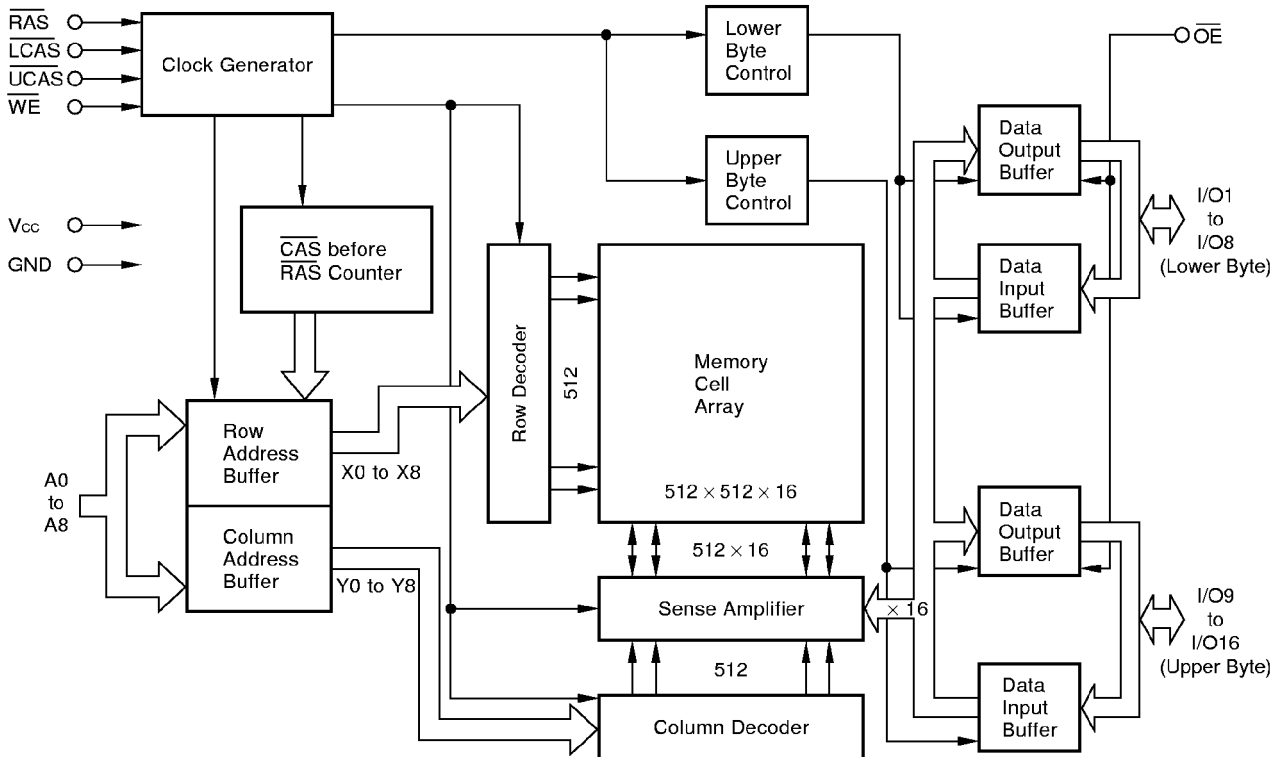
**40-pin Plastic SOJ (400 mil)**

μPD42S4260ALLE  
 μPD424260ALLE



- A0 to A8 : Address Inputs
- I/O1 to I/O16 : Data Inputs/Outputs
- $\overline{\text{RAS}}$  : Row Address Strobe
- $\overline{\text{UCAS}}$  : Column Address Strobe (upper)
- $\overline{\text{LCAS}}$  : Column Address Strobe (lower)
- $\overline{\text{WE}}$  : Write Enable
- $\overline{\text{OE}}$  : Output Enable
- Vcc : Power Supply
- GND : Ground
- NC : No Connection

**Block Diagram**



**Input/Output Pin Functions**

The  $\mu$ PD42S4260AL, 424260AL have input pins  $\overline{\text{RAS}}$ ,  $\overline{\text{CAS}}$ <sup>Note</sup>,  $\overline{\text{WE}}$ ,  $\overline{\text{OE}}$ , A0 to A8 and input/output pins I/O1 to I/O16.

Pin name	Input/ Output	Function
$\overline{\text{RAS}}$ (Row address strobe)	Input	$\overline{\text{RAS}}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh
$\overline{\text{CAS}}$ (Column address strobe)	Input	$\overline{\text{CAS}}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to A8 (Address inputs)	Input	Address bus. Input total 18-bit of address signal, upper 9-bit and lower 9-bit in sequence (address multiplex method). Therefore, one word is selected from 262,144-word by 16-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{\text{RAS}}$ . Then, switch the address bus to column address and activate $\overline{\text{CAS}}$ . Each address is taken into the device when $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are activated. Therefore, the address input setup time ( $t_{ASR}$ , $t_{ASC}$ ) and hold time ( $t_{RAH}$ , $t_{CAH}$ ) are specified for the activation of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ .
$\overline{\text{WE}}$ (Write enable)	Input	Write control signal. Write operation is executed by activating $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ .
$\overline{\text{OE}}$ (Output enable)	Input	Read control signal. Read operation can be executed by activating $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ and $\overline{\text{OE}}$ . If $\overline{\text{WE}}$ is activated during read operation, $\overline{\text{OE}}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O16 (Data inputs/ outputs)	Input/ Output	16-bit data bus. I/O1 to I/O16 are used to input/output data.

**Note**  $\overline{\text{CAS}}$  means  $\overline{\text{UCAS}}$  and  $\overline{\text{LCAS}}$ .

## Electrical Specifications

- $\overline{\text{CAS}}$  means  $\overline{\text{UCAS}}$  and  $\overline{\text{LCAS}}$ .
- All voltages are referenced to GND.
- After power up ( $V_{\text{CC}} \geq V_{\text{CC (MIN.)}}$ ), wait more than 100  $\mu\text{s}$  ( $\overline{\text{RAS}}$ ,  $\overline{\text{CAS}}$  inactive) and then, execute eight  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  or  $\overline{\text{RAS}}$  only refresh cycles as dummy cycles to initialize internal circuit.

## Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	$V_T$		-0.5 to +4.6	V
Supply voltage	$V_{\text{CC}}$		-0.5 to +4.6	V
Output current	$I_O$		20	mA
Power dissipation	$P_D$		1	W
Operating ambient temperature	$T_A$		0 to +70	$^{\circ}\text{C}$
Storage temperature	$T_{\text{stg}}$		-55 to +125	$^{\circ}\text{C}$

**Caution** Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

## Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	$V_{\text{CC}}$		3.0	3.3	3.6	V
High level input voltage	$V_{\text{IH}}$		2.0		$V_{\text{CC}} + 0.3$	V
Low level input voltage	$V_{\text{IL}}$		-0.3		+0.8	V
Operating ambient temperature	$T_A$		0		70	$^{\circ}\text{C}$

## Capacitance ( $T_A = 25^{\circ}\text{C}$ , $f = 1\text{ MHz}$ )

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	$C_{\text{I1}}$	Address			5	pF
	$C_{\text{I2}}$	$\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WE}}$ , $\overline{\text{OE}}$			7	pF
Data input/output capacitance	$C_{\text{I/O}}$	I/O			7	pF

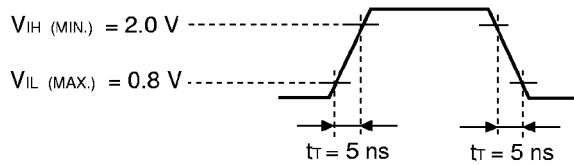
## DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter		Symbol	Test condition	MIN.	MAX.	Unit	Notes
Operating current		I <sub>CC1</sub>	$\overline{\text{RAS}}, \overline{\text{CAS}}$ cycling $t_{\text{RC}} = t_{\text{RC}(\text{MIN.})}, I_{\text{O}} = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$	80	mA	1, 2, 3
				$t_{\text{RAC}} = 70 \text{ ns}$	70		
Standby current	$\mu$ PD42S4260AL	I <sub>CC2</sub>	$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{IH}(\text{MIN.})}, I_{\text{O}} = 0 \text{ mA}$		0.5	mA	
			$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}} - 0.2 \text{ V}, I_{\text{O}} = 0 \text{ mA}$		0.08		
	$\mu$ PD424260AL	$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{IH}(\text{MIN.})}, I_{\text{O}} = 0 \text{ mA}$		2			
		$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}} - 0.2 \text{ V}, I_{\text{O}} = 0 \text{ mA}$		0.5			
$\overline{\text{RAS}}$ only refresh current		I <sub>CC3</sub>	$\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}} \geq V_{\text{IH}(\text{MIN.})}$ $t_{\text{RC}} = t_{\text{RC}(\text{MIN.})}, I_{\text{O}} = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$	80	mA	1, 2, 3, 4
				$t_{\text{RAC}} = 70 \text{ ns}$	70		
Operating current (Fast page mode)		I <sub>CC4</sub>	$\overline{\text{RAS}} \leq V_{\text{IL}(\text{MAX.})}, \overline{\text{CAS}}$ cycling $t_{\text{PC}} = t_{\text{PC}(\text{MIN.})}, I_{\text{O}} = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$	70	mA	1, 2, 5
				$t_{\text{RAC}} = 70 \text{ ns}$	60		
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh current		I <sub>CC5</sub>	$\overline{\text{RAS}}$ cycling $t_{\text{RC}} = t_{\text{RC}(\text{MIN.})}, I_{\text{O}} = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$	80	mA	1, 2
				$t_{\text{RAC}} = 70 \text{ ns}$	70		
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ long refresh current (512 cycles / 128 ms, only for the $\mu$ PD42S4260AL)		I <sub>CC6</sub>	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh: $t_{\text{RC}} = 250.0 \mu\text{s}$ $\overline{\text{RAS}}, \overline{\text{CAS}}:$ $V_{\text{CC}} - 0.2 \text{ V} \leq V_{\text{IH}} \leq V_{\text{IH}(\text{MAX.})}$ $0 \text{ V} \leq V_{\text{IL}} \leq 0.2 \text{ V}$	$t_{\text{RAS}} \leq 200 \text{ ns}$	80	$\mu\text{A}$	1, 2
			Standby: $\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}} - 0.2 \text{ V}$ Address: $V_{\text{IH}}$ or $V_{\text{IL}}$ $\overline{\text{WE}}, \overline{\text{OE}}: V_{\text{IH}}$ $I_{\text{O}} = 0 \text{ mA}$	$t_{\text{RAS}} \leq 1 \mu\text{s}$		100	$\mu\text{A}$
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh current (only for the $\mu$ PD42S4260AL)		I <sub>CC7</sub>	$\overline{\text{RAS}}, \overline{\text{CAS}}:$ $t_{\text{RAS}} = 5 \text{ ms}$ $V_{\text{CC}} - 0.2 \text{ V} \leq V_{\text{IH}} \leq V_{\text{IH}(\text{MAX.})}$ $0 \text{ V} \leq V_{\text{IL}} \leq 0.2 \text{ V}$ $I_{\text{O}} = 0 \text{ mA}$		80	$\mu\text{A}$	2
Input leakage current		I <sub>I(L)</sub>	$V_{\text{I}} = 0 \text{ to } 3.6 \text{ V}$ All other pins not under test = 0 V	-5	+5	$\mu\text{A}$	
Output leakage current		I <sub>O(L)</sub>	$V_{\text{O}} = 0 \text{ to } 3.6 \text{ V}$ Output is disabled (Hi-Z)	-5	+5	$\mu\text{A}$	
High level output voltage		V <sub>OH</sub>	$I_{\text{O}} = -2.0 \text{ mA}$	2.4		V	
Low level output voltage		V <sub>OL</sub>	$I_{\text{O}} = +2.0 \text{ mA}$		0.4	V	

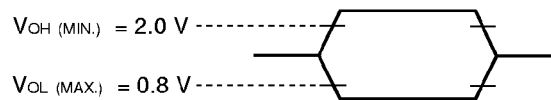
- Notes**
1. I<sub>CC1</sub>, I<sub>CC3</sub>, I<sub>CC4</sub>, I<sub>CC5</sub> and I<sub>CC6</sub> depend on cycle rates ( $t_{\text{RC}}$  and  $t_{\text{PC}}$ ).
  2. Specified values are obtained with outputs unloaded.
  3. I<sub>CC1</sub> and I<sub>CC3</sub> are measured assuming that address can be changed once or less during  $\overline{\text{RAS}} \leq V_{\text{IL}(\text{MAX.})}$  and  $\overline{\text{CAS}} \geq V_{\text{IH}(\text{MIN.})}$ .
  4. I<sub>CC3</sub> is measured assuming that all column address inputs are held at either high or low.
  5. I<sub>CC4</sub> is measured assuming that all column address inputs are switched only once during each fast page cycle.

**AC Characteristics (Recommended Operating Conditions unless otherwise noted)****AC Characteristics Test Conditions**

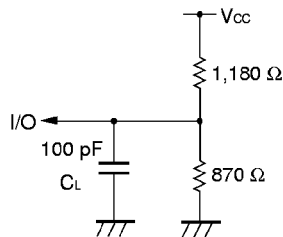
(1) Input timing specification



(2) Output timing specification



(3) Output load condition

**Common to Read, Write, Read Modify Write Cycle**

Parameter	Symbol	$t_{RAC} = 60 \text{ ns}$		$t_{RAC} = 70 \text{ ns}$		Unit	Notes	
		MIN.	MAX.	MIN.	MAX.			
Read/Write cycle time	$t_{RC}$	110	–	130	–	ns		
$\overline{\text{RAS}}$ precharge time	$t_{RP}$	40	–	50	–	ns		
$\overline{\text{CAS}}$ precharge time	$t_{CPN}$	10	–	10	–	ns		
$\overline{\text{RAS}}$ pulse width	$t_{RAS}$	60	10,000	70	10,000	ns	1	
$\overline{\text{CAS}}$ pulse width	$t_{CAS}$	15	10,000	20	10,000	ns		
$\overline{\text{RAS}}$ hold time	$t_{RSH}$	15	–	18	–	ns		
$\overline{\text{CAS}}$ hold time	$t_{CSH}$	60	–	70	–	ns		
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	$t_{RCD}$	20	45	20	50	ns	2	
$\overline{\text{RAS}}$ to column address delay time	$t_{RAD}$	15	30	15	35	ns	2	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	$t_{CRP}$	5	–	5	–	ns	3	
Row address setup time	$t_{ASR}$	0	–	0	–	ns		
Row address hold time	$t_{RAH}$	10	–	10	–	ns		
Column address setup time	$t_{ASC}$	0	–	0	–	ns		
Column address hold time	$t_{CAH}$	15	–	15	–	ns		
$\overline{\text{OE}}$ lead time referenced to $\overline{\text{RAS}}$	$t_{OES}$	0	–	0	–	ns		
$\overline{\text{CAS}}$ to data setup time	$t_{CLZ}$	0	–	0	–	ns		
$\overline{\text{OE}}$ to data setup time	$t_{OLZ}$	0	–	0	–	ns		
$\overline{\text{OE}}$ to data delay time	$t_{OED}$	13	–	15	–	ns		
Masked byte write hold time referenced to $\overline{\text{RAS}}$	$t_{MRH}$	0	–	0	–	ns		
Transition time (rise and fall)	$t_r$	3	50	3	50	ns		
Refresh time	$\mu$ PD42S4260AL	$t_{REF}$	–	128	–	128	ms	4
	$\mu$ PD424260AL		–	8	–	8	ms	



- Notes 1.** In  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh cycles,  $t_{\text{RAS}}(\text{MAX.})$  is 100  $\mu\text{s}$ .  
If  $10 \mu\text{s} < t_{\text{RAS}} < 100 \mu\text{s}$ ,  $\overline{\text{RAS}}$  precharge time for  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  self refresh ( $t_{\text{RPS}}$ ) is applied.
- 2.** For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{\text{RAS}}$
$t_{\text{RAD}} \leq t_{\text{RAD}}(\text{MAX.})$ and $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{MAX.})$	$t_{\text{RAC}}(\text{MAX.})$	$t_{\text{RAC}}(\text{MAX.})$
$t_{\text{RAD}} > t_{\text{RAD}}(\text{MAX.})$ and $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{MAX.})$	$t_{\text{AA}}(\text{MAX.})$	$t_{\text{RAD}} + t_{\text{AA}}(\text{MAX.})$
$t_{\text{RCD}} > t_{\text{RCD}}(\text{MAX.})$	$t_{\text{CAC}}(\text{MAX.})$	$t_{\text{RCD}} + t_{\text{CAC}}(\text{MAX.})$

$t_{\text{RAD}}(\text{MAX.})$  and  $t_{\text{RCD}}(\text{MAX.})$  are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time ( $t_{\text{RAC}}$ ,  $t_{\text{AA}}$  or  $t_{\text{CAC}}$ ) is to be used for finding out when output data will be available. Therefore, the input conditions  $t_{\text{RAD}} \geq t_{\text{RAD}}(\text{MAX.})$  and  $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{MAX.})$  will not cause any operation problems.

- 3.**  $t_{\text{CRP}}(\text{MIN.})$  requirement is applied to  $\overline{\text{RAS}}$ ,  $\overline{\text{CAS}}$  cycles.
- 4.** This specification is applied only to the  $\mu$ PD42S4260AL.

### Read Cycle

Parameter	Symbol	$t_{\text{RAC}} = 60 \text{ ns}$		$t_{\text{RAC}} = 70 \text{ ns}$		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Access time from $\overline{\text{RAS}}$	$t_{\text{RAC}}$	–	60	–	70	ns	1
Access time from $\overline{\text{CAS}}$	$t_{\text{CAC}}$	–	15	–	20	ns	1
Access time from column address	$t_{\text{AA}}$	–	30	–	35	ns	1
Access time from $\overline{\text{OE}}$	$t_{\text{OEA}}$	–	15	–	20	ns	
Column address lead time referenced to $\overline{\text{RAS}}$	$t_{\text{RAL}}$	30	–	35	–	ns	
Read command setup time	$t_{\text{RCS}}$	0	–	0	–	ns	
Read command hold time referenced to $\overline{\text{RAS}}$	$t_{\text{RRH}}$	0	–	0	–	ns	2
Read command hold time referenced to $\overline{\text{CAS}}$	$t_{\text{RCH}}$	0	–	0	–	ns	2
Output buffer turn-off delay time from $\overline{\text{OE}}$	$t_{\text{OEZ}}$	0	13	0	15	ns	3
Output buffer turn-off delay time from $\overline{\text{CAS}}$	$t_{\text{OFF}}$	0	13	0	15	ns	3

- Notes 1.** For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{\text{RAS}}$
$t_{\text{RAD}} \leq t_{\text{RAD}}(\text{MAX.})$ and $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{MAX.})$	$t_{\text{RAC}}(\text{MAX.})$	$t_{\text{RAC}}(\text{MAX.})$
$t_{\text{RAD}} > t_{\text{RAD}}(\text{MAX.})$ and $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{MAX.})$	$t_{\text{AA}}(\text{MAX.})$	$t_{\text{RAD}} + t_{\text{AA}}(\text{MAX.})$
$t_{\text{RCD}} > t_{\text{RCD}}(\text{MAX.})$	$t_{\text{CAC}}(\text{MAX.})$	$t_{\text{RCD}} + t_{\text{CAC}}(\text{MAX.})$

$t_{\text{RAD}}(\text{MAX.})$  and  $t_{\text{RCD}}(\text{MAX.})$  are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time ( $t_{\text{RAC}}$ ,  $t_{\text{AA}}$  or  $t_{\text{CAC}}$ ) is to be used for finding out when output data will be available. Therefore, the input conditions  $t_{\text{RAD}} \geq t_{\text{RAD}}(\text{MAX.})$  and  $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{MAX.})$  will not cause any operation problems.

- 2.** Either  $t_{\text{RCH}}(\text{MIN.})$  or  $t_{\text{RRH}}(\text{MIN.})$  should be met in read cycles.
- 3.**  $t_{\text{OFF}}(\text{MAX.})$  and  $t_{\text{OEZ}}(\text{MAX.})$  define the time when the output achieves the condition of Hi-Z and is not referenced to  $V_{\text{OH}}$  or  $V_{\text{OL}}$ .

**Write Cycle**

Parameter	Symbol	$t_{RAC} = 60 \text{ ns}$		$t_{RAC} = 70 \text{ ns}$		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
$\overline{WE}$ hold time referenced to $\overline{CAS}$	$t_{WCH}$	10	–	10	–	ns	1
$\overline{WE}$ pulse width	$t_{WP}$	10	–	10	–	ns	1
$\overline{WE}$ lead time referenced to $\overline{RAS}$	$t_{RWL}$	20	–	20	–	ns	
$\overline{WE}$ lead time referenced to $\overline{CAS}$	$t_{CWL}$	15	–	15	–	ns	
$\overline{WE}$ setup time	$t_{WCS}$	0	–	0	–	ns	2
$\overline{OE}$ hold time	$t_{OEH}$	0	–	0	–	ns	
Data-in setup time	$t_{DS}$	0	–	0	–	ns	3
Data-in hold time	$t_{DH}$	10	–	15	–	ns	3

- Notes**
- $t_{WP (MIN.)}$  is applied to late write cycles or read modify write cycles. In early write cycles,  $t_{WCH (MIN.)}$  should be met.
  - If  $t_{WCS} \geq t_{WCS (MIN.)}$ , the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.
  - $t_{DS (MIN.)}$  and  $t_{DH (MIN.)}$  are referenced to the  $\overline{CAS}$  falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the  $\overline{WE}$  falling edge.

**Read Modify Write Cycle**

Parameter	Symbol	$t_{RAC} = 60 \text{ ns}$		$t_{RAC} = 70 \text{ ns}$		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
Read modify write cycle time	$t_{RWC}$	160	–	175	–	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	$t_{RWD}$	83	–	90	–	ns	1
$\overline{CAS}$ to $\overline{WE}$ delay time	$t_{CWD}$	38	–	40	–	ns	1
Column address to $\overline{WE}$ delay time	$t_{AWD}$	53	–	55	–	ns	1

- Note 1.** If  $t_{WCS} \geq t_{WCS (MIN.)}$ , the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If  $t_{RWD} \geq t_{RWD (MIN.)}$ ,  $t_{CWD} \geq t_{CWD (MIN.)}$ ,  $t_{AWD} \geq t_{AWD (MIN.)}$  and  $t_{CPWD} \geq t_{CPWD (MIN.)}$ , the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

**Fast Page Mode**

Parameter	Symbol	$t_{RAC} = 60 \text{ ns}$		$t_{RAC} = 70 \text{ ns}$		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
Fast page mode cycle time	$t_{PC}$	40	–	45	–	ns	
Access time from $\overline{\text{CAS}}$ precharge	$t_{ACP}$	–	35	–	40	ns	
$\overline{\text{RAS}}$ pulse width	$t_{RASP}$	60	125,000	70	125,000	ns	
$\overline{\text{CAS}}$ precharge time	$t_{CP}$	10	–	10	–	ns	
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	$t_{RHCP}$	35	–	40	–	ns	
Read modify write cycle time	$t_{PRWC}$	85	–	90	–	ns	
$\overline{\text{CAS}}$ precharge to $\overline{\text{WE}}$ delay time	$t_{CPWD}$	60	–	60	–	ns	1

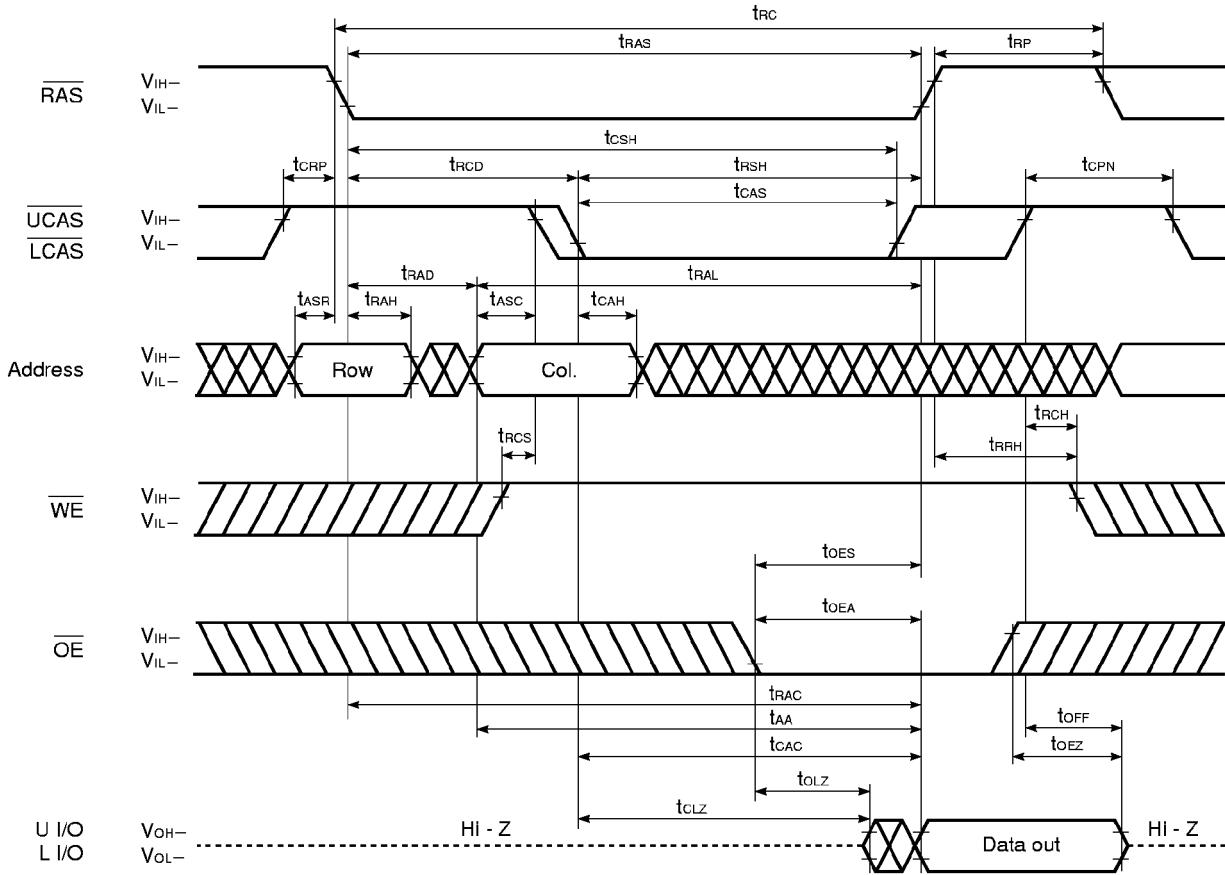
**Note 1.** If  $t_{WCS} \geq t_{WCS}(\text{MIN.})$ , the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If  $t_{RW} \geq t_{RW}(\text{MIN.})$ ,  $t_{CWD} \geq t_{CWD}(\text{MIN.})$ ,  $t_{AW} \geq t_{AW}(\text{MIN.})$  and  $t_{CPWD} \geq t_{CPWD}(\text{MIN.})$ , the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

**Refresh Cycle**

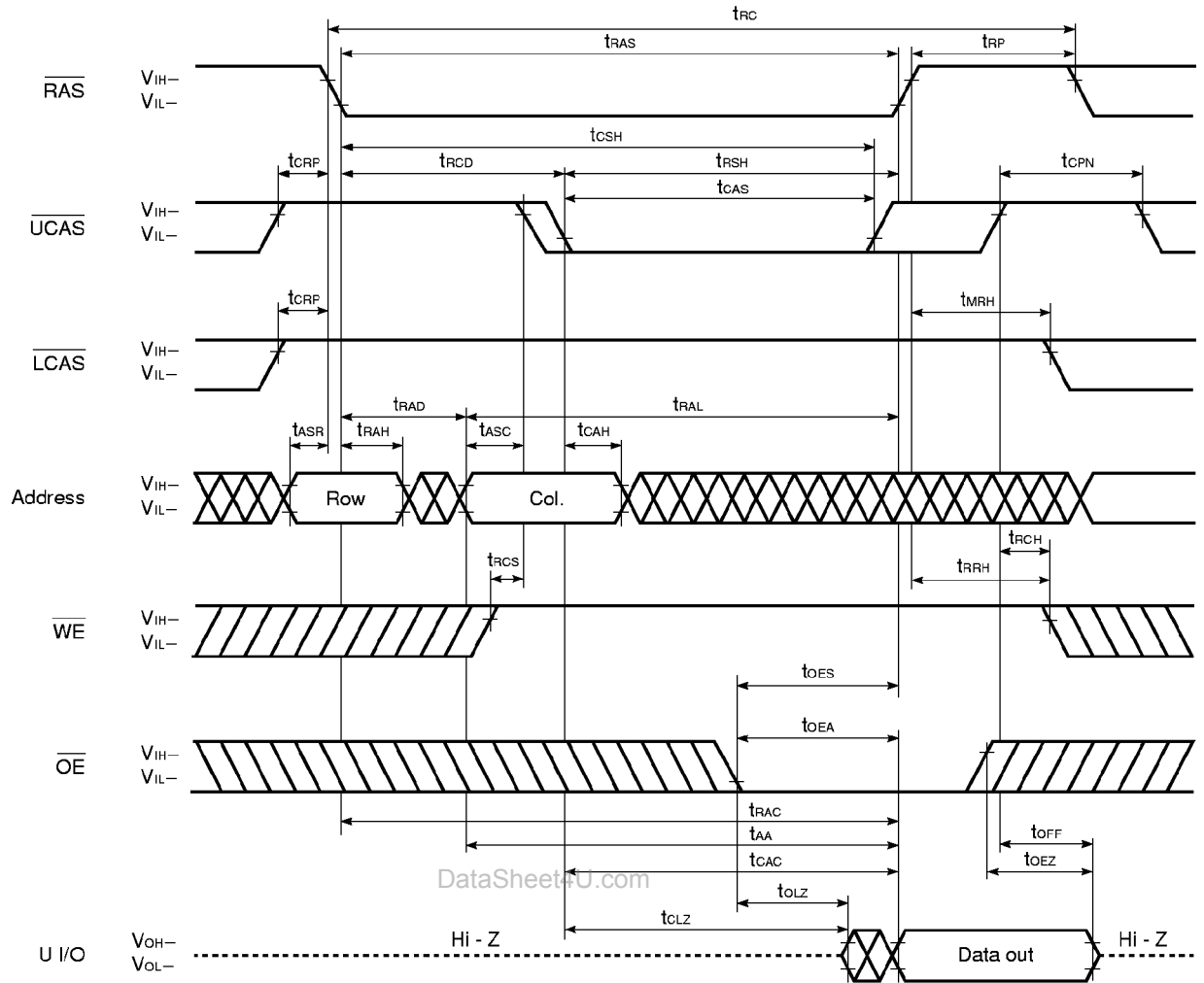
Parameter	Symbol	$t_{RAC} = 60 \text{ ns}$		$t_{RAC} = 70 \text{ ns}$		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
$\overline{\text{CAS}}$ setup time	$t_{CSR}$	5	–	5	–	ns	
$\overline{\text{CAS}}$ hold time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh)	$t_{CHR}$	10	–	10	–	ns	
$\overline{\text{RAS}}$ precharge $\overline{\text{CAS}}$ hold time	$t_{RPC}$	5	–	5	–	ns	
$\overline{\text{RAS}}$ pulse width ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh cycle)	$t_{RASS}$	100	–	100	–	$\mu\text{s}$	1
$\overline{\text{RAS}}$ precharge time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh cycle)	$t_{RPS}$	110	–	130	–	ns	1
$\overline{\text{CAS}}$ hold time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh cycle)	$t_{CHS}$	–50	–	–50	–	ns	1
$\overline{\text{WE}}$ hold time (hidden refresh cycle)	$t_{WHR}$	15	–	15	–	ns	

**Note 1.** This specification is applied only to the  $\mu$ PD42S4260AL.

**Read Cycle**

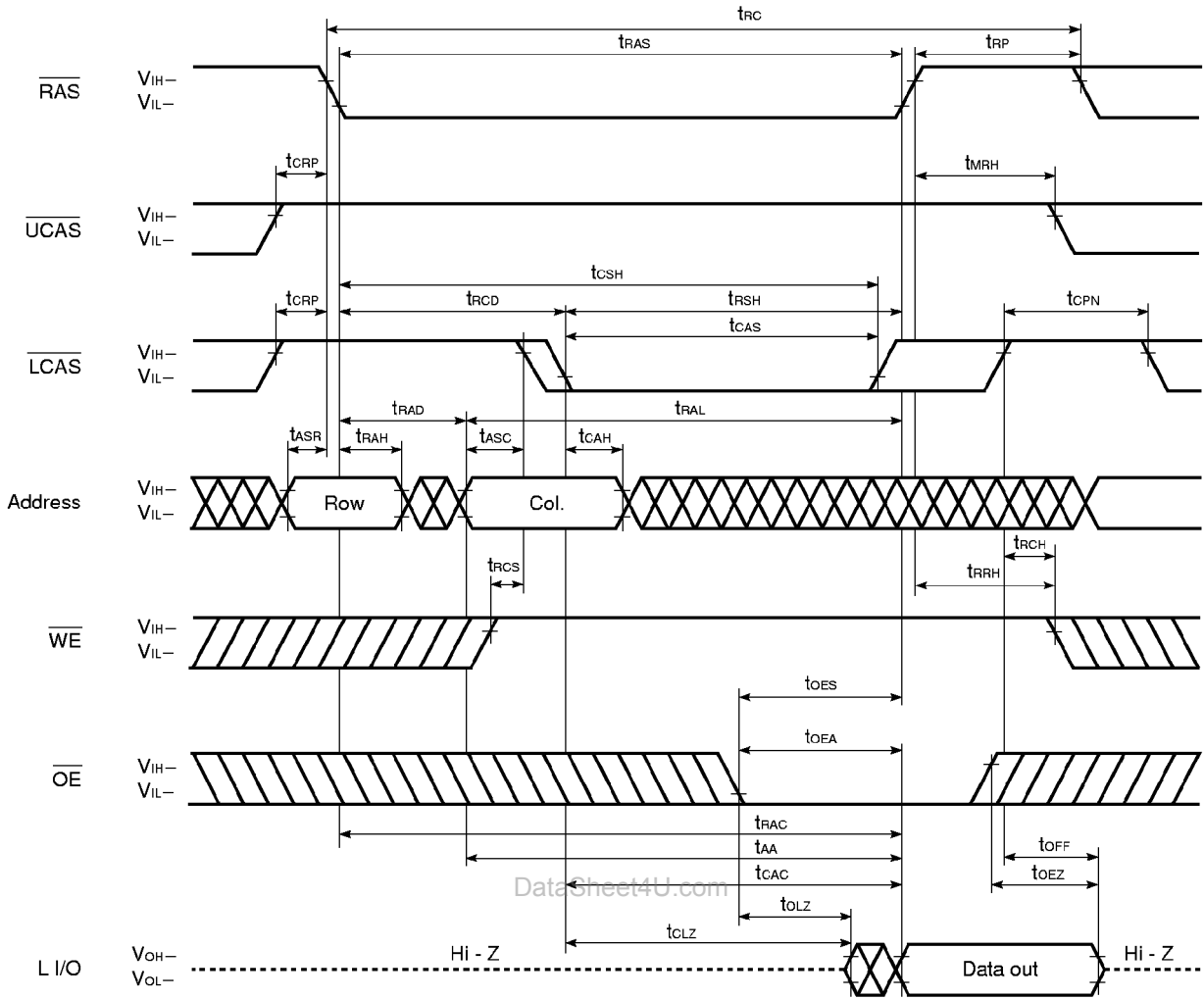


**Upper Byte Read Cycle**



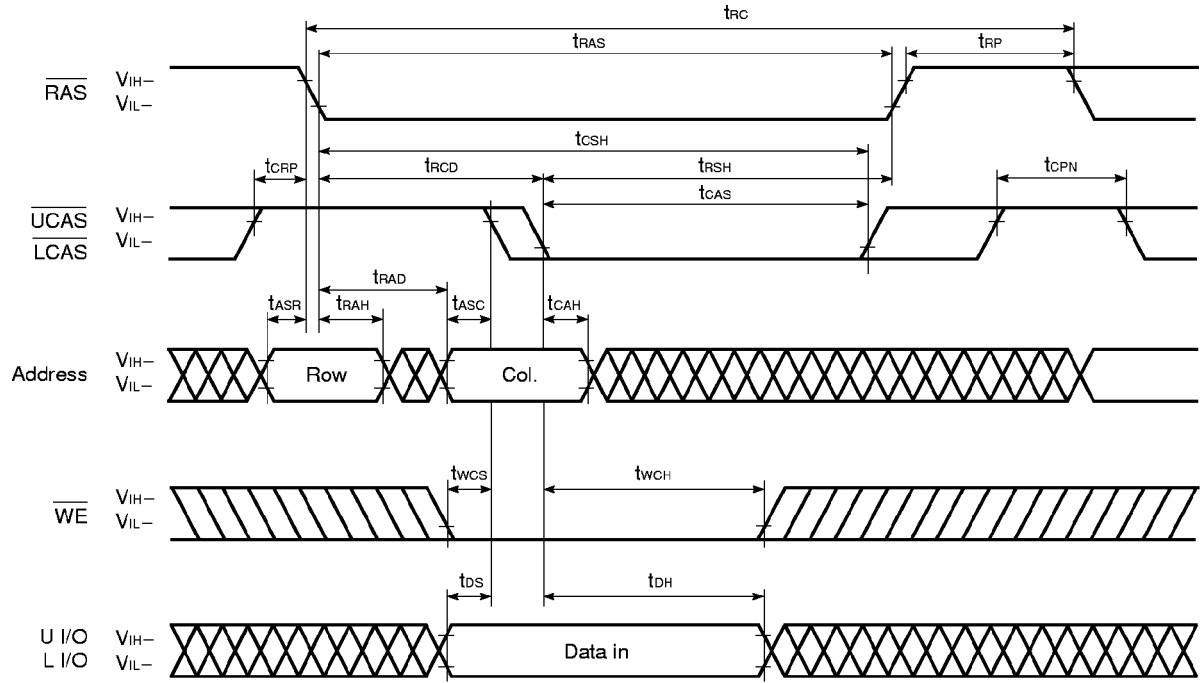
**Remark** L I/O: Hi-Z

**Lower Byte Read Cycle**



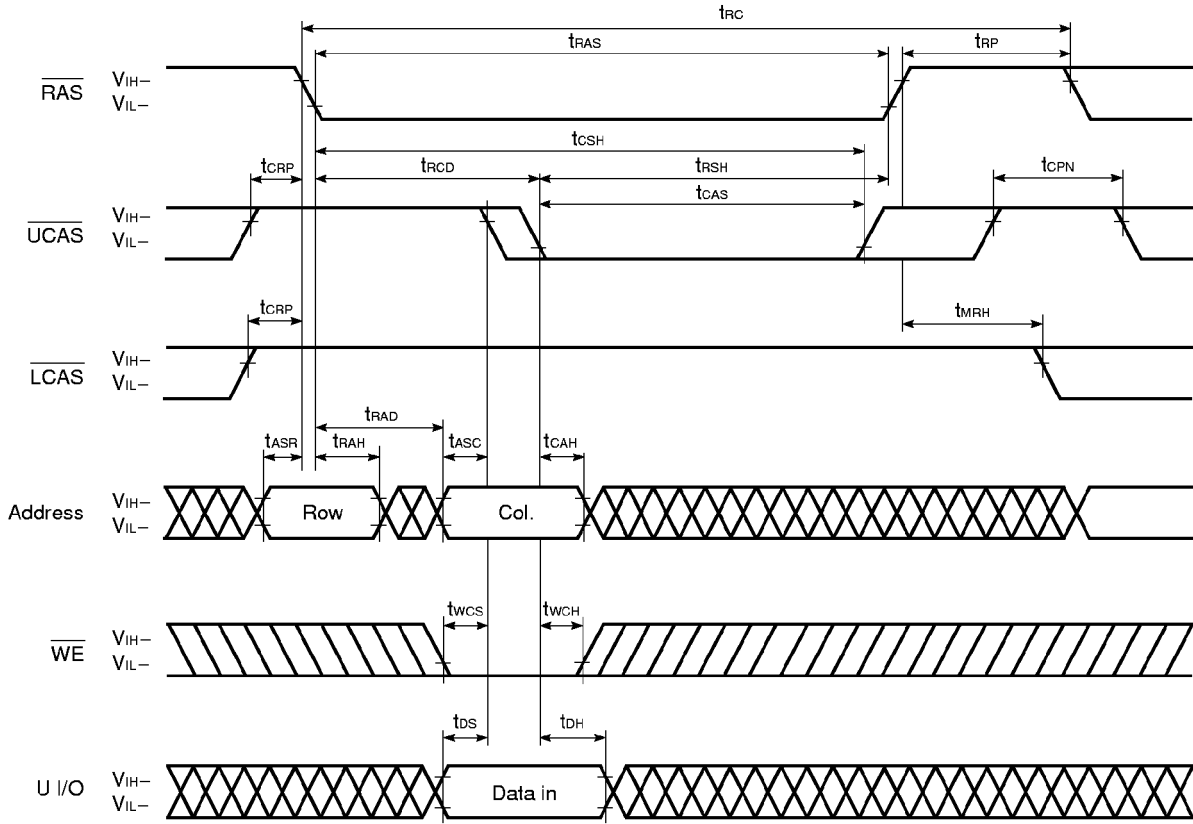
**Remark** U I/O: Hi-Z

**Early Write Cycle**



**Remark**  $\overline{OE}$ : Don't care

**Upper Byte Early Write Cycle**



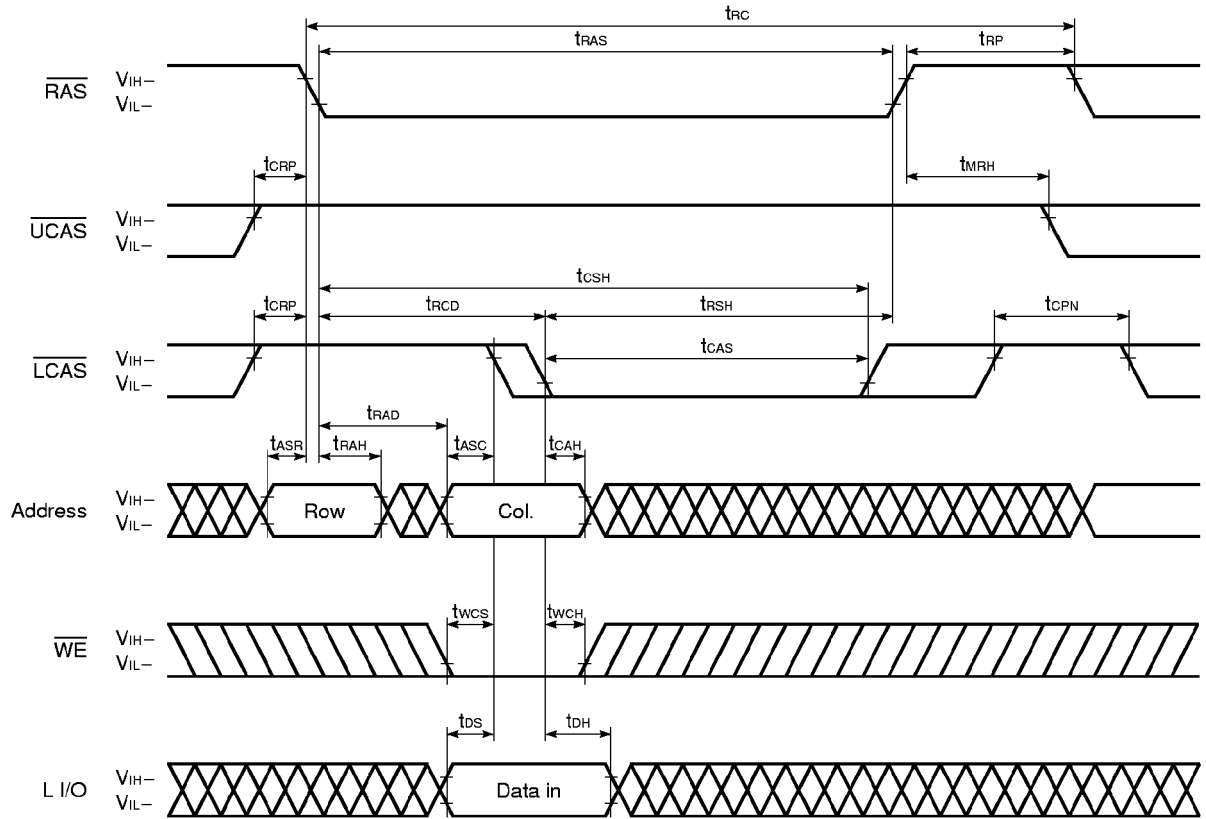
**Remark**  $\overline{OE}$ , L I/O: Don't care

DataSheet4U.com

DataShee

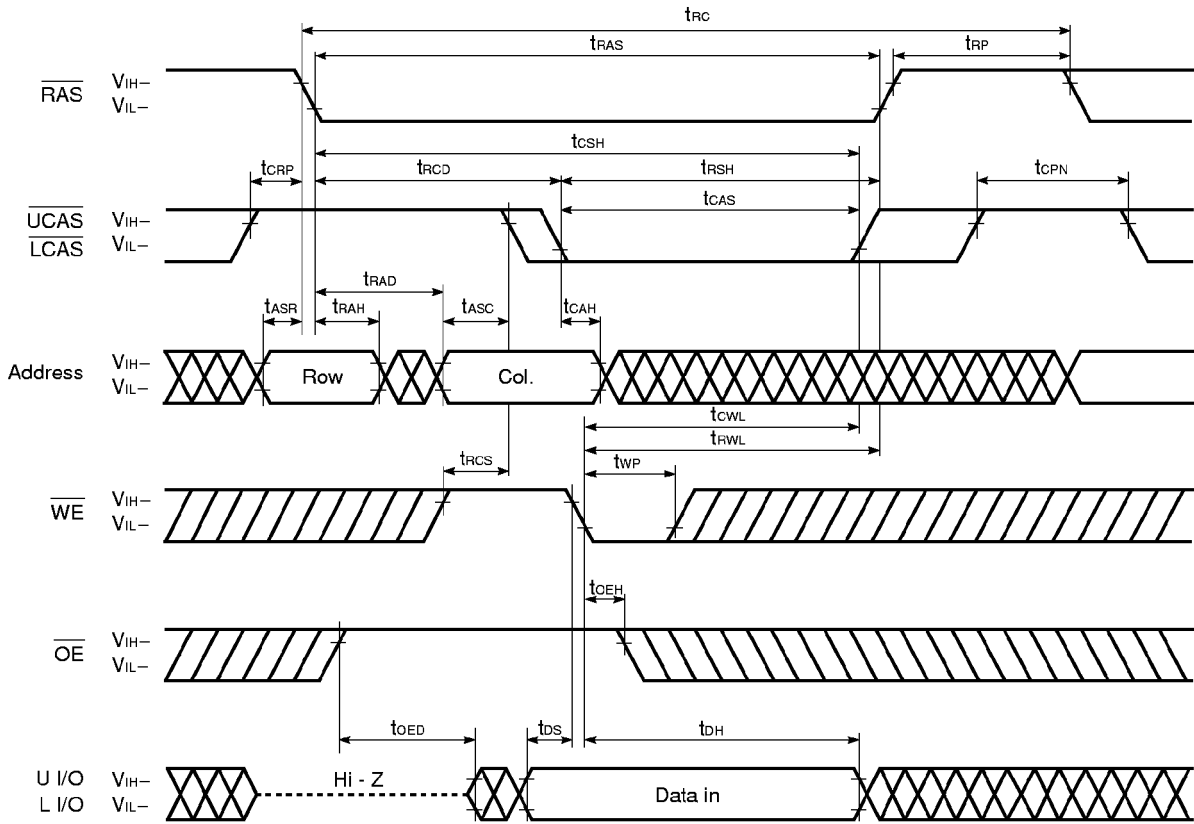


**Lower Byte Early Write Cycle**

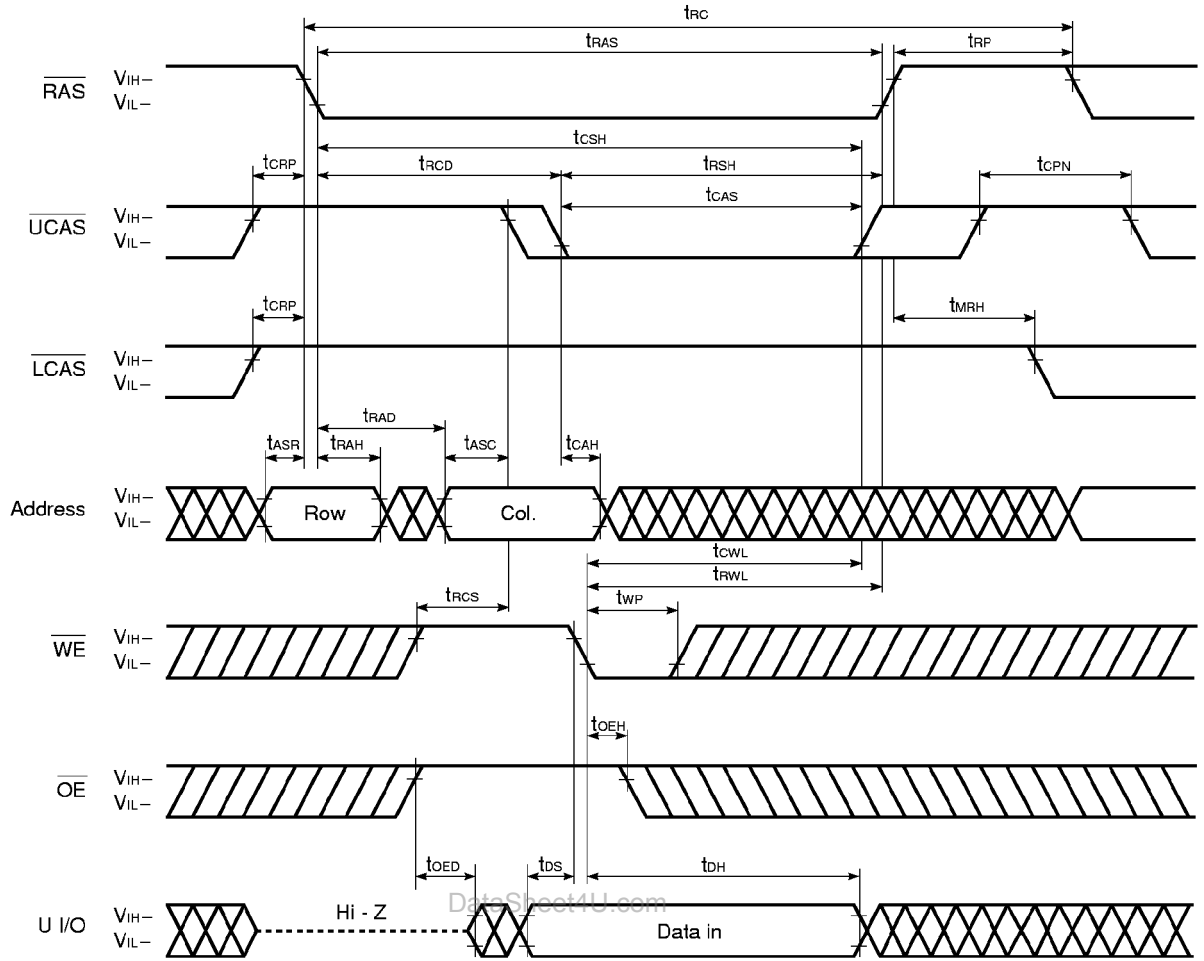


**Remark**  $\overline{OE}$ , U I/O: Don't care

**Late Write Cycle**

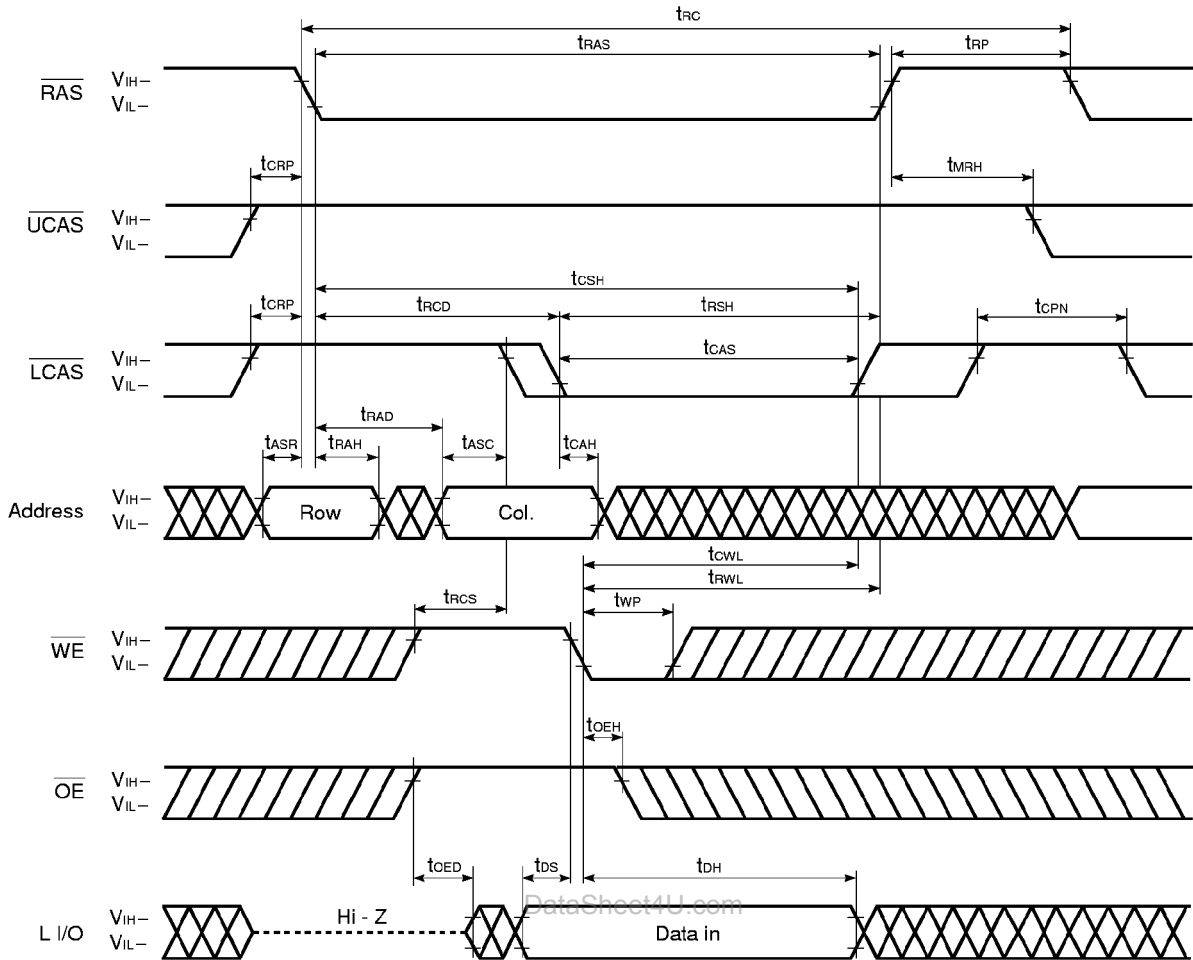


**Upper Byte Late Write Cycle**



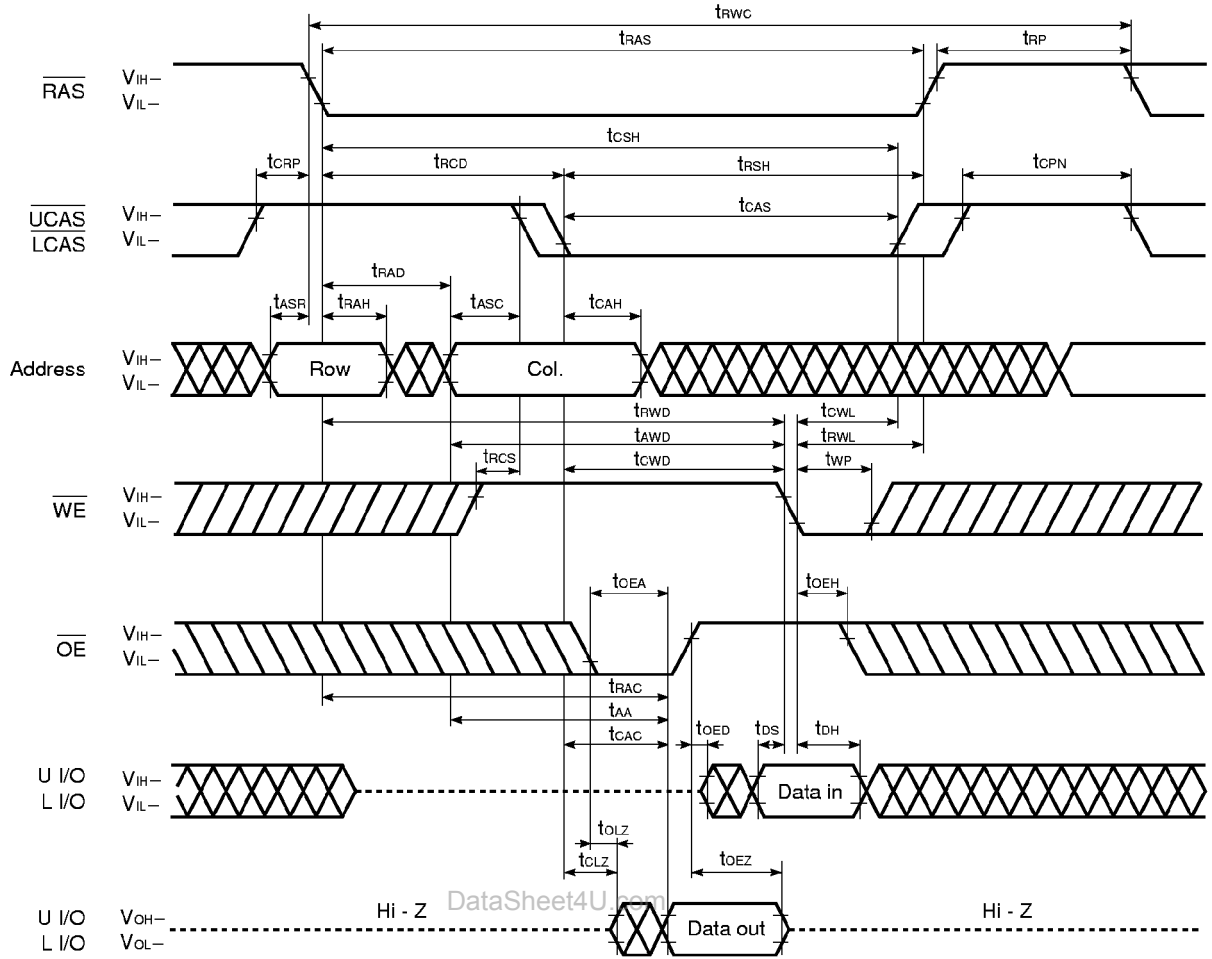
**Remark** L I/O: Don't care

**Lower Byte Late Write Cycle**

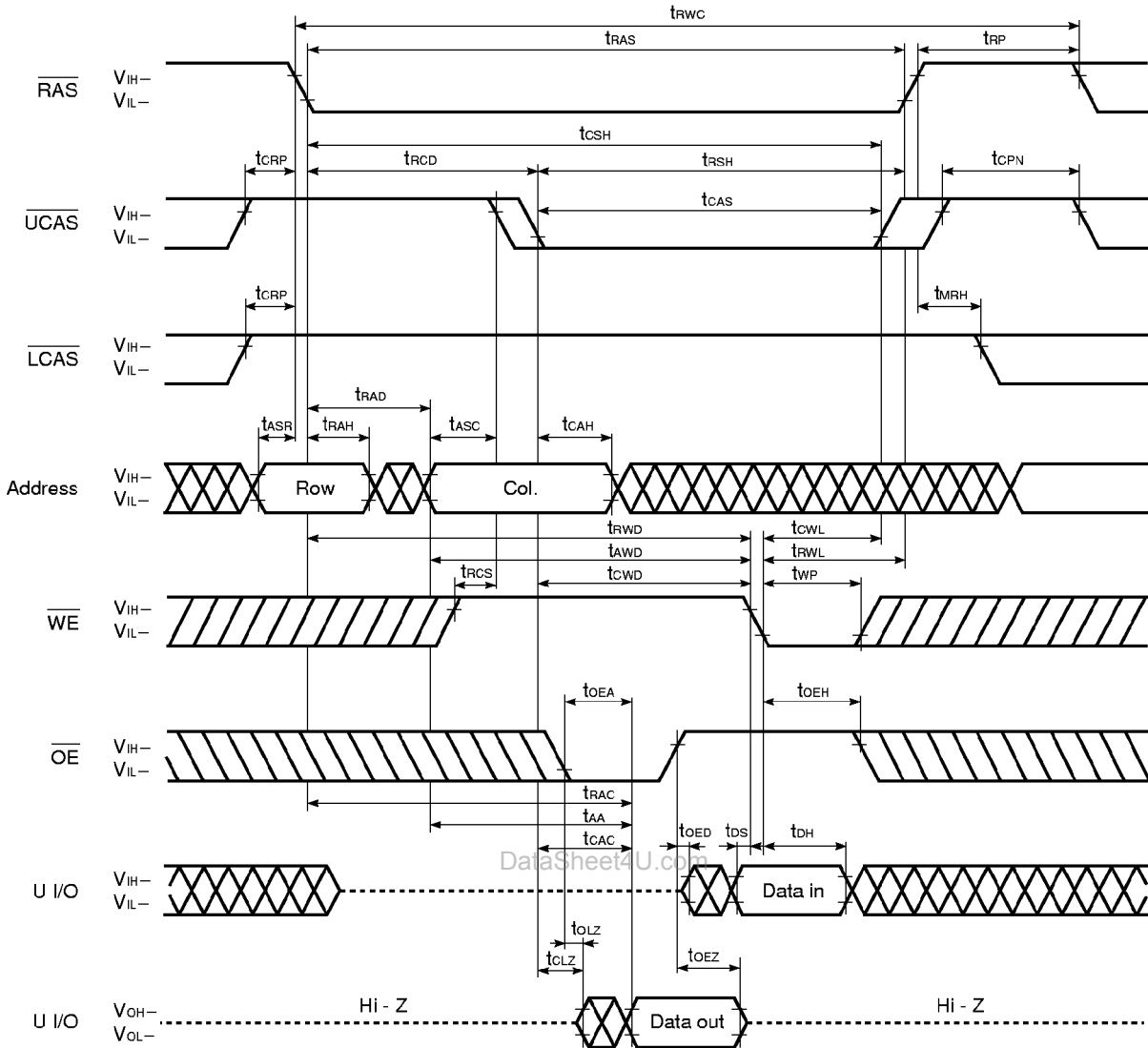


**Remark** U I/O: Don't care

**Read Modify Write Cycle**

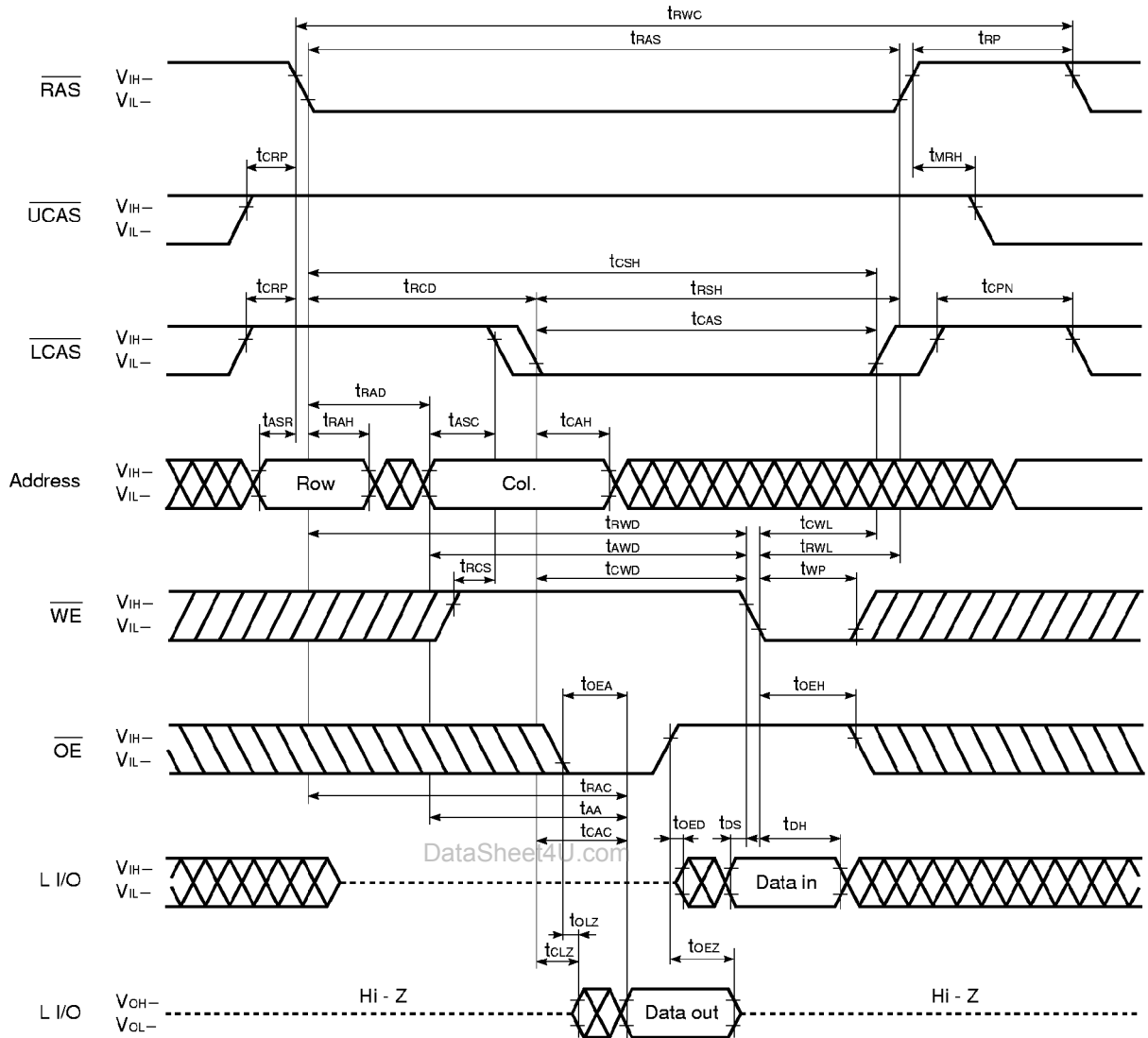


**Upper Byte Read Modify Write Cycle**



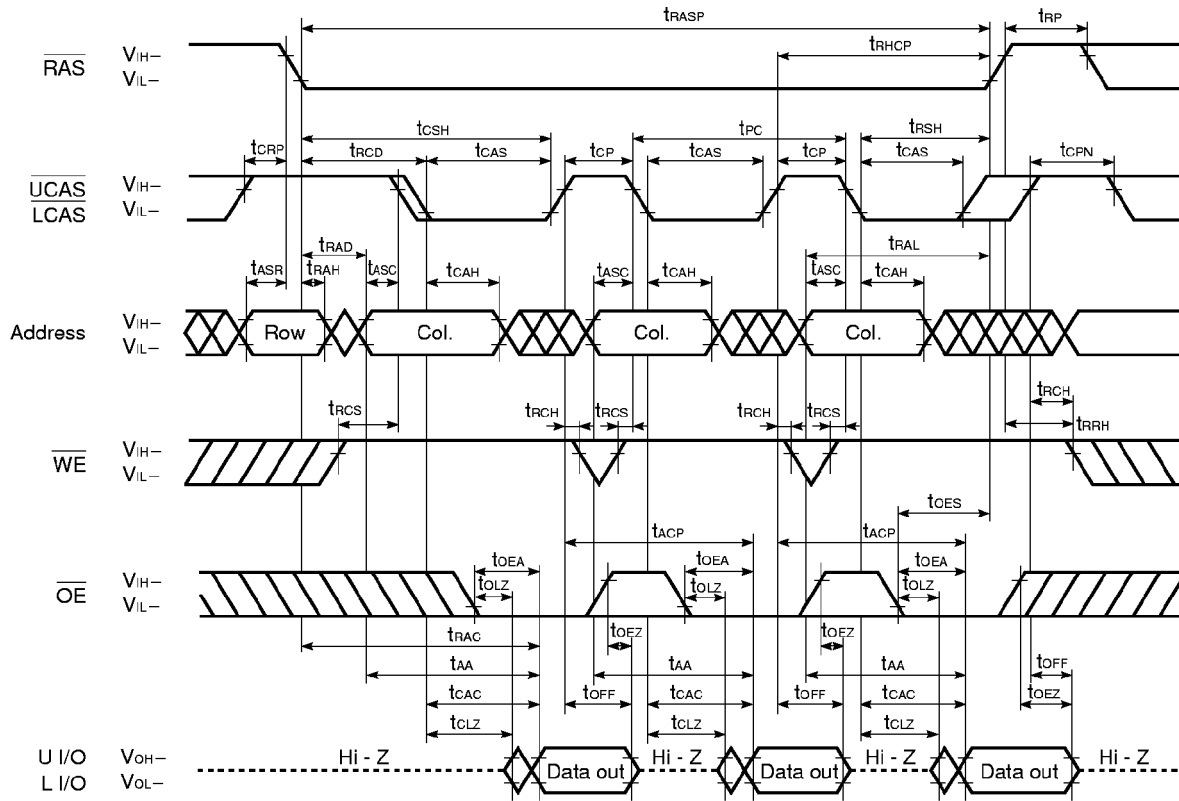
**Remark** In this cycle, the input data to Lower I/O is ineffective. The data out of that remains Hi-Z.

**Lower Byte Read Modify Write Cycle**



**Remark** In this cycle, the input data to Upper I/O is ineffective. The data out of that remains Hi-Z.

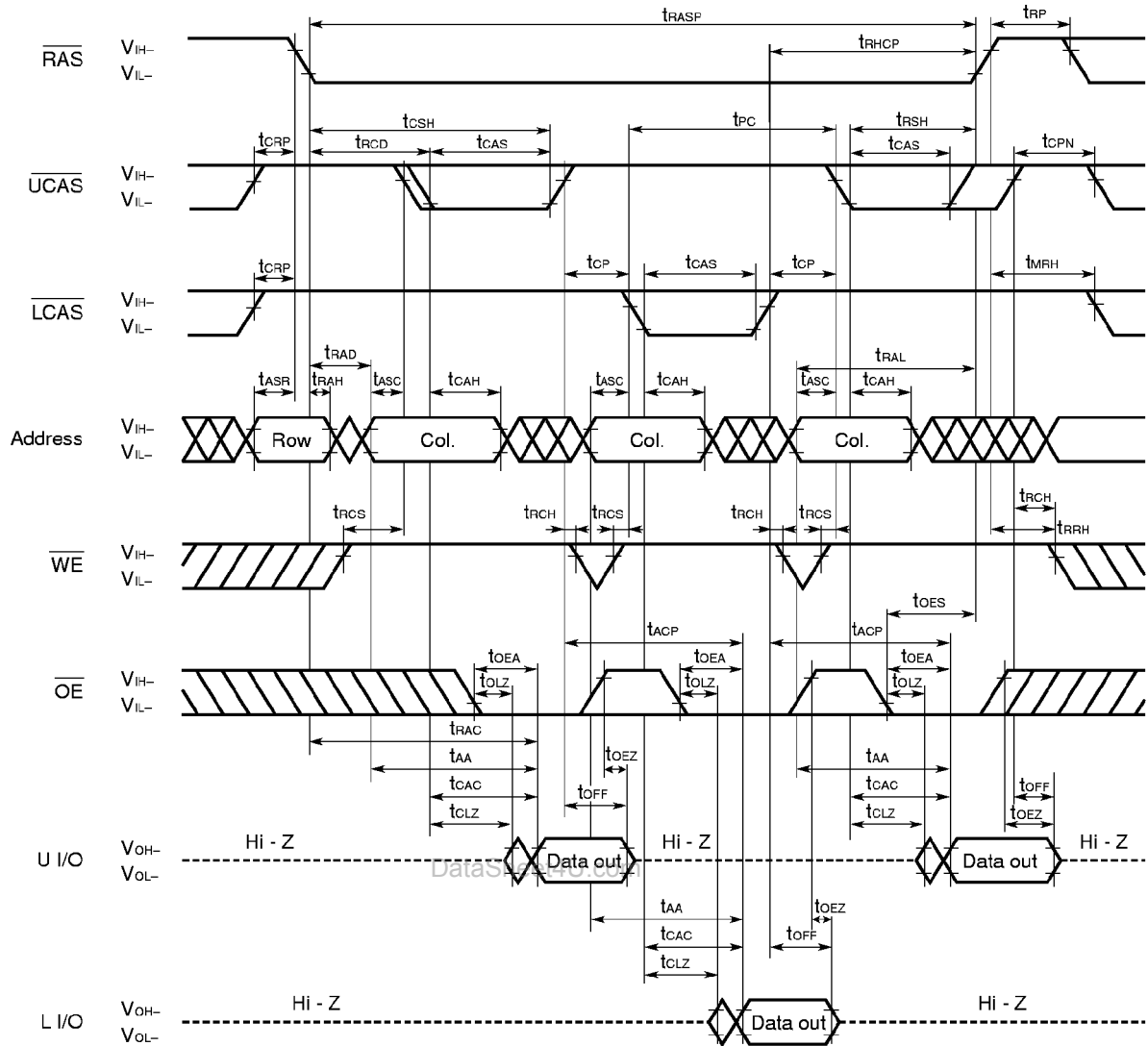
### Fast Page Mode Read Cycle



**Remark** In the fast page mode, read, write and read modify write cycles are available for each of the consecutive  $\overline{\text{CAS}}$  cycles within the same  $\overline{\text{RAS}}$  cycle.

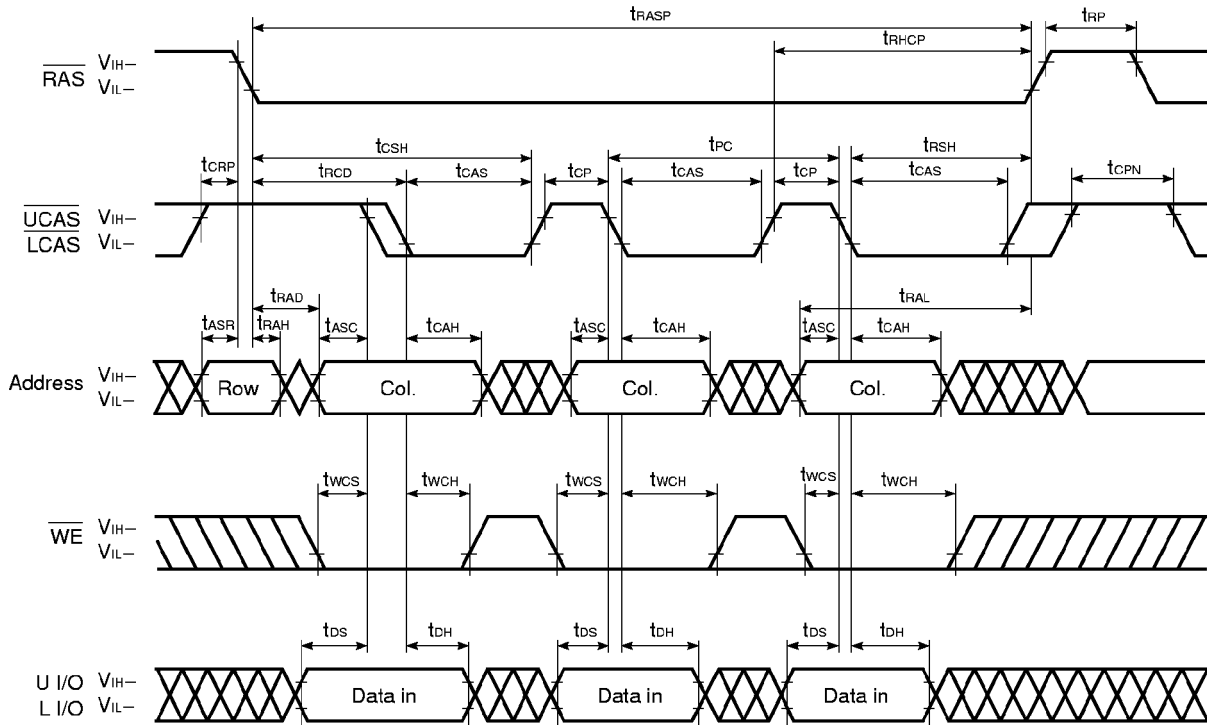


## Fast Page Mode Byte Read Cycle



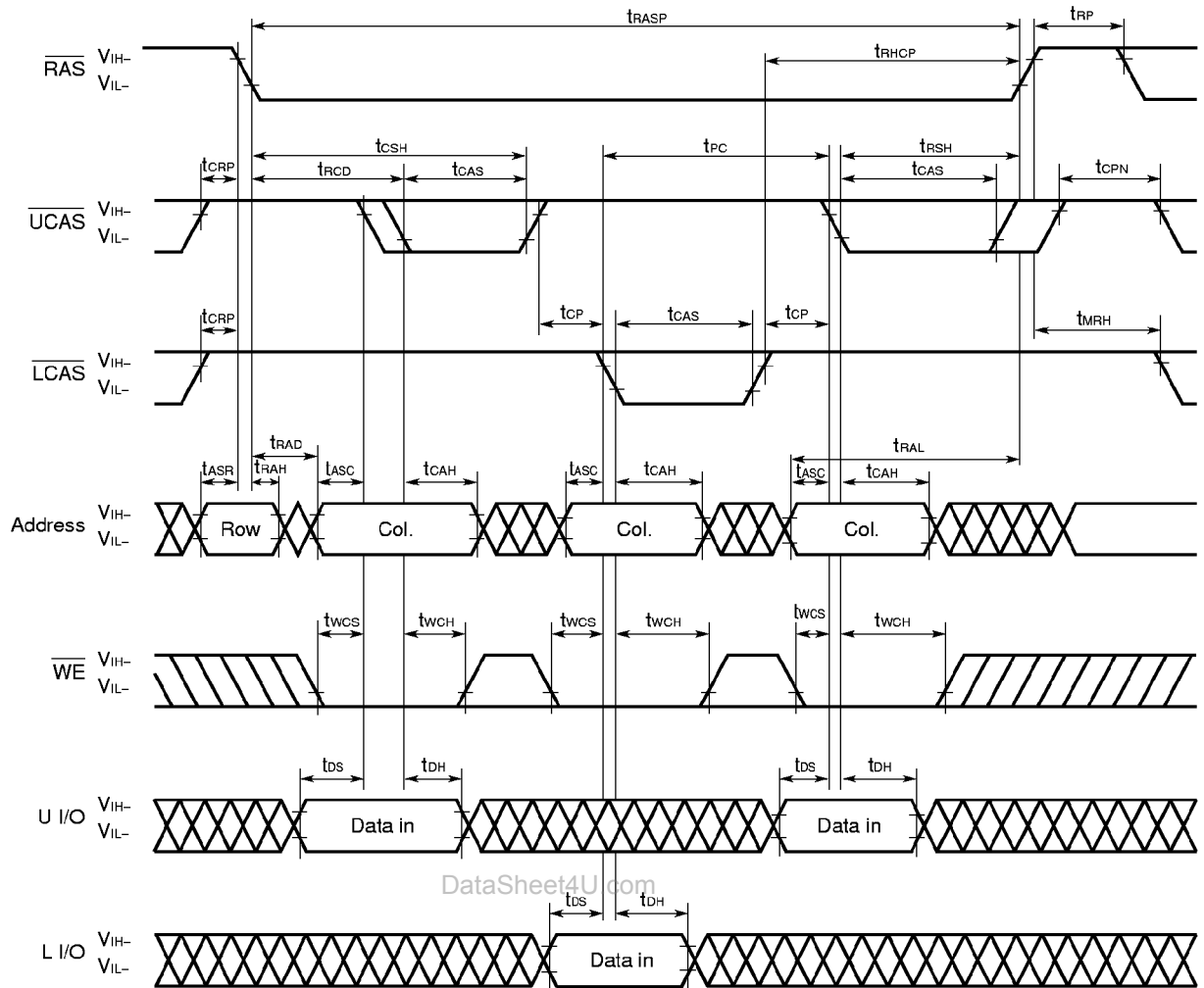
- Remarks**
1. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive  $\overline{\text{CAS}}$  cycles within the same  $\overline{\text{RAS}}$  cycle.
  2. This cycle can be used to control either  $\overline{\text{UCAS}}$  or  $\overline{\text{LCAS}}$  only. Or, it can be used to control  $\overline{\text{UCAS}}$  or  $\overline{\text{LCAS}}$  simultaneously, or at random.

## Fast Page Mode Early Write Cycle



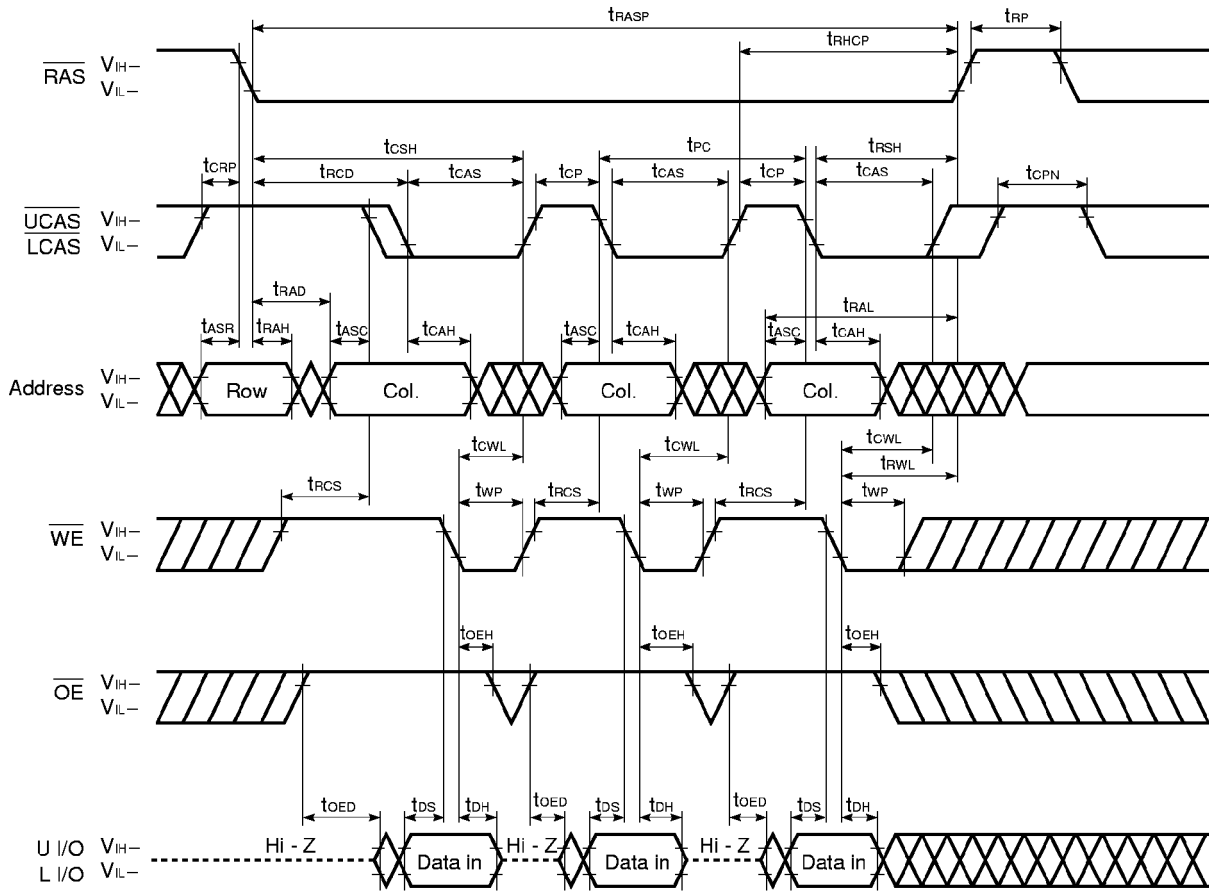
- Remarks**
1.  $\overline{OE}$ : Don't care
  2. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive  $\overline{CAS}$  cycles within the same  $\overline{RAS}$  cycle.

## Fast Page Mode Byte Early Write Cycle



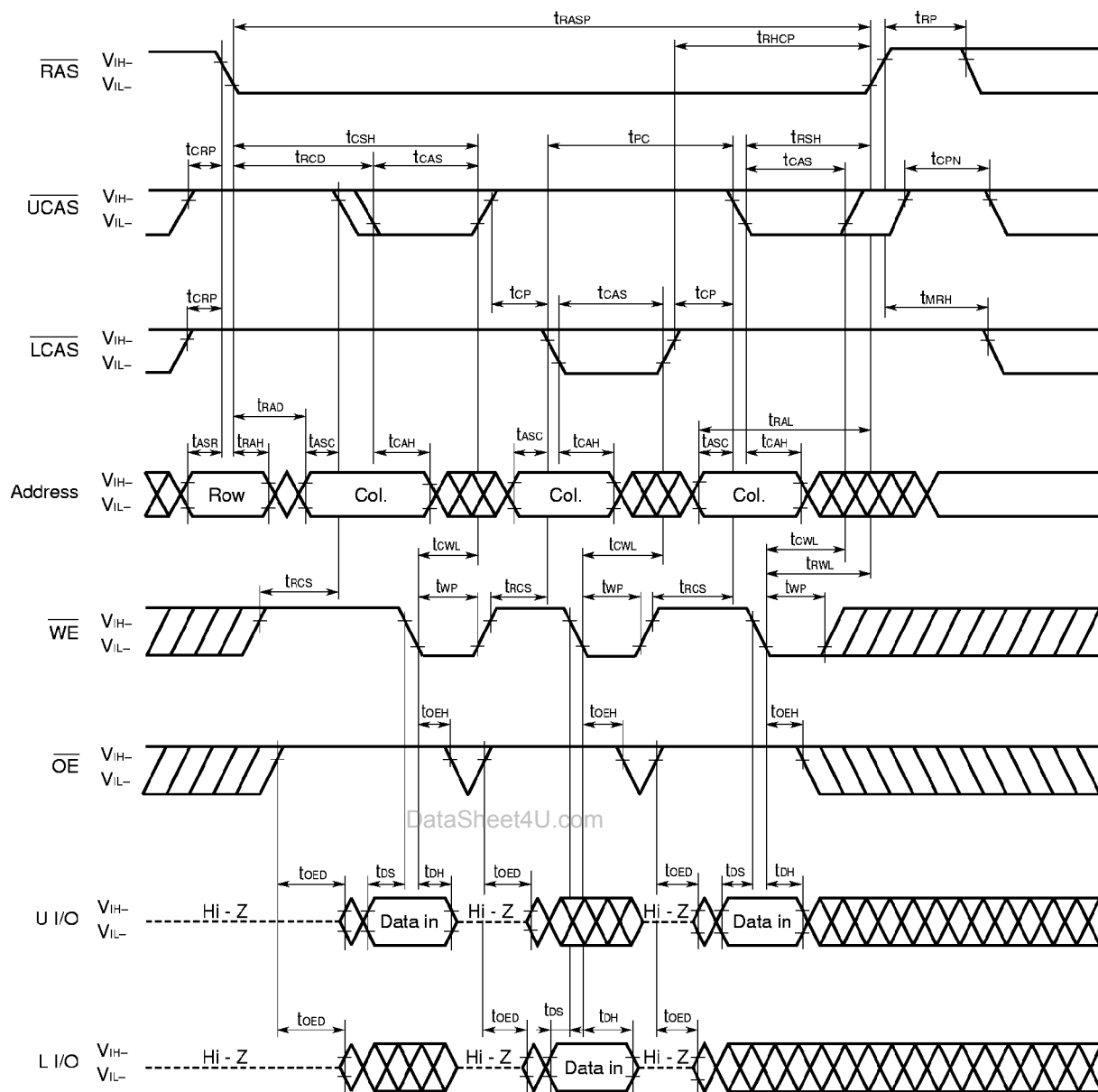
- Remarks**
1.  $\overline{OE}$ : Don't care
  2. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive  $\overline{CAS}$  cycles within the same  $\overline{RAS}$  cycle.
  3. This cycle can be used to control either  $\overline{UCAS}$  or  $\overline{LCAS}$  only. Or, it can be used to control  $\overline{UCAS}$  or  $\overline{LCAS}$  simultaneously, or at random.

**Fast Page Mode Late Write Cycle**

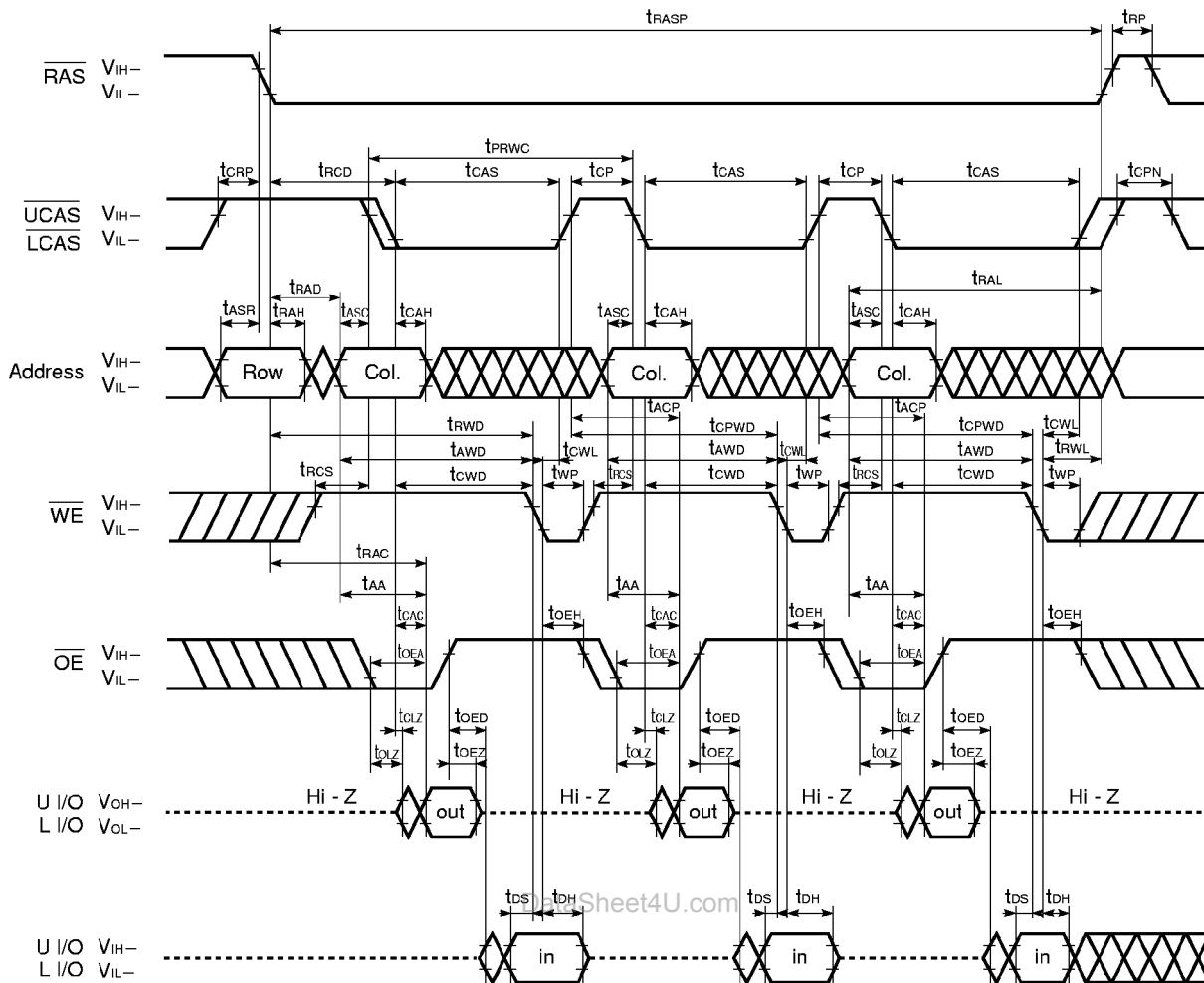


**Remark** In the fast page mode, read, write and read modify write cycles are available for each of the consecutive  $\overline{\text{CAS}}$  cycles within the same  $\overline{\text{RAS}}$  cycle.

### Fast Page Mode Byte Late Write Cycle

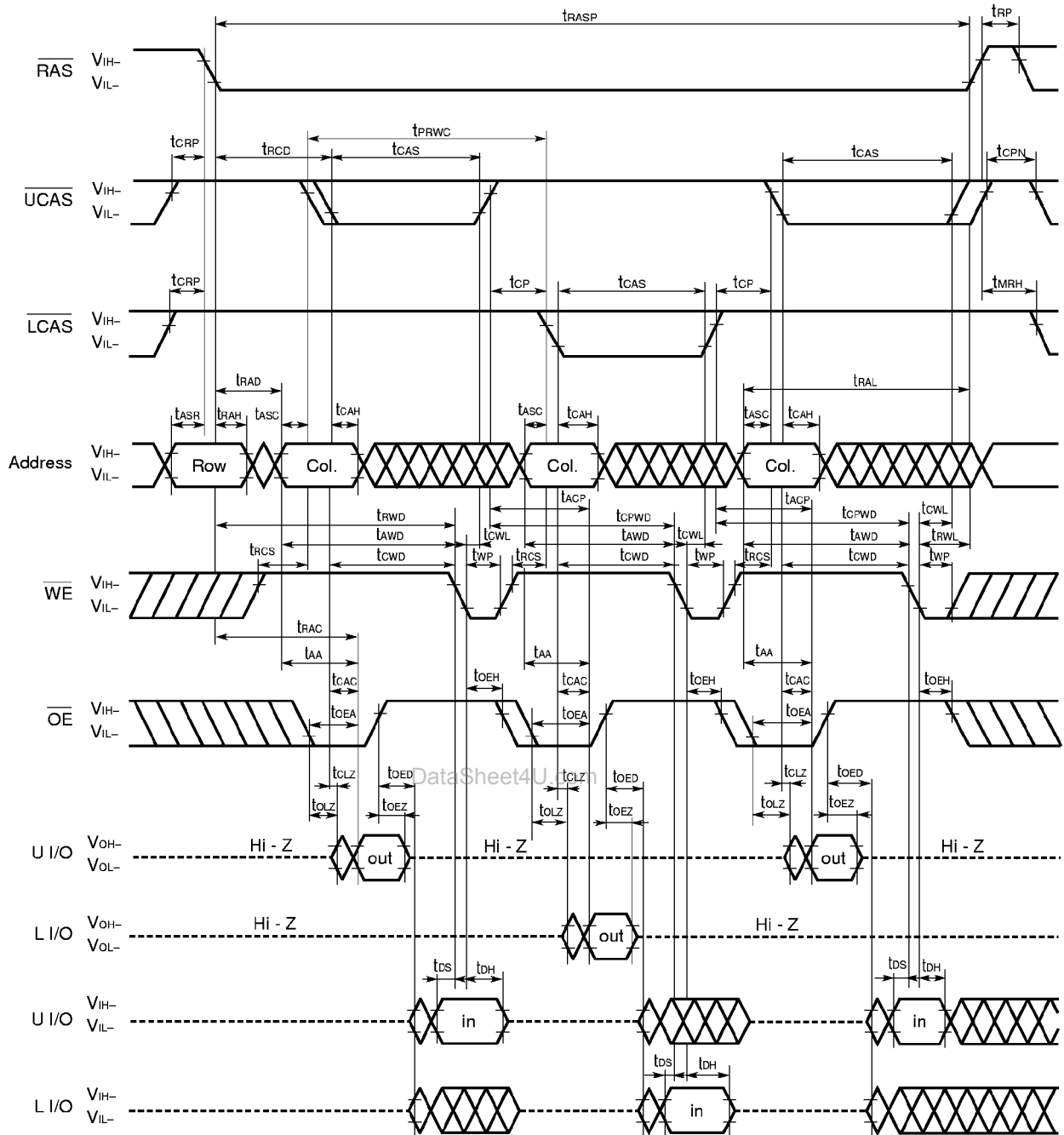


- Remarks**
1. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive  $\overline{\text{CAS}}$  cycles within the same  $\overline{\text{RAS}}$  cycle.
  2. This cycle can be used to control either  $\overline{\text{UCAS}}$  or  $\overline{\text{LCAS}}$  only. Or, it can be used to control  $\overline{\text{UCAS}}$  or  $\overline{\text{LCAS}}$  simultaneously, or at random.

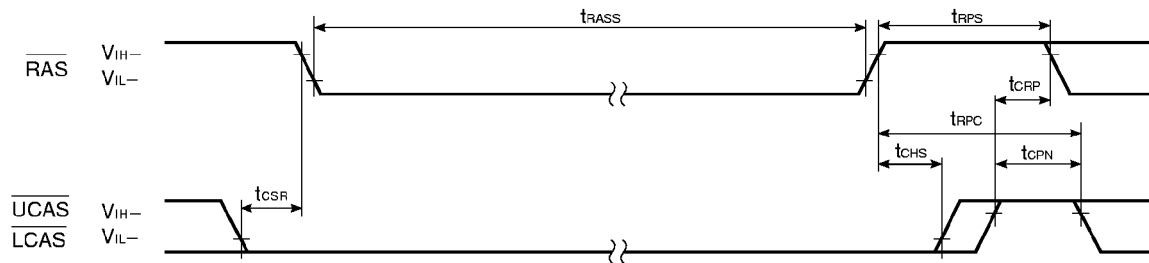
**Fast Page Mode Read Modify Write Cycle**

**Remark** In the fast page mode, read, write and read modify write cycles are available for each of the consecutive  $\overline{\text{CAS}}$  cycles within the same  $\overline{\text{RAS}}$  cycle.

## Fast Page Mode Byte Read Modify Write Cycle



- Remarks**
1. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive  $\overline{CAS}$  cycles within the same  $\overline{RAS}$  cycle.
  2. This cycle can be used to control either  $\overline{UCAS}$  or  $\overline{LCAS}$  only. Or, it can be used to control  $\overline{UCAS}$  or  $\overline{LCAS}$  simultaneously, or at random.

**CAS Before RAS Self Refresh Cycle (Only for the  $\mu$ PD42S4260AL)**

**Remark** Address,  $\overline{WE}$ ,  $\overline{OE}$ : Don't care L I/O, U I/O: Hi-Z

**Cautions on Use of CAS Before RAS Self Refresh**

CAS before RAS self refresh can be used independently when used in combination with distributed CAS before RAS long refresh; However, when used in combination with burst CAS before RAS long refresh or with long RAS only refresh (both distributed and burst), the following cautions must be observed.

**(1) Normal Combined Use of CAS Before RAS Self Refresh and Burst CAS Before RAS Long Refresh**

When CAS before RAS self refresh and burst CAS before RAS long refresh are used in combination, please perform CAS before RAS refresh 512 times within an 8 ms interval just before and after setting CAS before RAS self refresh.

**(2) Normal Combined Use of CAS Before RAS Self Refresh and Long RAS Only Refresh**

When CAS before RAS self refresh and RAS only refresh are used in combination, please perform RAS only refresh 512 times within an 8 ms interval just before and after setting CAS before RAS self refresh.

**(3) If  $t_{RASS(MIN)}$  is not satisfied at the beginning of CAS before RAS self refresh cycles ( $t_{RAS} < 100 \mu s$ ), CAS before RAS refresh cycles will be executed one time.**

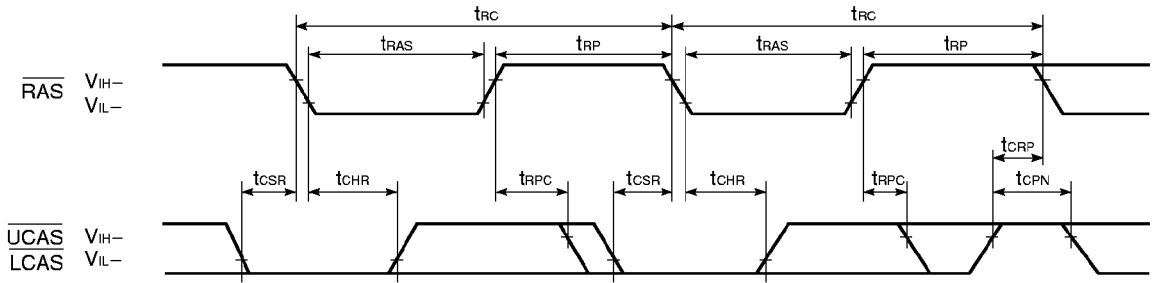
If  $10 \mu s < t_{RAS} < 100 \mu s$ , RAS precharge time for CAS before RAS self refresh ( $t_{RPS}$ ) is applied.

And refresh cycles (512/128 ms) should be met.

For details, please refer to **How to use DRAM** User's Manual.

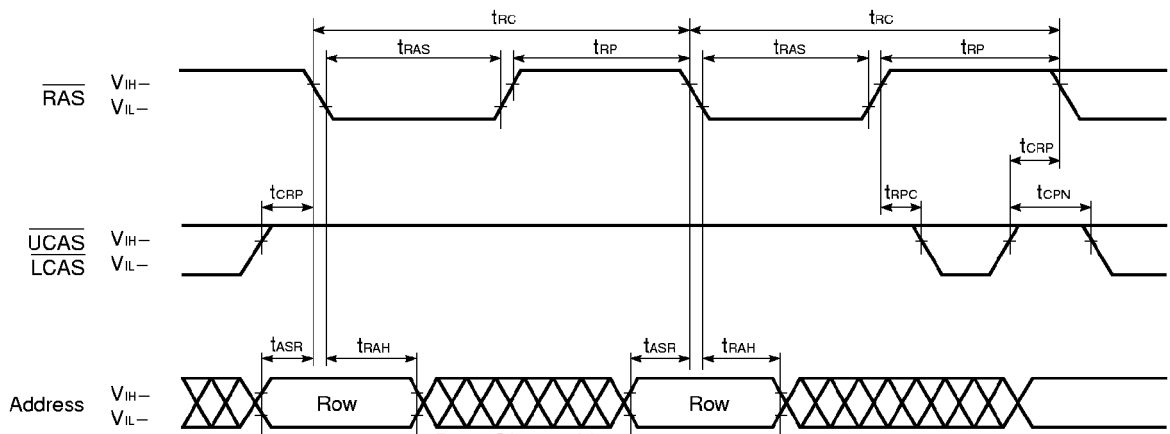


**CAS Before RAS Refresh Cycle**



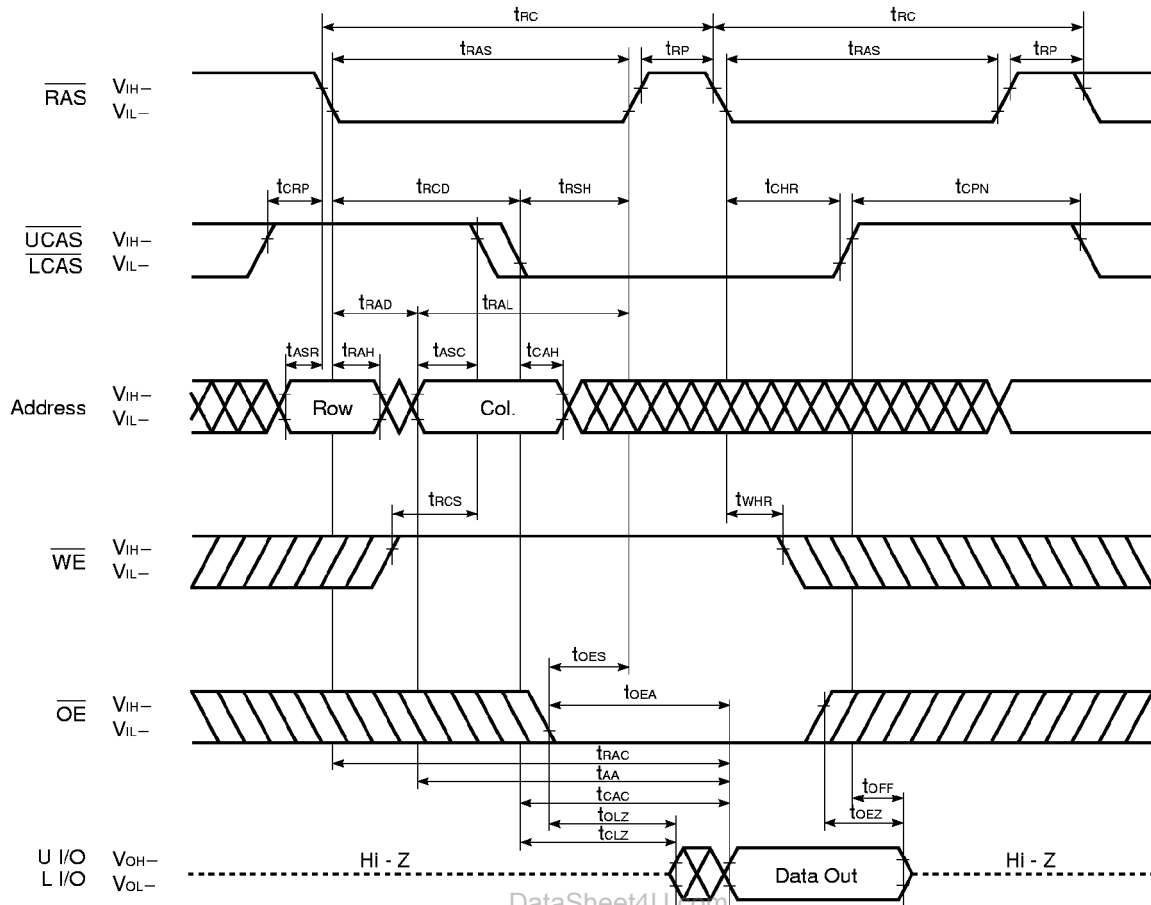
**Remark** Address,  $\overline{WE}$ ,  $\overline{OE}$ : Don't care L I/O, U I/O: Hi-Z

**RAS Only Refresh Cycle**

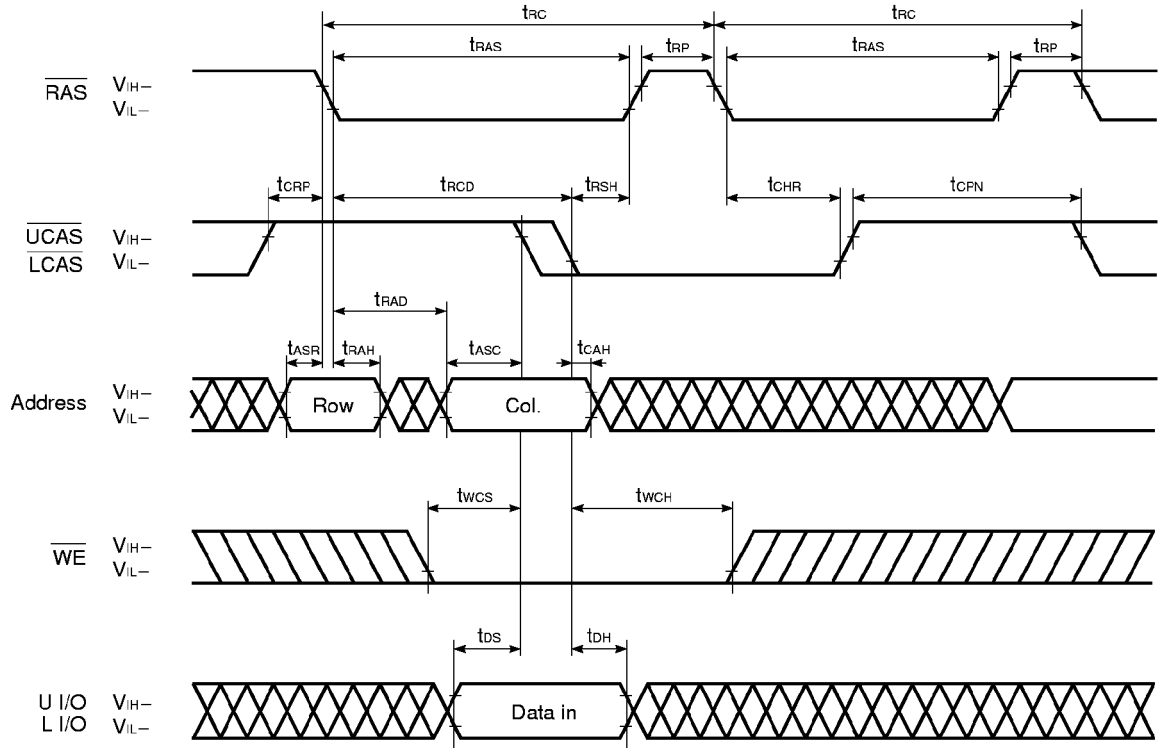


**Remark**  $\overline{WE}$ ,  $\overline{OE}$ : Don't care L I/O, U I/O: Hi-Z

**Hidden Refresh Cycle (Read)**



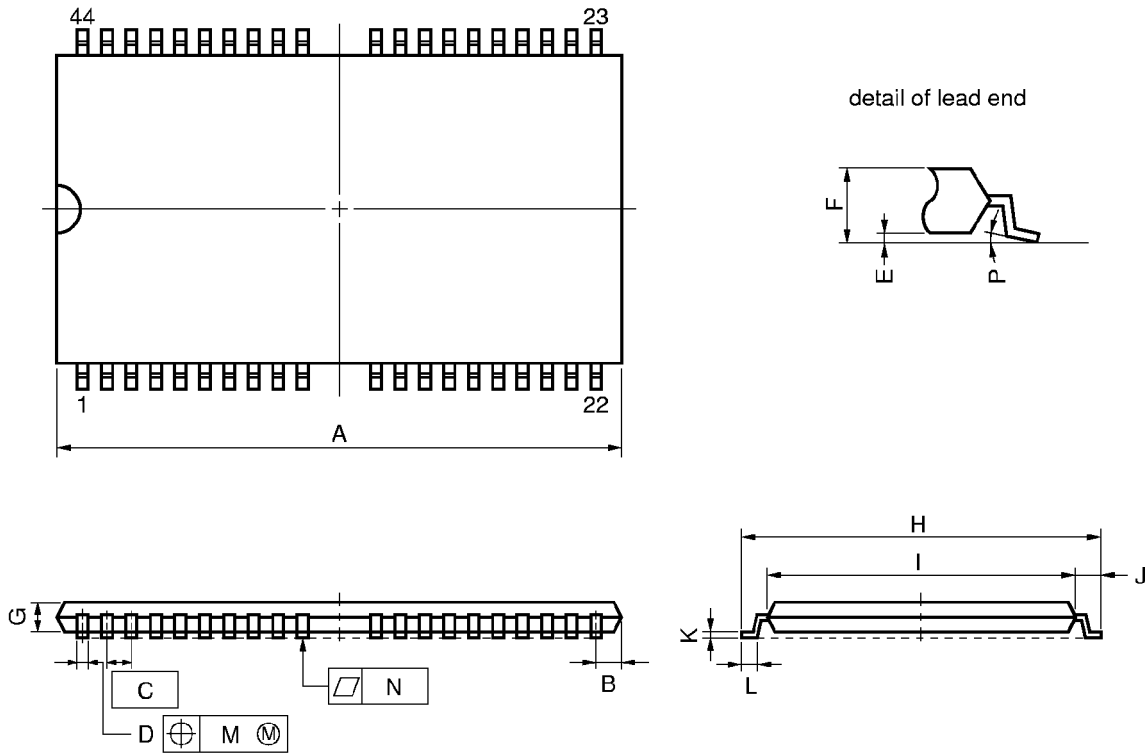
**Hidden Refresh Cycle (Write)**



**Remark**  $\overline{\text{OE}}$ : Don't care

**Package Drawings**

**44 PIN PLASTIC TSOP(II) (400 mil)**



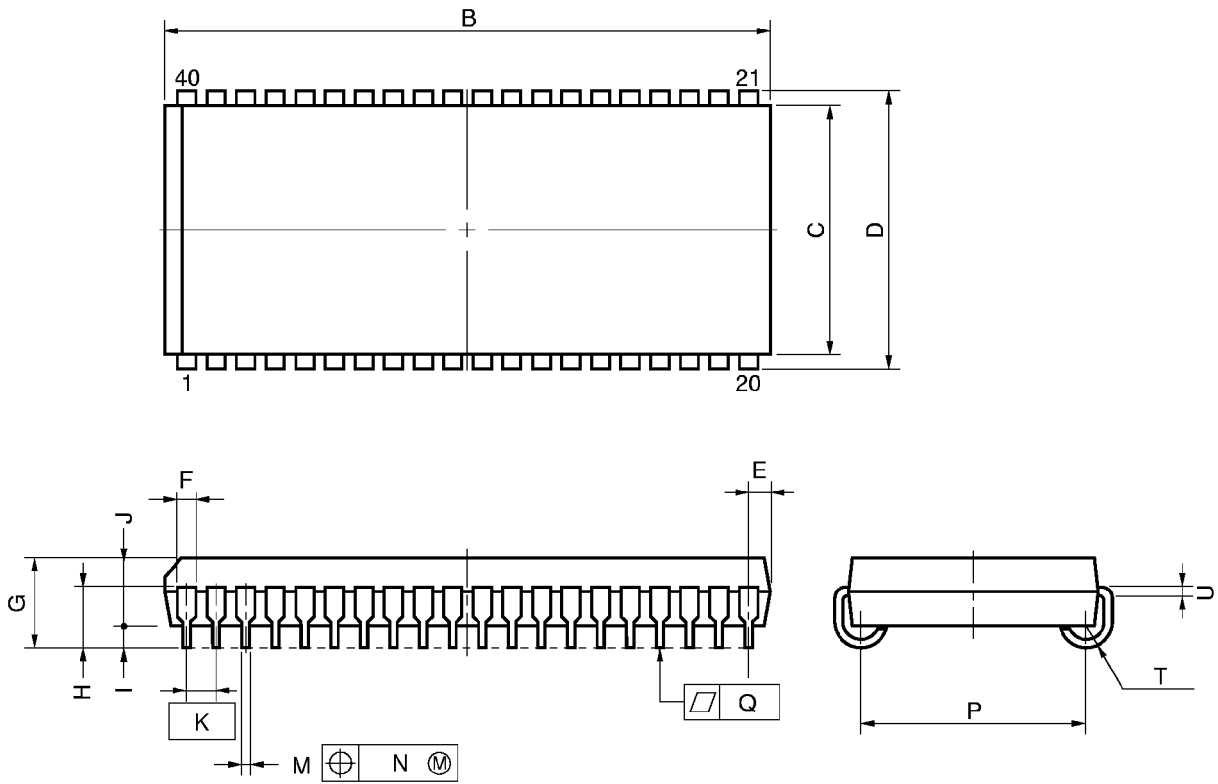
**NOTE**

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	18.63 MAX.	0.734 MAX.
B	0.93 MAX.	0.037 MAX.
C	0.8 (T.P.)	0.031 (T.P.)
D	0.32 <sup>+0.08</sup> <sub>-0.07</sub>	0.013±0.003
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	0.031 <sup>+0.009</sup> <sub>-0.008</sub>
K	0.145 <sup>+0.025</sup> <sub>-0.015</sub>	0.006±0.001
L	0.5±0.1	0.020 <sup>+0.004</sup> <sub>-0.005</sub>
M	0.13	0.005
N	0.10	0.004
P	3 <sup>+7</sup> <sub>-3</sub> °	3 <sup>+7</sup> <sub>-3</sub> °

**S44G5-80-7JF4**

**40 PIN PLASTIC SOJ (400 mil)**



**NOTE**  
 Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
B	26.29 <sup>+0.2</sup> <sub>-0.35</sub>	1.035 <sup>+0.008</sup> <sub>-0.014</sub>
C	10.16	0.400
D	11.18±0.2	0.440±0.008
E	1.08±0.15	0.043 <sup>+0.006</sup> <sub>-0.007</sub>
F	0.7	0.028
G	3.5±0.2	0.138±0.008
H	2.4±0.2	0.094 <sup>+0.009</sup> <sub>-0.008</sub>
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27(T.P.)	0.050(T.P.)
M	0.40±0.10	0.016 <sup>+0.004</sup> <sub>-0.005</sub>
N	0.12	0.005
P	9.40±0.20	0.370±0.008
Q	0.15	0.006
T	R0.85	R0.033
U	0.20 <sup>+0.10</sup> <sub>-0.05</sub>	0.008 <sup>+0.004</sup> <sub>-0.002</sub>

P40LE-400A-2

**Recommended Soldering Conditions**

Please consult with our sales offices for soldering conditions of the  $\mu$ PD42S4260AL, 424260AL.

**Types of Surface Mount Device**

$\mu$ PD42S4260ALG5-7JF, 424260ALG5-7JF: 44-pin plastic TSOP (II) (400 mil)

$\mu$ PD42S4260ALLE, 424260ALLE: 40-pin plastic SOJ (400 mil)