NCP700

Ultra Low Noise, High PSSR, BiCMOS RF LDO Regulator

Noise sensitive RF applications such as Power Amplifiers in cell phones and precision instrumentation require very clean power supplies.

The NCP700 is 150 mA LDO that provides the engineer with a very stable, accurate voltage with ultra low noise and very high Power Supply Rejection Ratio (PSRR) suitable for RF applications. In order to optimize performance for battery operated portable applications, the NCP700 employs an advanced BiCMOS process to combine the benefits of low noise and superior dynamic performance of bipolar elements with very low ground current consumption at full loads offered by CMOS.

Furthermore, in order to provide a small footprint for space-conscious applications, the NCP700 is stable with small, low value capacitors and is available in a very small DFN6 2x2.2 package.

Features

- Output Voltage Options:
  - 1.8 V, 2.8 V, 3.0 V
  - Contact Factory for Other Voltage Options
- Ultra Low Noise (typ 15 μV_{rms})
- Very High PSRR (typ 80 dB)
- Stable with Ceramic Output Capacitors as low as 1 μF
- Low Sleep Mode Current (max 1 μA)
- Active Discharge Circuit
- Current Limit Protection
- Thermal Shutdown Protection
- These are Pb-Free Devices

Typical Applications

- Cellular Telephones (Power Amplifier)
- Noise Sensitive Applications (Video, Audio)
- Analog Power Supplies
- PDAs / Palmtops / Organizers / GPS
- Battery Supplied Devices

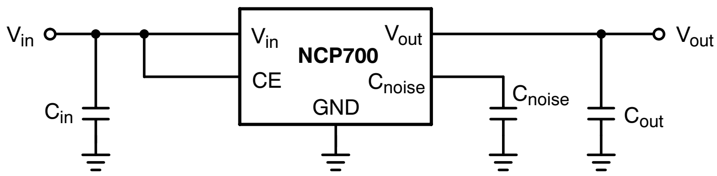
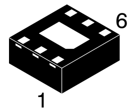


Figure 1. Typical Application Schematic

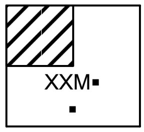
ON Semiconductor®

http://onsemi.com



6 PIN DFN
MN SUFFIX
CASE 506BA

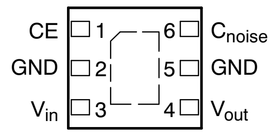
MARKING DIAGRAM



XX = Specific Device Code
M = Date Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

PIN ASSIGNMENT



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

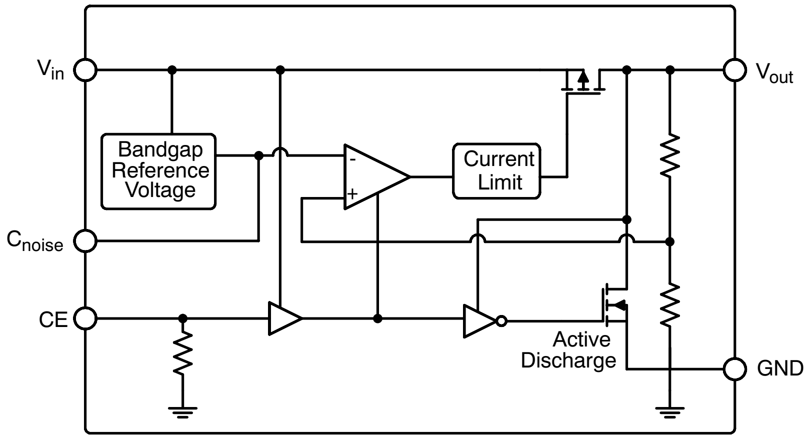


Figure 2. Simplified Block Diagram

PIN FUNCTION DESCRIPTION

DFN6 2x2.2 Pin No.	Pin Name	Description
1	CE	Chip Enable: This pin allows on/off control of the regulator. To disable the device, connect to GND. If this function is not in use, connect to V_{in}. Internal 5 MΩ Pull Down resistor is connected between CE and GND.
2, 5, EPAD	GND	Power Supply Ground (Pins are fused for the DFN package)
3	V_{in}	Power Supply Input Voltage
4	V_{out}	Regulated Output Voltage
6	C_{noise}	Noise reduction pin. (Connect 100 nF or 10 nF capacitor to GND)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage (Note 1)	V_{in}	-0.3 V to 6 V	V
Chip Enable Voltage	V_{CE}	-0.3 V to V_{in} +0.3 V	V
Noise Reduction Voltage	V_{Cnoise}	-0.3 V to V_{in} +0.3 V	V
Output Voltage	V_{out}	-0.3 V to V_{in} +0.3 V	V
Maximum Junction Temperature (Note 1)	$T_{J(max)}$	150	°C
Storage Temperature Range	T_{STG}	-55 to 150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

NOTE: This device series contains ESD protection and exceeds the following tests:
Human Body Model 2000 V per MIL-STD-883, Method 3015
Machine Model Method 200 V

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Package Thermal Resistance, DFN6: (Note 1) Junction-to-Lead (pin 2) Junction-to-Ambient	$R_{\theta JA}$	 37 120	°C/W

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area

ELECTRICAL CHARACTERISTICS

(V_{in} = V_{out} + 1.0 V, V_{CE} = 1.2 V, C_{in} = 0.1 μF, C_{out} = 1 μF, C_{noise} = 10 nF, T_A = -40°C to 85°C, unless otherwise specified (Note 2))

Characteristic	Test Conditions	Symbol	Min	Typ	Max	Unit
REGULATOR OUTPUT						
Input Voltage		V_{in}	2.5	-	5.5	V
Output Voltage (Note 3) 1.8 V 2.8 V 3.0 V	V_{in} = (V_{out} +1.0 V) to 5.5 V I_{out} = 1 mA	V_{out}	1.764 2.744 2.940	- - -	1.836 2.856 3.060	V
Output Voltage (Note 3) 1.8 V 2.8 V 3.0 V	V_{in} = (V_{out} +1.0 V) to 5.5 V I_{out} = 1 mA to 150 mA	V_{out}	1.746 2.716 2.910	- - -	1.854 2.884 3.090	V
Power Supply Ripple Rejection	V_{in} = V_{out} +1.0 V + 0.5 V_{p-p} I_{out} = 1 mA to 150 mA f = 120 Hz C_{noise} = 100nF f = 1 kHz f = 10 kHz	PSRR	 - - -	 80 80 65	 - - -	dB
Line Regulation	V_{in} = (V_{out} +1.0 V) to 5.5 V, I_{out} = 1 mA	Reg_{line}	-0.2	-	0.2	%/V
Load Regulation	I_{out} = 1 mA to 150 mA	Reg_{load}	-	12	25	mV
Output Noise Voltage	f = 10 Hz to 100 kHz I_{out} = 1 mA to 150 mA C_{noise} = 100 nF C_{noise} = 10 nF	V_n	 - -	 15 20	 - -	μV_{rms}
Output Current Limit	V_{out} = $V_{out(nom)}$ – 0.1 V	I_{LIM}	150	310	470	mA
Output Short Circuit Current	V_{out} = 0 V	I_{SC}	150	320	490	mA
Dropout Voltage (Note 4) 2.8 V 3.0 V	I_{out} = 150 mA	V_{DO}	- -	105 100	155 150	mV
GENERAL						
Ground Current	I_{out} = 1 mA I_{out} = 150 mA	I_{GND}	- -	70 110	90 220	μA
Disable Current	V_{CE} = 0 V	I_{DIS}	-	0.1	1	μA
Thermal Shutdown Threshold (Note 5)		T_{SD}	-	150	-	°C
Thermal Shutdown Hysteresis (Note 5)		T_{SH}	-	20	-	°C
CHIP ENABLE						
Input Threshold Low High		$V_{th(CE)}$	- 1.2	- -	0.4 -	V
Internal Pull-Down Resistance (Note 6)		$R_{PD(CE)}$	2.5	5	10	MΩ
TIMING						
Turn-on Time	I_{out} = 150 mA C_{noise} = 10 nF C_{noise} = 100 nF	t_{on}	- -	0.4 4	- -	ms
Turn-off Time	C_{noise} = 10 nF/100 nF I_{out} = 1 mA I_{out} = 10 mA	t_{off}	- -	800 200	- -	μs

2. Performance guaranteed over the indicated operating temperature range by design and/or characterization, production tested at T_J = T_A = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
3. Contact factory for other voltage options.
4. Measured when the output voltage falls 100 mV below the regulated voltage at V_{in} = V_{out} + 1.0 V
If V_{out} < 2.5 V, then V_{DO} = V_{in} - V_{out} at V_{in} = 2.5 V.
5. Guaranteed by design and characterization.
6. Expected to disable device when CE pin is floating.

TYPICAL CHARACTERISTICS

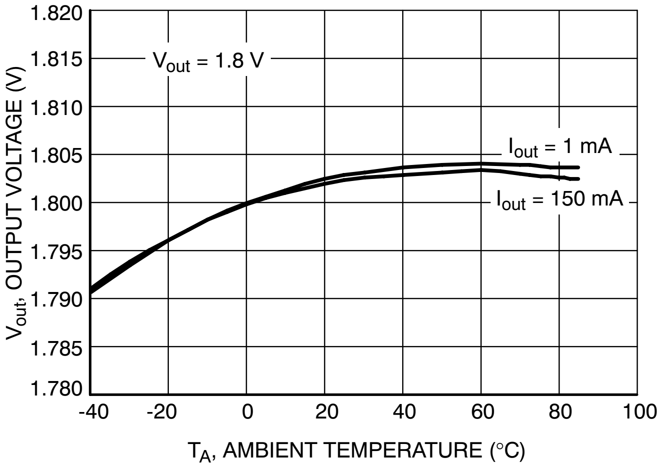


Figure 3. Output Voltage vs. Temperature (V_{out} = 1.8 V)

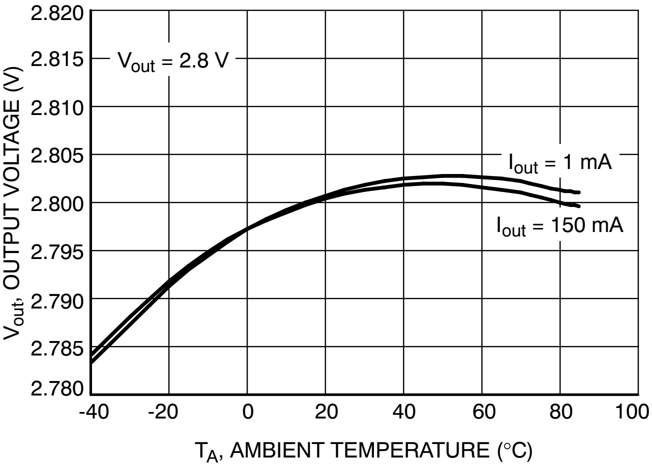


Figure 4. Output Voltage vs. Temperature (V_{out} = 2.8 V)

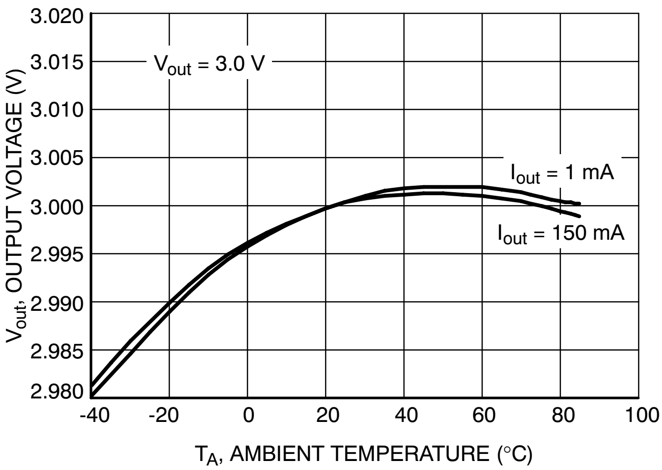


Figure 5. Output Voltage vs. Temperature (V_{out} = 3.0 V)

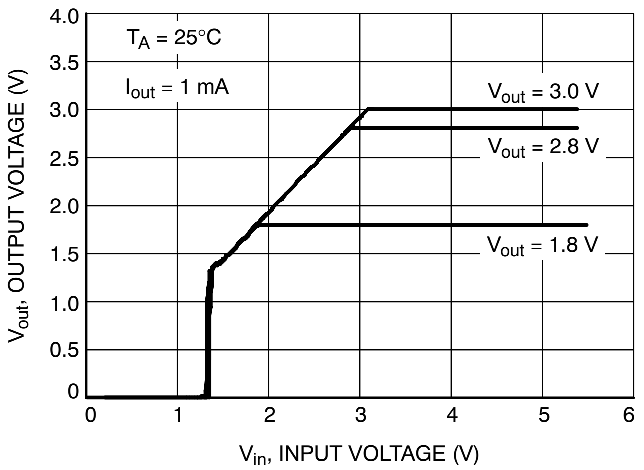


Figure 6. Output Voltage vs. Input Voltage

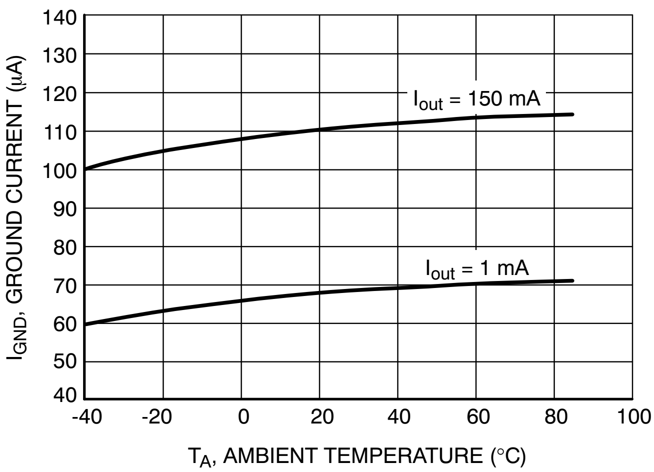


Figure 7. Ground Current vs. Temperature

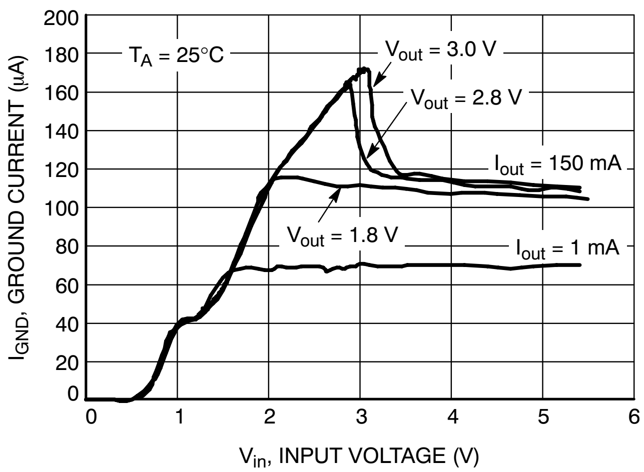


Figure 8. Ground Current vs. Input Voltage

TYPICAL CHARACTERISTICS

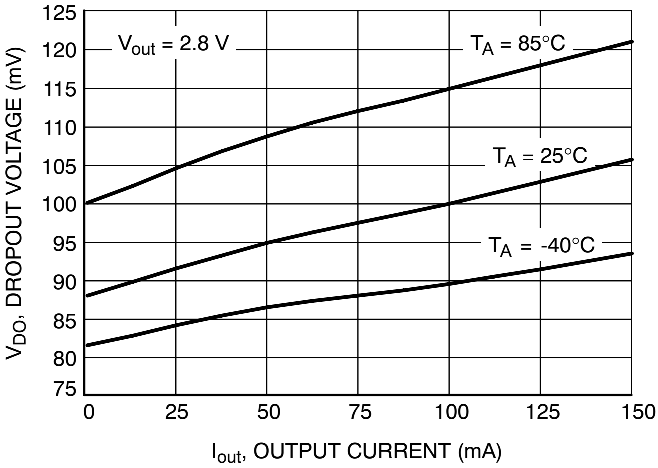


Figure 9. Dropout Voltage vs. Output Current

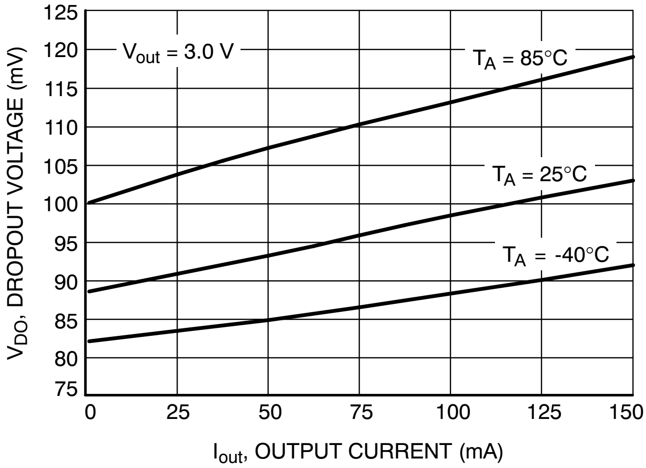


Figure 10. Dropout Voltage vs. Output Current

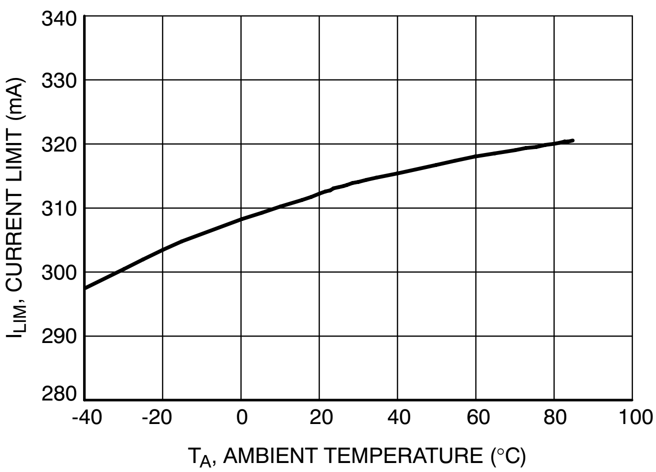


Figure 11. Current Limit vs. Temperature

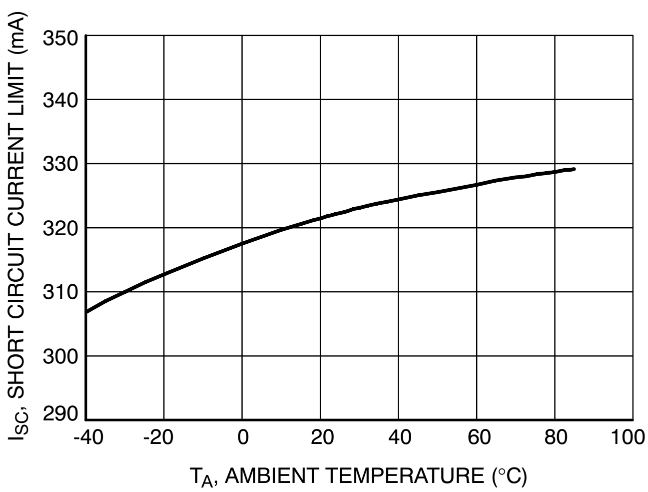


Figure 12. Short Circuit Current vs. Temperature

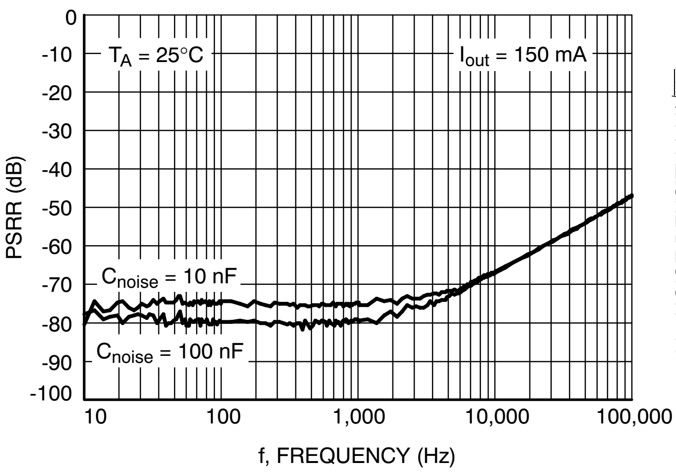


Figure 13. PSRR vs. Frequency

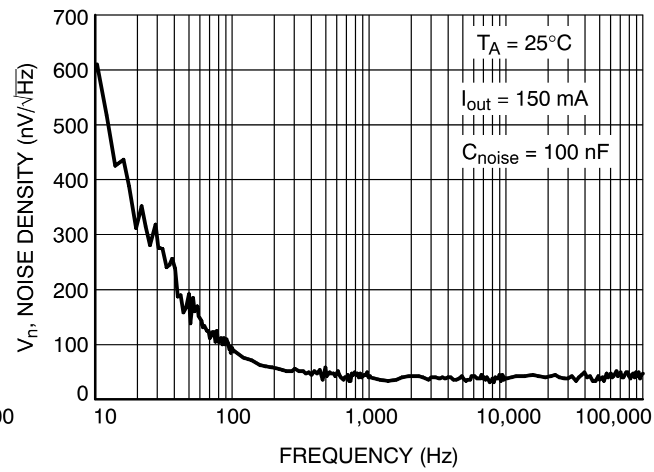


Figure 14. Noise Density vs. Frequency

TYPICAL CHARACTERISTICS

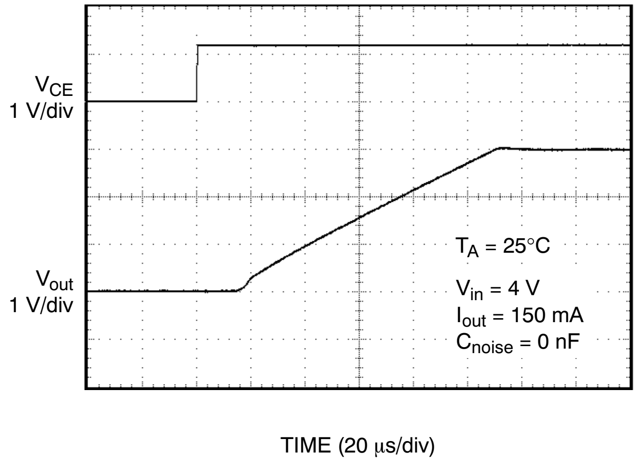


Figure 15. Enable Voltage and Output Voltage vs. Time (Start-Up)

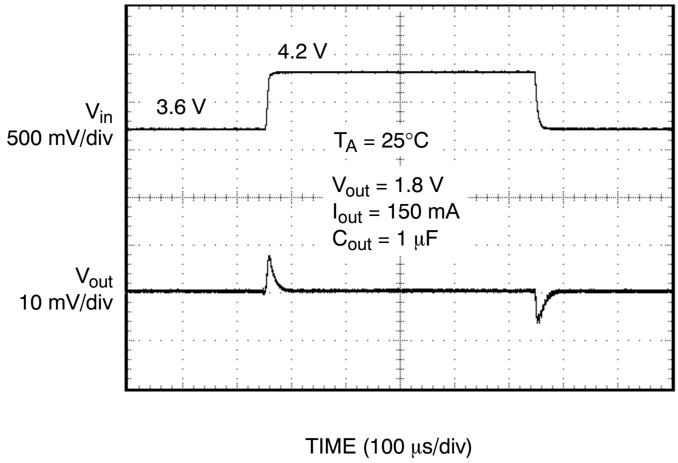


Figure 16. Line Transient

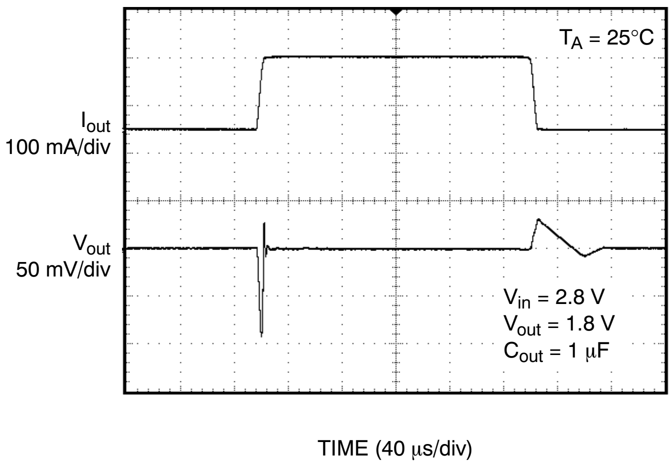


Figure 17. Load Transient

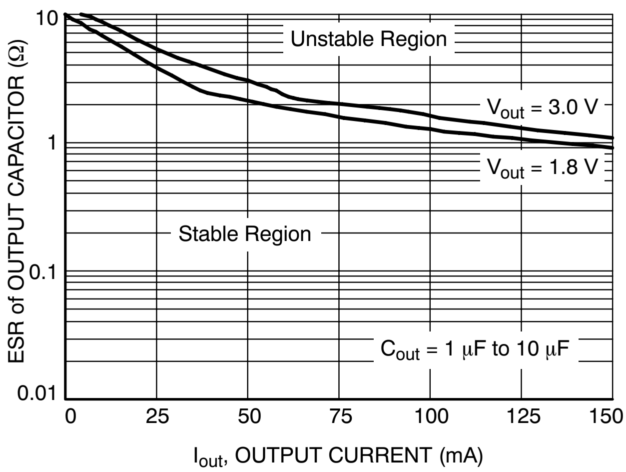


Figure 18. Output Capacitor ESR vs. Output Current

APPLICATION INFORMATION

General

The NCP700 is a 150 mA (current limited) linear regulator with a logic input for on/off control for the high speed turn-off output voltage.

Access to the major contributor of noise within the integrated circuit is provided as the focus for noise reduction within the linear regulator system.

Power Up/Down

During power up, the NCP700 maintains a high impedance output (V_{out}) until sufficient voltage is present on V_{in} to power the internal bandgap reference voltage. When sufficient voltage is supplied (approx 1.2 V), V_{out} will start to turn on (assume CE shorted to V_{in}), linearly increasing until the output regulation voltage has been reached.

Active discharge circuitry has been implemented to insure a fast turn off time. Then CE goes low, the active discharge transistor turns on creating a fast discharge of the output voltage. Power to drive this circuitry is drawn from the output node. This is to maintain the lowest quiescent current when in the sleep mode (V_{CE} = 0.4 V). This circuitry subsequently turns off when the output voltage discharges.

CE (chip enable)

The enable function is controller by the logic pin CE. The voltage threshold of this pin is set between 0.4 V and 1.2 V. A voltage lower than 0.4 V guarantees the device is off. A voltage higher than 1.2 V guarantees the device is on. The NCP700 enters a sleep mode when in the off state drawing less than 1 μA of quiescent current.

The device can be used as a simple regulator without use of the chip enable feature by tying the CE pin to the V_{in} pin.

Current Limit

Output Current is internally limited within the IC to a minimum of 150 mA. The design is set to a higher value to allow for variation in processing and the temperature coefficient of the parameter. The NCP700 will source this amount of current measured with a voltage 100 mV lower than the typical operating output voltage.

The specification for short circuit current limit (@ V_{out} = 0 V) is specified at 320 mA (typ). There is no additional circuitry to lower the current limit at low output voltages. This number is provided for informational purposes only.

Output Capacitor

The NCP700 has been designed to work with low ESR ceramic capacitors. There is no ESR lower limit for stability for the recommended 1 μF output capacitor. Stable region for Output capacitor ESR vs Output Current is shown in Figure 18.

Output Noise

The main contributor for noise present on the output pin V_{out} is the reference voltage node. This is because any noise which is generated at this node will be subsequently amplified through the error amplifier and the PMOS pass device. Access to the reference voltage node is supplied directly through the C_{noise} pin. Noise can be reduced from a typical value of 20 μV_{rms} by using 10 nF to 15 μV_{rms} by using a 100 nF from the C_{noise} pin to ground.

A bypass capacitor is recommended for good noise performance and better load transient response.

Thermal Shutdown

When the die temperature exceeds the Thermal Shutdown threshold, a Thermal Shutdown (TSD) event is detected and the output (V_{out}) is turned off. There is no effect from the active discharge circuitry. The IC will remain in this state until the die temperature moves below the shutdown threshold (150°C typical) minus the hysteresis factor (20°C typical).

This feature provides protection from a catastrophic device failure due to accidental overheating. It is not intended to be used as a substitute for proper heat sinking. The maximum device power dissipation can be calculated by:

$$P_D = \frac{T_J - T_A}{R_{\theta JA}}$$

Thermal resistance value versus copper area and package is shown in Figure 19.

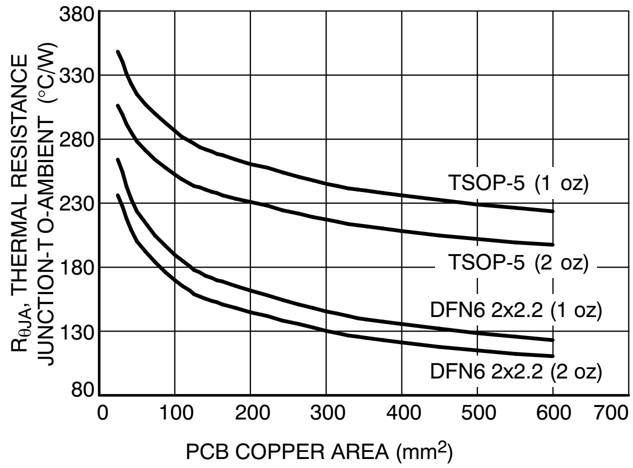


Figure 19. $R_{\theta JA}$ vs. PCB Copper Area

(TSOP-5 for comparison only)

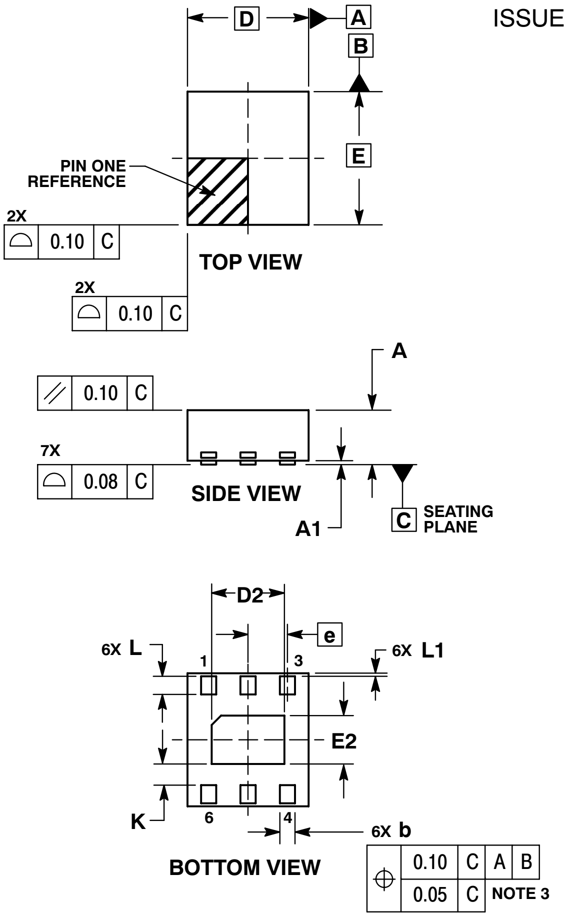
ORDERING INFORMATION

Device	Nominal Output Voltage	Marking	Package	Shipping†
NCP700MN180R2G	1.8 V	LZ	DFN6 2x2.2 Pb-Free	3000 / Tape & Reel
NCP700MN280R2G	2.8 V	LX		
NCP700MN300R2G	3.0 V	LY		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

6 PIN DFN, 2x2.2, 0.65P
CASE 506BA-01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
b	0.20	0.30
D	2.00 BSC	
D2	1.10	1.30
E	2.20 BSC	
E2	0.70	0.90
e	0.65 BSC	
K	0.20	---
L	0.25	0.35
L1	0.00	0.10

The products described herein (NCP700), may be covered by one or more U.S. patents.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada
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Japan Customer Focus Center
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ON Semiconductor Website: **www.onsemi.com**

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