ELPIDA

DATA SHEET

8GB DDR3 SDRAM SO-DIMM

EBJ81UG8BBU0 (1024M words × 64 bits, 2 Ranks)

Specifications

- Density: 8GB
- Organization
  - 1024M words × 64 bits, 2 ranks
- Mounting 16 pieces of 4G bits DDR3 SDRAM sealed in FBGA
- Package: 204-pin socket type small outline dual in-line memory module (SO-DIMM)
  - PCB height: 30.0mm
  - Lead pitch: 0.6mm
  - Lead-free (RoHS compliant) and Halogen-free
- Power supply: VDD = 1.5V ± 0.075V
- Data rate: 1600Mbps/1333Mbps (max.)
  Backward compatible to1066Mbps/800Mbps/667Mbps
- Eight internal banks for concurrent operation (components)
- Interface: SSTL_15
- Burst lengths (BL): 8 and 4 with Burst Chop (BC)
- /CAS Latency (CL): 5, 6, 7, 8, 9, 10, 11
- /CAS write latency (CWL): 5, 6, 7, 8
- Precharge: auto precharge option for each burst access
- Refresh: auto-refresh, self-refresh
- Refresh cycles
  - Average refresh period
    7.8µs at 0°C ≤ TC ≤ +85°C
    3.9µs at +85°C < TC ≤ +95°C
- Operating case temperature range
  - TC = 0°C to +95°C

Features

- Double-data-rate architecture: two data transfers per clock cycle
- The high-speed data transfer is realized by the 8 bits prefetch pipelined architecture
- Bi-directional differential data strobe (DQS and /DQS) is transmitted/received with data for capturing data at the receiver
- DQS is edge-aligned with data for READs; center-aligned with data for WRITEs
- Differential clock inputs (CK and /CK)
- DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- Data mask (DM) for write data
- Posted /CAS by programmable additive latency for better command and data bus efficiency
- On-Die-Termination (ODT) for better signal quality
  - Synchronous ODT
  - Dynamic ODT
  - Asynchronous ODT
- Multi Purpose Register (MPR) for pre-defined pattern read out
- ZQ calibration for DQ drive and ODT
- Programmable Partial Array Self-Refresh (PASR)
- /RESET pin for Power-up sequence and reset function
- SRT range:
  - Normal/extended
- Programmable Output driver impedance control

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Ordering Information

Part number	Data rate Mbps (max.)	Component JEDEC speed bin (CL-tRCD-tRP)	Package	Contact pad	Mounted devices
EBJ81UG8BBU0-GN-F	1600	DDR3-1600K (11-11-11)	204-pin SO-DIMM (lead-free and halogen-free)	Gold	EDJ4208BBBG-GN-F
EBJ81UG8BBU0-DJ-F	1333	DDR3-1333H (9-9-9)			EDJ4208BBBG-GN-F EDJ4208BBBG-DJ-F

Detailed Information

For detailed electrical specifications and further information, please refer to the component DDR3 SDRAM datasheet EDJ4204BBBG, EDJ4208BBBG (E1800E).

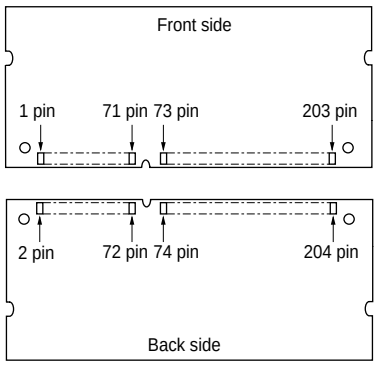
Pin Configurations

Front side		Back side		Front side		Back side		Front side		Back side	
Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	VREFDQ	2	VSS			KEY		143	DQ35	144	VSS
3	VSS	4	DQ4	73	CKE0	74	CKE1	145	VSS	146	DQ44
5	DQ0	6	DQ5	75	VDD	76	VDD	147	DQ40	148	DQ45
7	DQ1	8	VSS	77	NC	78	A15	149	DQ41	150	VSS
9	VSS	10	/DQS0	79	BA2	80	A14	151	VSS	152	/DQS5
11	DM0	12	DQS0	81	VDD	82	VDD	153	DM5	154	DQS5
13	VSS	14	VSS	83	A12(/BC)	84	A11	155	VSS	156	VSS
15	DQ2	16	DQ6	85	A9	86	A7	157	DQ42	158	DQ46
17	DQ3	18	DQ7	87	VDD	88	VDD	159	DQ43	160	DQ47
19	VSS	20	VSS	89	A8	90	A6	161	VSS	162	VSS
21	DQ8	22	DQ12	91	A5	92	A4	163	DQ48	164	DQ52
23	DQ9	24	DQ13	93	VDD	94	VDD	165	DQ49	166	DQ53
25	VSS	26	VSS	95	A3	96	A2	167	VSS	168	VSS
27	/DQS1	28	DM1	97	A1	98	A0	169	/DQS6	170	DM6
29	DQS1	30	/RESET	99	VDD	100	VDD	171	DQS6	172	VSS
31	VSS	32	VSS	101	CK0	102	CK1	173	VSS	174	DQ54
33	DQ10	34	DQ14	103	/CK0	104	/CK1	175	DQ50	176	DQ55
35	DQ11	36	DQ15	105	VDD	106	VDD	177	DQ51	178	VSS
37	VSS	38	VSS	107	A10(AP)	108	BA1	179	VSS	180	DQ60
39	DQ16	40	DQ20	109	BA0	110	/RAS	181	DQ56	182	DQ61
41	DQ17	42	DQ21	111	VDD	112	VDD	183	DQ57	184	VSS
43	VSS	44	VSS	113	/WE	114	/CS0	185	VSS	186	/DQS7
45	/DQS2	46	DM2	115	/CAS	116	ODT0	187	DM7	188	DQS7
47	DQS2	48	VSS	117	VDD	118	VDD	189	VSS	190	VSS
49	VSS	50	DQ22	119	A13	120	ODT1	191	DQ58	192	DQ62
51	DQ18	52	DQ23	121	/CS1	122	NC	193	DQ59	194	DQ63
53	DQ19	54	VSS	123	VDD	124	VDD	195	VSS	196	VSS
55	VSS	56	DQ28	125	NC	126	VREFCA	197	SA0	198	NC
57	DQ24	58	DQ29	127	VSS	128	VSS	199	VDDSPD	200	SDA
59	DQ25	60	VSS	129	DQ32	130	DQ36	201	SA1	202	SCL
61	VSS	62	/DQS3	131	DQ33	132	DQ37	203	VTT	204	VTT
63	DM3	64	DQS3	133	VSS	134	VSS				
65	VSS	66	VSS	135	/DQS4	136	DM4				
67	DQ26	68	DQ30	137	DQS4	138	VSS				
69	DQ27	70	DQ31	139	VSS	140	DQ38				
71	VSS	72	VSS	141	DQ34	142	DQ39				

Pin Description

Pin name	Function	
A0 to A15	Address input Row address Column address	 A0 to A15 A0 to A9
A10 (AP)	Auto precharge	
A12 (/BC)	Burst chop	
BA0, BA1, BA2	Bank select address	
/RAS	Row address strobe	
/CAS	Column address strobe	
/WE	Write enable	
/CS0, /CS1	Chip select	
CKE0, CKE1	Clock enable	
CK0, CK1	Clock input	
/CK0, /CK1	Differential clock input	
ODT0, ODT1	ODT control	
DQ0 to DQ63	Data input/output	
DQS0 to DQS7, /DQS0 to /DQS7	Input and output data strobe	
DM0 to DM7	Input mask	
SCL	Clock input for serial PD	
SDA	Data input/output for serial PD	
SA0, SA1	Address input for serial PD	
VDD*[1]	Power for internal circuit	
VDDSPD	Power for serial PD	
VREFCA	Reference voltage for CA	
VREFDQ	Reference voltage for DQ	
VSS	Ground	
VTT	I/O termination supply for SDRAM	
/RESET	Set DRAM to a known state	
NC	No connection	

Note: 1. The VDD and VDDQ pins are tied common to a single power-plane on these designs.

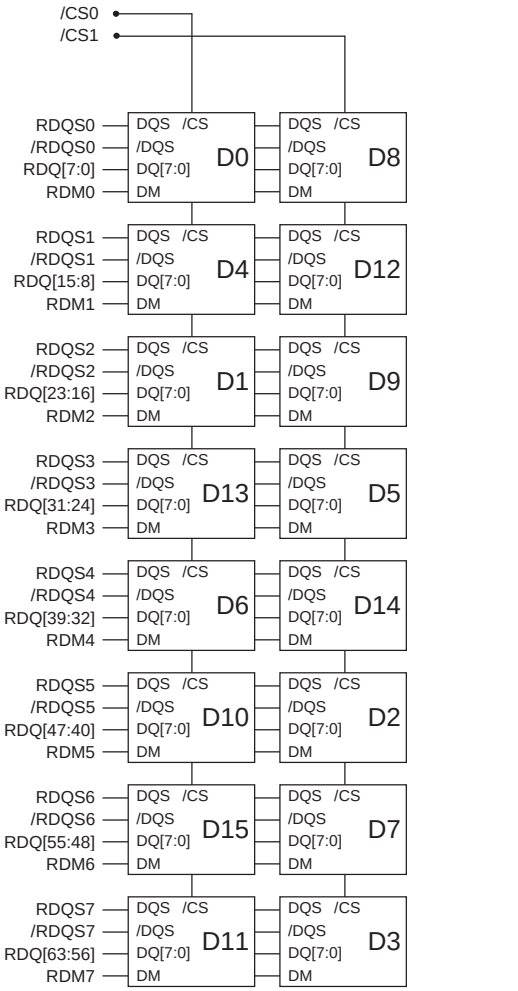


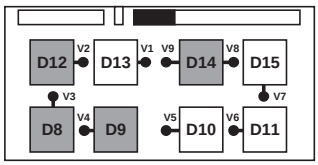
Serial PD Matrix

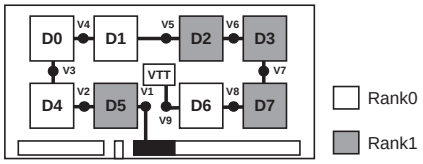
		-DJ		-GN	
Byte No.	Function described	Hex	Comments	Hex	Comments
0	Number of serial PD bytes written/ SPD device size/CRC coverage	92h	176/256/0-116	92h	176/256/0-116
1	SPD revision	10h	Rev.1.0	10h	Rev.1.0
2	Key byte/DRAM device type	0Bh	DDR3 SDRAM	0Bh	DDR3 SDRAM
3	Key byte/module type	03h	SO-DIMM	03h	SO-DIMM
4	SDRAM density and banks	04h	4G bits, 8 banks	04h	4G bits, 8 banks
5	SDRAM addressing	21h	16 rows, 10 columns	21h	16 rows, 10 columns
6	Module nominal voltage, VDD	00h	1.5V	00h	1.5V
7	Module organization	09h	2 ranks/×8 bits	09h	2 ranks/×8 bits
8	Module memory bus width	03h	64 bits/non-ECC	03h	64 bits/non-ECC
9	Fine timebase (FTB) dividend/divisor	52h	5/2	52h	5/2
10	Medium timebase (MTB) dividend	01h	1	01h	1
11	Medium timebase (MTB) divisor	08h	8	08h	8
12	SDRAM minimum cycle time (tCK (min.))	0Ch	1.5ns	0Ah	1.25ns
13	Reserved	00h	—	00h	—
14	SDRAM CAS latencies supported, LSB	7Eh	5, 6, 7, 8, 9, 10	FEh	5, 6, 7, 8, 9, 10, 11
15	SDRAM CAS latencies supported, MSB	00h	—	00h	—
16	SDRAM minimum CAS latencies time (tAA (min.))	69h	13.125ns	69h	13.125ns
17	SDRAM minimum write recovery time (tWR (min.))	78h	15ns	78h	15ns
18	SDRAM minimum /RAS to /CAS delay (tRCD (min.))	69h	13.125ns	69h	13.125ns
19	SDRAM minimum row active to row active delay (tRRD (min.))	30h	6ns	30h	6ns
20	SDRAM minimum row precharge time (tRP (min.))	69h	13.125ns	69h	13.125ns
21	SDRAM upper nibbles for tRAS and tRC	11h	—	11h	—
22	SDRAM minimum active to precharge time (tRAS (min.)), LSB	20h	36ns	18h	35ns
23	SDRAM minimum active to active /auto-refresh time (tRC (min.)), LSB	89h	49.125ns	81h	48.125ns
24	SDRAM minimum refresh recovery time delay (tRFC (min.)), LSB	20h	260ns	20h	260ns
25	SDRAM minimum refresh recovery time delay (tRFC (min.)), MSB	08h	260ns	08h	260ns
26	SDRAM minimum internal write to read command delay (tWTR (min.))	3Ch	7.5ns	3Ch	7.5ns
27	SDRAM minimum internal read to precharge command delay (tRTP (min.))	3Ch	7.5ns	3Ch	7.5ns
28	Upper nibble for tFAW	00h	30ns	00h	30ns
29	Minimum four activate window delay time (tFAW (min.))	F0h	30ns	F0h	30ns
30	SDRAM optional features	83h	DLL-off, RZQ/6, 7	83h	DLL-off, RZQ/6, 7
31	SDRAM thermal and refresh options	81h	PASR/2X refresh at +85ºC to +95ºC	81h	PASR/2X refresh at +85ºC to +95ºC
32	Module thermal sensor	00h	Not incorporated	00h	Not incorporated
33	SDRAM device type	00h	Standard	00h	Standard
34 to 59	Reserved	00h	—	00h	—

		-DJ		-GN	
Byte No.	Function described	Hex	Comments	Hex	Comments
60	Module nominal height	0Fh	29 < height ≤ 30mm	0Fh	29 < height ≤ 30mm
61	Module maximum thickness	11h	Dual sides	11h	Dual sides
62	Reference raw card used	65h	Raw Card F3	65h	Raw Card F3
63	Address mapping from edge connector to DRAM	00h	Standard	00h	Standard
64 to 116	Reserved	00h	—	00h	—
117	Module ID: manufacturer's JEDEC ID code, LSB	02h	Elpida Memory	02h	Elpida Memory
118	Module ID: manufacturer's JEDEC ID code, MSB	FEh	Elpida Memory	FEh	Elpida Memory
119	Module ID: manufacturing location	××	—	××	—
120	Module ID: manufacturing date	yy	Year code (BCD)	yy	Year code (BCD)
121	Module ID: manufacturing date	ww	Week code (BCD)	ww	Week code (BCD)
122 to 125	Module ID: module serial number	××	—	××	—
126	Cyclical redundancy code (CRC)	9Bh	—	4Eh	—
127	Cyclical redundancy code (CRC)	C8h	—	16h	—
128	Module part number	45h	E	45h	E
129	Module part number	42h	B	42h	B
130	Module part number	4Ah	J	4Ah	J
131	Module part number	38h	8	38h	8
132	Module part number	31h	1	31h	1
133	Module part number	55h	U	55h	U
134	Module part number	47h	G	47h	G
135	Module part number	38h	8	38h	8
136	Module part number	42h	B	42h	B
137	Module part number	42h	B	42h	B
138	Module part number	55h	U	55h	U
139	Module part number	30h	0	30h	0
140	Module part number	2Dh	—	2Dh	—
141	Module part number	44h	D	47h	G
142	Module part number	4Ah	J	4Eh	N
143	Module part number	2Dh	—	2Dh	—
144	Module part number	46h	F	46h	F
145	Module part number	20h	(Space)	20h	(Space)
146	Module revision code	30h	Initial	30h	Initial
147	Module revision code	20h	(Space)	20h	(Space)
148	SDRAM manufacturer's JEDEC ID code, LSB	02h	Elpida Memory	02h	Elpida Memory
149	SDRAM manufacturer's JEDEC ID code, MSB	FEh	Elpida Memory	FEh	Elpida Memory
150 to 175	Manufacturer's specific data				
176 to 255	Open for customer use	00h	—	00h	—

Block Diagram

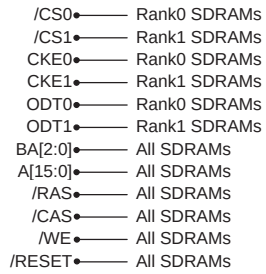


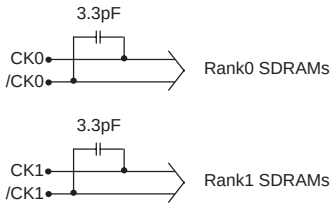


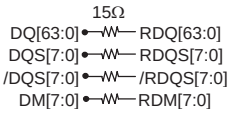


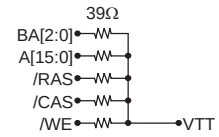
Address, command and control line

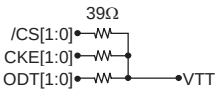
Note :
1. DQ wiring may be changed within a byte.

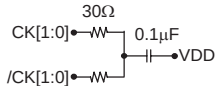


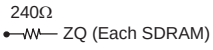


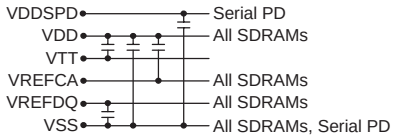


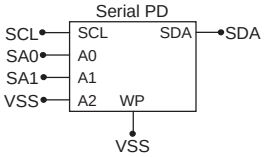












Electrical Specifications

- All voltages are referenced to VSS (GND).

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Notes
Power supply voltage	VDD	–0.4 to +1.975	V	1, 3, 4
Input voltage	VIN	–0.4 to +1.975	V	1, 4
Output voltage	VOUT	–0.4 to +1.975	V	1, 4
Reference voltage	VREFCA	–0.4 to 0.6 × VDD	V	3, 4
Reference voltage for DQ	VREFDQ	–0.4 to 0.6 × VDDQ	V	3, 4
Storage temperature	Tstg	–55 to +100	°C	1, 2, 4
Power dissipation	PD	8	W	
Short circuit output current	IOUT	50	mA	1, 4

Notes: 1. Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. Storage temperature is the case surface temperature on the center/top side of the DRAM.
3. VDD and VDDQ must be within 300mV of each other at all times; and VREF must be not greater than 0.6 × VDDQ, When VDD and VDDQ are less than 500mV; VREF may be equal to or less than 300mV.
4. DDR3 SDRAM component specification.

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Operating Temperature Condition

Parameter	Symbol	Rating	Unit	Notes
Operating case temperature	TC	0 to +95	°C	1, 2, 3

Notes: 1. Operating temperature is the case surface temperature on the center/top side of the DRAM.

2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0°C to +85°C under all operating conditions.
3. Some applications require operation of the DRAM in the Extended Temperature Range between +85°C and +95°C case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:
   a) Refresh commands must be doubled in frequency, therefore reducing the refresh interval tREFI to 3.9µs. (This double refresh requirement may not apply for some devices.)
   b) If Self-refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 bit [A6, A7] = [0, 1]) or enable the optional Auto Self-Refresh mode (MR2 bit [A6, A7] = [1, 0]).

Recommended DC Operating Conditions (TC = 0°C to +85°C)

Parameter	Symbol	min.	typ.	max.	Unit	Notes
Supply voltage	VDD, VDDQ	1.425	1.5	1.575	V	1, 2, 3
	VSS	0	0	0	V	1
	VDDSPD	3.0	3.3	3.6	V	
Input reference voltage for address, command inputs	VREFCA (DC)	0.49 × VDD	—	0.51 × VDD	V	1, 4, 5
Input reference voltage for DQ, DM inputs	VREFDQ (DC)	0.49 × VDD	—	0.51 × VDD	V	1, 4, 5

Notes: 1. DDR3 SDRAM component specification.

2. Under all conditions VDDQ must be less than or equal to VDD.
3. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
4. The AC peak noise on VREF may not allow VREF to deviate from VREF(DC) by more than ±1% VDD (for reference: approx. ±15 mV).
5. For reference: approx. VDD/2 ±15 mV.

DC Characteristics 1 (TC = 0°C to +85°C, VDD = 1.5V ± 0.075V, VSS = 0V)

Data rate (Mbps)		1600	1333		
Parameter	Symbol	max.	max.	Unit	Notes
Operating current (ACT-PRE) (Another rank is in IDD2P1)	IDD0	800	760	mA	
Operating current (ACT-PRE) (Another rank is in IDD3N)	IDD0	960	920	mA	
Operating current (ACT-READ-PRE) (Another rank is in IDD2P1)	IDD1	920	880	mA	
Operating current (ACT-READ-PRE) (Another rank is in IDD3N)	IDD1	1080	1040	mA	
Precharge power-down standby current	IDD2P1	560	560	mA	Fast PD Exit
	IDD2P0	320	320	mA	Slow PD Exit
Precharge standby current	IDD2N	720	720	mA	
Precharge standby ODT current	IDD2NT	720	720	mA	
Precharge quiet standby current	IDD2Q	720	720	mA	
Active power-down current (Always fast exit)	IDD3P	624	592	mA	
Active standby current	IDD3N	880	880	mA	
Operating current (Burst read operating) (Another rank is in IDD2P1)	IDD4R	1280	1160	mA	
Operating current (Burst read operating) (Another rank is in IDD3N)	IDD4R	1440	1320	mA	
Operating current (Burst write operating) (Another rank is in IDD2P1)	IDD4W	1320	1200	mA	
Operating current (Burst write operating) (Another rank is in IDD3N)	IDD4W	1480	1360	mA	
Burst refresh current (Another rank is in IDD2P1)	IDD5B	2280	2280	mA	
Burst refresh current (Another rank is in IDD3N)	IDD5B	2440	2440	mA	
All bank interleave read current (Another rank is in IDD2P1)	IDD7	1960	1880	mA	
All bank interleave read current (Another rank is in IDD3N)	IDD7	2120	2040	mA	
RESET low current	IDD8	272	272	mA	

Self-Refresh Current (TC = 0°C to +85°C, VDD = 1.5V ± 0.075V)

Parameter	Symbol	max.	Unit	Notes
Self-refresh current normal temperature range	IDD6	352	mA	
Self-refresh current extended temperature range	IDD6ET	400	mA	
Auto self-refresh current (optional)	IDD6TC	—	mA	

Timings used for IDD and IDDQ Measurement-Loop Patterns

	DDR3-1600	DDR3-1333	
Parameter	11-11-11	9-9-9	Unit
CL	11	9	nCK
tCK min.	1.25	1.5	ns
nRCD min.	11	9	nCK
nRC min.	39	33	nCK
nRAS min.	28	24	nCK
nRP min.	11	9	nCK
nFAW	24	20	nCK
nRRD	5	4	nCK
nRFC	208	174	nCK

Pin Functions

CK, /CK (input pins)

CK and /CK are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of /CK. Output (read) data is referenced to the crossings of CK and /CK (both directions of crossing).

/CS (input pins)

All commands are masked when /CS is registered high. /CS provides for external rank selection on systems with multiple ranks. /CS is considered part of the command code.

/RAS, /CAS, and /WE (input pins)

/RAS, /CAS and /WE (along with /CS) define the command being entered.

A0 to A15 (input pins)

Provided the row address for active commands and the column address for read/write commands to select one location out of the memory array in the respective bank. (A10(AP) and A12(/BC) have additional functions, see below) The address inputs also provide the op-code during mode register set commands.

[Address Pins Table]

Address (A0 to A15)		
Row address (RA)	Column address (CA)	Notes
AX0 to AX15	AY0 to AY9	

A10(AP) (input pin)

A10 is sampled during read/write commands to determine whether auto-precharge should be performed to the accessed bank after the read/write operation. (high: auto-precharge; low: no auto-precharge)

A10 is sampled during a precharge command to determine whether the precharge applies to one bank (A10 = low) or all banks (A10 = high). If only one bank is to be precharged, the bank is selected by bank addresses (BA).

A12 (/BC) (input pin)

A12 is sampled during read and write commands to determine if burst chop (on-the-fly) will be performed.

(A12 = high: no burst chop, A12 = low: burst chopped.)

BA0 to BA2 (input pins)

BA0, BA1 and BA2 define to which bank an active, read, write or precharge command is being applied. BA0 and BA1 also determine if a mode register is to be accessed during a MRS cycle.

[Bank Select Signal Table]

	BA0	BA1	BA2
Bank 0	L	L	L
Bank 1	H	L	L
Bank 2	L	H	L
Bank 3	H	H	L
Bank 4	L	L	H
Bank 5	H	L	H
Bank 6	L	H	H
Bank 7	H	H	H

Remark: H: VIH. L: VIL.

CKE (input pins)

CKE high activates, and CKE low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE low provides precharge power-down and self-refresh operation (all banks idle), or active power-down (row active in any bank). CKE is asynchronous for self-refresh exit. After VREF has become stable during the power-on and initialization sequence, it must be maintained for proper operation of the CKE receiver. For proper self-refresh entry and exit, VREF must be maintained to this input. CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, /CK, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during self-refresh.

DQ (input and output pins)

Bi-directional data bus.

DQS and /DQS (input and output pins)

Output with read data, input with write data. Edge-aligned with read data, centered in write data.
The data strobe DQS is paired with differential signals /DQS to provide differential pair signaling to the system during READs and WRITEs.

ODT (input pins)

ODT (registered high) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is only applied to each DQ, DQS, /DQS, DM. The ODT pin will be ignored if the mode register (MR1) is programmed to disable ODT.

DM (input pins)

DM is the reference signal of the data input mask function. DMs are sampled at the cross point of DQS and /DQS.

VDD (power supply pins)

1.5V is applied. (VDD is for the internal circuit.)

VDDSPD (power supply pin)

3.3V is applied (For serial PD).

VSS (power supply pins)

Ground is connected.

VTT (power supply pins)

I/O termination supply for SDRAM.

VREFDQ (power supply pin)

Reference voltage for DQ.

VREFCA (power supply pin)

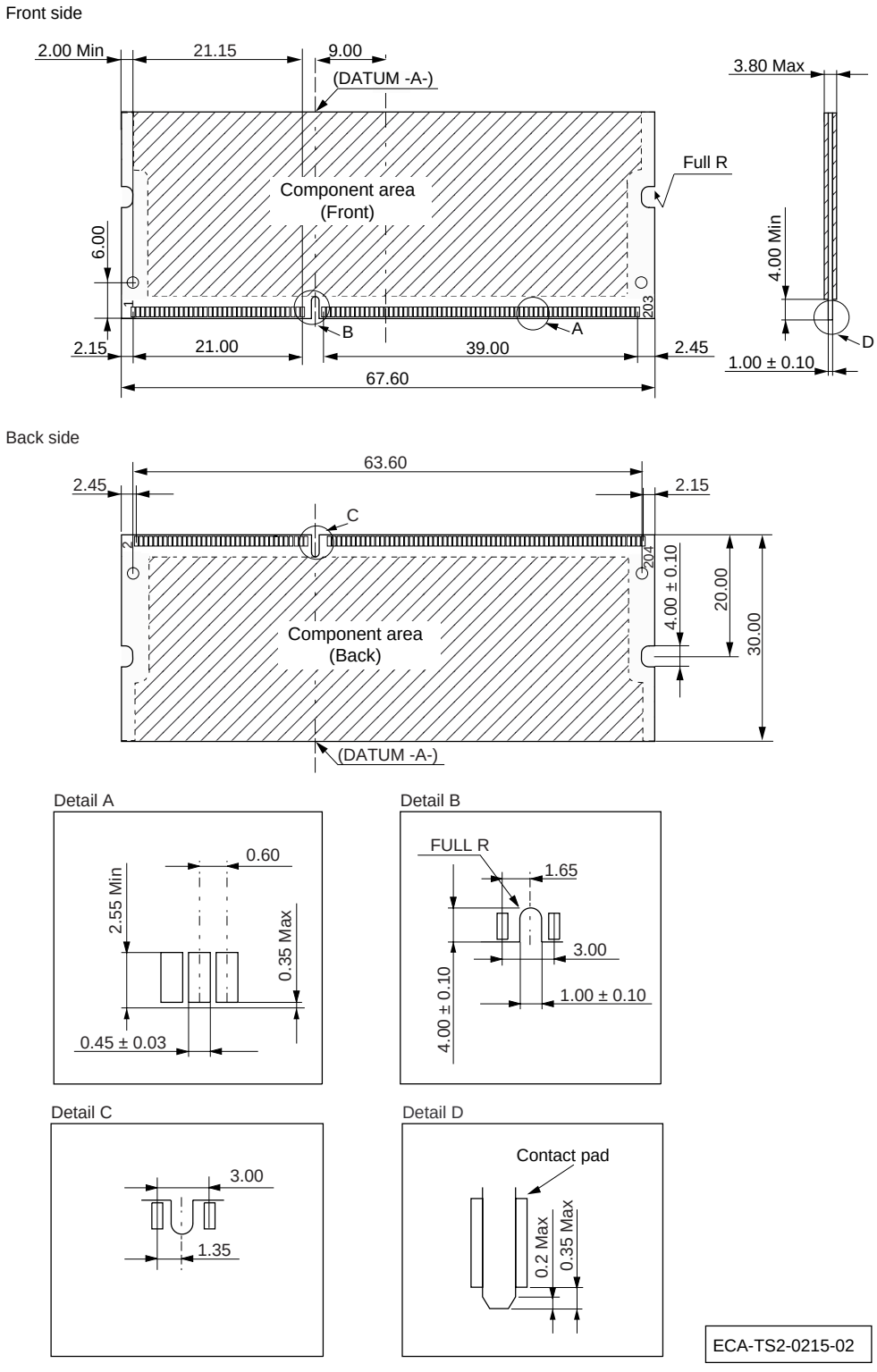
Reference voltage for CA.

/RESET (input pin)

/RESET is negative active signal (active low) and is referred to VSS.

Physical Outline

Unit: mm



Note: 1. Tolerances on all dimensions ±0.15 unless otherwise specified.

CAUTION FOR HANDLING MEMORY MODULES

When handling or inserting memory modules, be sure not to touch any components on the modules, such as the memory ICs, chip capacitors and chip resistors. It is necessary to avoid undue mechanical stress on these components to prevent damaging them.
In particular, do not push module cover or drop the modules in order to protect from mechanical defects, which would be electrical defects.

When re-packing memory modules, be sure the modules are not touching each other.
Modules in contact with other modules may cause excessive mechanical stress, which may damage the modules.

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NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR MOS DEVICES

Exposing the MOS devices to a strong electric field can cause destruction of the gate oxide and ultimately degrade the MOS devices operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it, when once it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. MOS devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. MOS devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor MOS devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS DEVICES

No connection for CMOS devices input pins can be a cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. The unused pins must be handled in accordance with the related specifications.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Power-on does not necessarily define initial status of MOS devices. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the MOS devices with reset function have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. MOS devices are not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for MOS devices having reset function.

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2) Usage in exposure to direct sunlight or the outdoors, or in dusty places.
3) Usage involving exposure to significant amounts of corrosive gas, including sea air, CL_2, H_2S, NH_3, SO_2, and NO_X.
4) Usage in environments with static electricity, or strong electromagnetic waves or radiation.
5) Usage in places where dew forms.
6) Usage in environments with mechanical vibration, impact, or stress.
7) Usage near heating elements, igniters, or flammable items.

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