REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with NOR 5962-R344-97.	97-06-12	K. A. Cottongim
B	Correct table II.	98-05-14	K. A. Cottongim

REV																				
SHEET																				
REV	B	B	B	B	B	B														
SHEET	15	16	17	18	19	20														

REV STATUS OF SHEETS	REV	B	B	B	B	B	B	B	B	B	B	B	B	B
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Gary Zahn

CHECKED BY
Michael C. Jones

APPROVED BY
Kendall A. Cottongim

DRAWING APPROVAL DATE
97-02-10

REVISION LEVEL
B

DEFENSE SUPPLY CENTER COLUMBUS
P. O. BOX 3990
COLUMBUS, OHIO 43216-5000

MICROCIRCUIT, HYBRID, LINEAR, MIL-STD-1553, BC/RTU/MT, MULTIPLEXED TERMINAL

SIZE	CAGE CODE	
A	67268	5962-96887

SHEET 1 OF 20

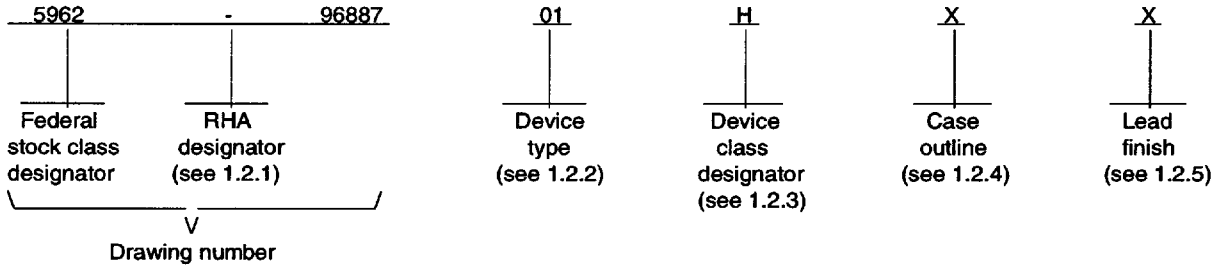
DSCC FORM 2233
APR 97

5962-E308-98

1. SCOPE

1.1 Scope. This drawing documents five product assurance classes, class D (lowest reliability), class E, (exceptions), class G (lowest high reliability), class H (high reliability), and class K, (highest reliability) and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of radiation hardness assurance levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. Device classes H and K RHA marked devices shall meet the MIL-PRF-38534 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	BU61582X1	MIL-STD-1553, BC/RT/MT, 32K RAM, +5/-15 V transciever
02	BU61582X2	MIL-STD-1553, BC/RT/MT, 32K RAM, +5/-12 V transciever
03	BU61583X1	MIL-STD-1553, BC/RT/MT, 32K RAM, +5/-15 V transciever, RT address latch
04	BU61583X2	MIL-STD-1553, BC/RT/MT, 32K RAM, +5/-12 V transciever, RT address latch
05	BU61582X0	MIL-STD-1553, BC/RT/MT, 32K RAM, transcieverless
06	BU61583X0	MIL-STD-1553, BC/RT/MT, 32K RAM, transcieverless, RT latch

1.2.3 Device class designator. This device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device performance documentation
D, E, G, H, or K	Certification and qualification to MIL-PRF-38534

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	70	Dual-in-line
Y	See figure 1	70	Flat package
Z	See figure 1	70	Gull wing

1.2.5 Lead finish. The lead finish shall be as specified in MIL-PRF-38534.

1.3 Absolute maximum ratings. 1/

Positive supply voltage range (+5VA, +5VB)	-0.3 V dc to +7.0 V dc
Negative supply voltage range (-VA, -VB):	
Device types 01, 02, 03, and 04	+0.3 V dc to -18 V dc
Logic supply voltage range (+5V logic)	-0.3 V dc to +7.0 V dc
Power dissipation (P_D): 1/ 2/ 3/	
Device types 01and 03	3.77 W
Device types 02 and 04	3.71 W
Device types 05 and 06	0.75 W
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction to case (θ_{JC})	6.99°C/W 2/

1.4 Recommended operating conditions.

Positive supply voltage range (+5VA, +5VB)	+4.5 V dc to +5.5 V dc
Logic supply voltage range (+5V logic)	+4.5 V dc to +5.5 V dc
Negative supply voltage range (-VA, -VB):	
Device types 01 and 03	-14.25 V dc to -15.75 V dc
Device types 02 and 04	-11.40 V dc to -12.60 V dc
Minimum logic high input voltage (V_{IH})	3.9 V dc
Maximum logic low input voltage (V_{IL})	1.3 V dc
Operating frequency (F_{OP})	12.0 MHz or 16 MHz
Case operating temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbook. The following specification, standards, and handbook form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38534 - Hybrid Microcircuits, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

HANDBOOK

DEPARTMENT OF DEFENSE

MIL-HDBK-780 - Standard Microcircuit Drawings.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability. Applies up to T_C = +125°C.
2/ Hottest die.
3/ Assumes 100 percent transmitter duty cycle on one channel and 0 percent duty cycle on the other channel.

(Unless otherwise indicated, copies of the specification, standards, and handbook are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item performance requirements for device classes D, E, G, H, and K shall be in accordance with MIL-PRF-38534. Compliance with MIL-PRF-38534 may include the performance of all tests herein or as designated in the device manufacturer's Quality Management (QM) plan or as designated for the applicable device class. Therefore, the tests and inspections herein may not be performed for the applicable device class (see MIL-PRF-38534). Futhermore, the manufacturers may take exceptions or use alternate methods to the tests and inspections herein and not perform them. However, the performance requirements as defined in MIL-PRF-38534 shall be met for the appilcable device class.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38534 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full specified operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking of Device(s). Marking of device(s) shall be in accordance with MIL-PRF-38534. The device shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's vendor similar PIN may also be marked as listed in QML-38534.

3.6 Data. In addition to the general performance requirements of MIL-PRF-38534, the manufacturer of the device described herein shall maintain the electrical test data (variables format) from the initial quality conformance inspection group A lot sample, for each device type listed herein. Also, the data should include a summary of all parameters manually tested, and for those which, if any, are guaranteed. This data shall be maintained under document revision level control by the manufacturer and be made available to the preparing activity (DSCC-VA) upon request.

3.7 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to supply to this drawing. The certificate of compliance (original copy) submitted to DSCC-VA shall affirm that the manufacturer's product meets the performance requirements of MIL-PRF-38534 and herein.

3.8 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38534 shall be provided with each lot of microcircuits delivered to this drawing.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38534 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
+5 Volt supply current, idle 1/	I_{CC1}	+5 V logic = +5.5 V, +5VA = +5VB = +5.5 V	1, 2, 3	01-04	5	190	mA
				05,06	5	150	
+5 Volt supply current, channel A = 25% duty cycle, channel B = idle 1/	I_{CC2}		1, 2, 3	01-04	5	190	mA
				05,06	5	150	
+5 Volt supply current, channel A = idle, channel B = 25% duty cycle 1/	I_{CC3}		1, 2, 3	01-04	5	190	mA
				05,06	5	150	
Negative supply 2/ current	I_{EE1}		1, 2, 3	01-04	5	60	mA
Negative supply current, channel A = 25% duty cycle, channel B = idle 2/	I_{EE2}		1, 2, 3	01,03	25	108	mA
				02,04	25	120	
Negative supply current, channel B = 25% duty cycle, channel A = idle 2/	I_{EE3}		1, 2, 3	01,03	25	108	mA
				02,04	25	120	
Low level input current 3/	I_{IL1}	+5V logic = +5.5 V, +5VA = +5VB = +5.5V, V_{IN} = 0 V	1, 2, 3	All	-550	-60	µA
Low level input current 4/	I_{IL2}				-10	+10	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High level input 3/ current	I_{IH1}	+5V logic = +5.5 V, +5VA = +5VB = +5.5V, V_{IN} = 2.4 V	1, 2, 3	All	-150	-25	µA
High level input 4/ current	I_{IH2}				-10	10	
Output voltage low 5/	V_{OL1}	+5V logic = +5.5 V, +5VA = +5VB = +5.5V, I_{OL} = -6.4 mA	1, 2, 3	All		0.5	V
Output voltage high 5/	V_{OH1}	+5V logic = +5.5 V, +5VA = +5VB = +5.5V, I_{OL} = 6.4 mA	1, 2, 3	All	4.0		V
Functional tests		+5V logic = +5.0 V, +5VA = +5VB = +5.0V, see 4.3.1c	7, 8	All			Pass/ fail
Receiver threshold	V_{TH}	+5V logic = +5.0 V, +5VA = +5VB = +5.0V, transformer coupled into a 70 Ω resistive load	4, 5, 6	All	500	700	mVp-p
Transmitter differential output voltage	V_O	+5V logic = +5.0 V, +5VA = +5VB = +5.0V, transformer coupled into a 70 Ω resistive load	4, 5, 6	All	18	27	Vp-p
Transmitter output rise time	t_R			All	100	300	ns
Transmitter output fall time	t_F			All	100	300	ns
Transmitter output offset voltage 6/	V_{OS}			All	-250	+250	mVp-p

1/ Measured at the following pins: Pins 38, 54, and 68.
2/ Measured at the following pins: Pins 36 and 70.
3/ Measured at the following pins: Pins 8-17, 20-25, 29-32, 39-44, 46-53, and 55-62.
4/ Measured at the following pins: Pins 3-7, 19, 26, 27, 33, 63, and 64.
5/ Measured at the following pins: Pins 8-17, 20-25, 28-32, 45-53, 55-62, and 65-67.
6/ Parameter shall be tested as part of initial characterization of these devices and after design and process changes. Parameter shal be guaranteed to the limits specified in table I for all lots not specifically tested.

Case outline X.

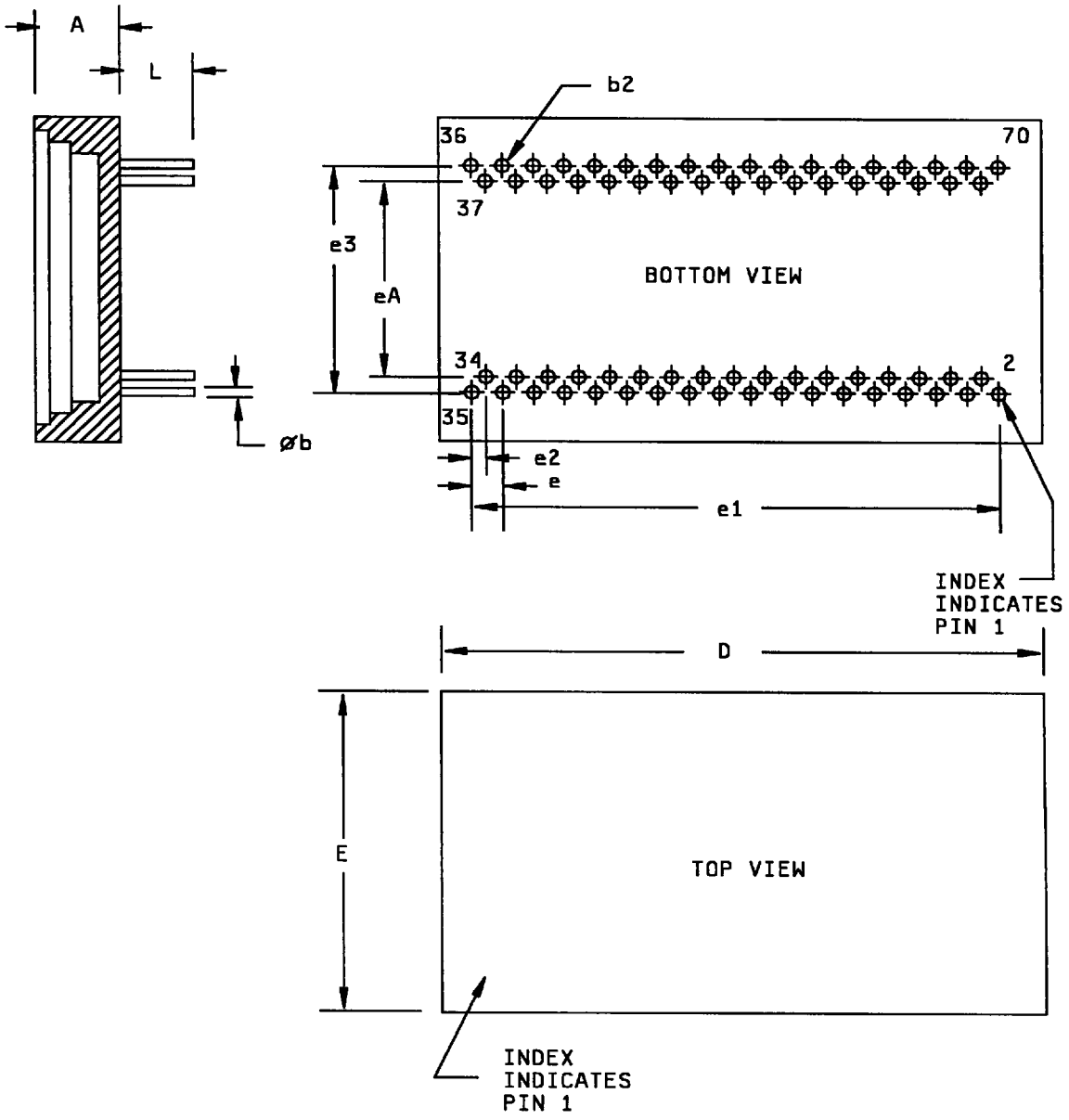


FIGURE 1. Case outline(s).

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-96887
		REVISION LEVEL B	SHEET 7

DSCC FORM 2234
APR 97

9004708 0039041 T44

Symbol	Millimeter		Inches	
	Minimum	Maximum	Minimum	Maximun
A	---	5.46	---	0.215
øb	0.41	0.51	0.016	0.020
b2	1.65	1.91	0.065	0.075
D	---	48.26	---	1.900
e	2.41	2.67	0.095	0.105
eA	10.03	10.29	0.395	0.405
e1	43.05	43.31	1.695	1.705
e2	1.14	1.40	0.045	0.055
e3	15.11	15.37	0.595	0.605
E	---	25.40	---	1.000
L	4.32	4.83	0.170	0.190

NOTES:
1. The U.S. government preferred system of measurement is the metric SI. This case outline was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Pin numbers are for reference only.

FIGURE 1. Case outline(s) - Continued.

Case outline Y.

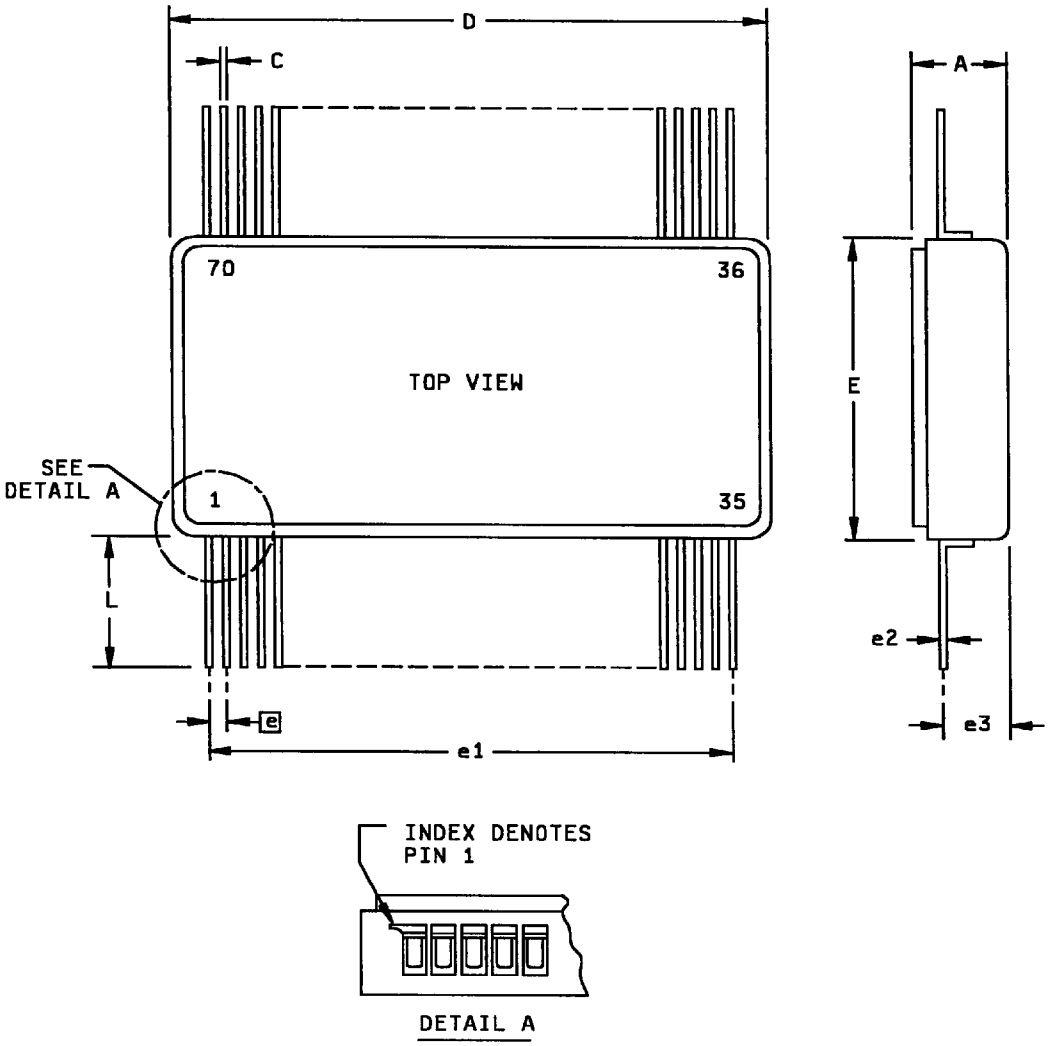


FIGURE 1. Case outline(s) - Continued.

Symbol	Millimeter		Inches	
	Minimum	Maximum	Minimum	Maximum
A	---	5.46	---	0.215
C	0.41	0.51	0 .016	0.020
D	---	48.26	---	1.900
e	1.14	1.40	0.045	0.055
e1	43.05	43.31	1.695	1.705
e2	0.20	0.30	0.008	0.012
e3	1.52	2.03	0.060	0.080
E	---	25.40	---	1.000
L	10.16	---	0.400	---

NOTES:
1. The U.S. government preferred system of measurement is the metric SI. This case outline was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Pin numbers are for reference only.

FIGURE 1. Case outlines - Continued.

Case outline Z.

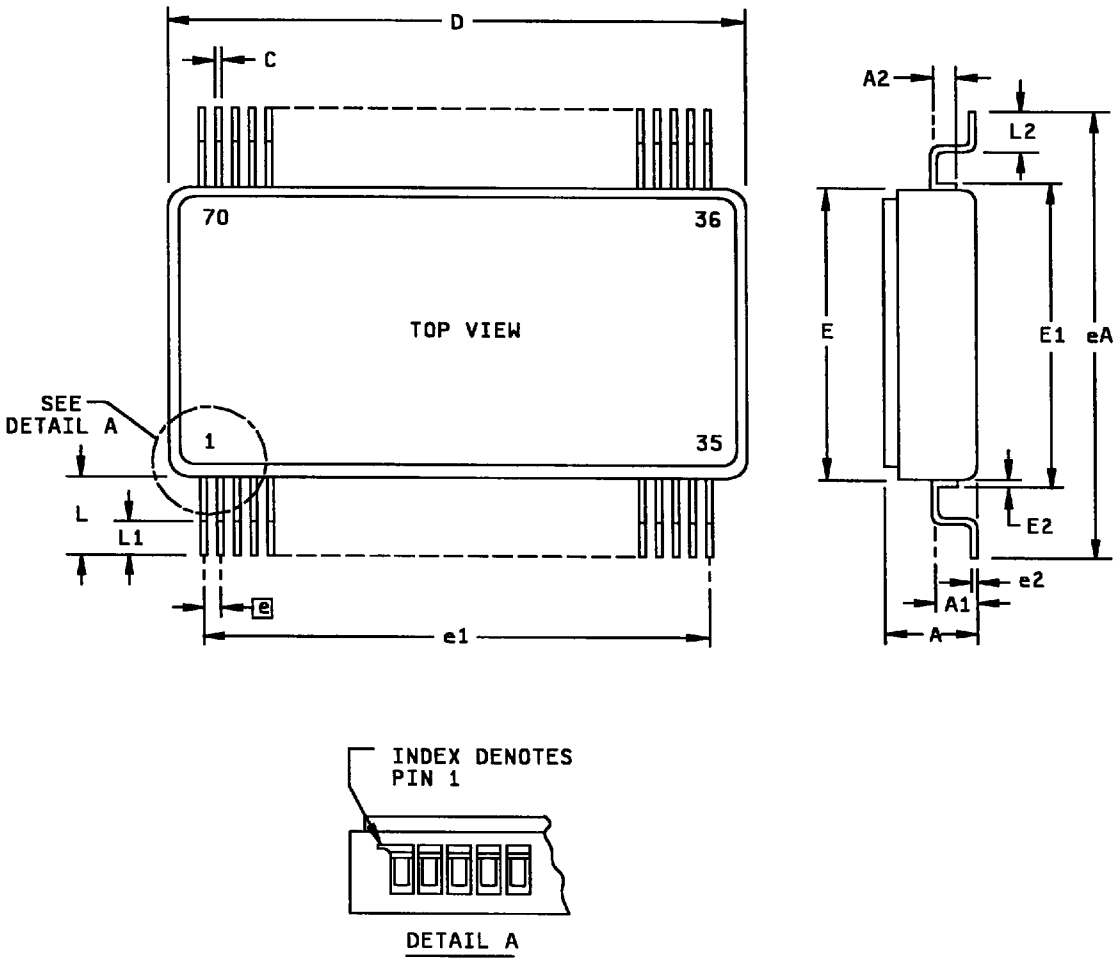


FIGURE 1. Case outline(s) - Continued.

Case outline Z - Continued.

Symbol	Millimeter		Inches	
	Minimum	Maximum	Minimum	Maximum
A		5.46		0.215
A1	1.65 REF		0.065 REF	
A2	1.02 TYP		0.040 TYP	
C	0.41	0.51	0.016	0.020
D		48.26		1.900
e	1.14	1.40	0.045	0.055
e1	43.05	43.31	1.695	1.705
e2	0.20	0.30	0.008	0.012
eA	34.54	35.56	1.360	1.400
E		25.40		1.000
E1		26.01		1.024
E2		0.30		0.012
L	4.57	4.83	0.180	0.190
L1	2.03		0.080	
L2	1.27		0.050	

NOTES:
1. The U.S. government preferred system of measurement is the metric SI. This case outline was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Pin numbers are for reference only.

FIGURE 1. Case outlines - Continued.

Device types	All		
Case outlines	X, Y, Z		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	TX/RX-A 1/	36	-VB 1/ 2/
2	TX/RX-A 1/	37	GNDB 1/
3	SELECT	38	+5VB 1/
4	STRBD	39	RTAD0
5	MEM/REG	40	RTAD1
6	RD/WR	41	RTAD2
7	MSTCLR	42	RTAD3
8	A15	43	RTAD4
9	A14	44	RTADP
10	A13	45	INCMD
11	A12	46	D00
12	A11	47	D01
13	A10	48	D02
14	A09	49	D03
15	A08	50	D04
16	A07	51	D05
17	A06	52	D06
18	LOGIC GND	53	D07
19	CLOCK IN	54	+5V LOGIC
20	A05	55	D08
21	A04	56	D09
22	A03	57	D10
23	A02	58	D11
24	A01	59	D12
25	A00	60	D13
26	DTGRT/MSB/LSB	61	D14
27	SSFLAG/EXT TRIG	62	D15
28	MEMENA OUT	63	TAG CLK
29	MEMOE/ADDR LAT	64	TRANSPARENT/BUFFERED
30	MEMWR/ZEROWAIT	65	INT
31	DTREQ/16/8	66	READYD
32	DTACK/POLARITY SEL	67	IOEN
33	MEMENA IN/TRIGGER SEL	68	+5VA 1/
34	TX/RX-B 1/	69	GNDA 1/
35	TX/RX-B 1/	70	-VA 1/ 2/

NOTES:

1/ For device types 05 and 06; pin 1 is RXA, pin 2 is $\overline{\text{RXA}}$, pin 34 is $\overline{\text{RXB}}$, pin 35 is RXB, pin 36 is TXINHB, pin 37 is TXB, pin 38 is TXB, pin 68 is TXINHA, pin 69 is TXA, and pin 70 is TXA.

2/ For device types 01 and 03; pin 36 and pin 70 are -15 V.
For device types 02 and 04; pin 36 and pin 70 are -12 V.

FIGURE 2. Terminal connections

TABLE II. Electrical test requirements.

MIL-PRF-38534 test requirements	Subgroups (in accordance with MIL-PRF-38534, group A test table)
Interim electrical parameters	1,2,3,4,5,6,7,8
Final electrical parameters	1*,2,3,4,5,6,7,8
Group A test requirements	1,2,3,4,5,6,7,8
Group C end-point electrical parameters	1,2,3,4,5,6,7,8
MIL-STD-883, group E end-point electrical parameters for RHA devices	Subgroups** (in accordance with method 5005, group A test table)

* PDA applies to subgroup 1.
** When applicable to this standard microcircuit drawing, the subgroups shall be defined.

4.2 Screening. Screening shall be in accordance with MIL-PRF-38534. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A as specified in accordance with table I of method 1015 of MIL-STD-883.

(3) Burn-in test shall be for 320 hours.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. 100% Nondestructive bond pull test.

4.3 Conformance and periodic inspections. Conformance inspection (CI) and periodic inspection (PI) shall be in accordance with MIL-PRF-38534 and as specified herein.

4.3.1 Group A inspection (CI). Group A inspection shall be in accordance with MIL-PRF-38534 and as follows:

a. Tests shall be as specified in table II herein.

b. Subgroups 9, 10, and 11 shall be omitted.

c. Subgroups 7 and 8 shall consist of verifying the functionality of the device. It forms a part of the vendors test tape and shall be maintained and available from the aprroved source of supply.

4.3.2 Group B inspection (PI). Group B inspection shall be in accordance with MIL-PRF-38534.

4.3.3 Group C inspection (PI). Group C inspection shall be in accordance with MIL-PRF-38534 and as follows:

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A as specified in accordance with table I of method 1005 of MIL-STD-883.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.3.4 Group D inspection (PI). Group D inspection shall be in accordance with MIL-PRF-38534.

4.3.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels shall be M, D, R, and H. RHA quality conformance inspection sample tests shall be performed at the RHA level specified in the acquisition document.

a. RHA tests for levels M, D, R, and H shall be performed through each level to determine at what levels the devices meet the RHA requirements. These RHA tests shall be performed for initial qualification and after design or process changes which may affect the RHA performance of the device.

b. End-point electrical parameters shall be as specified in table II herein.

c. Prior to total dose irradiation, each selected sample shall be assembled in its qualified package. It shall pass the specified group A electrical parameters in table I for subgroups specified in table II herein.

d. The devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38534 for RHA level being tested, and meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25° C ±5 percent, after exposure.

e. Prior to and during total dose irradiation testing, the devices shall be biased to establish a worst case condition as specified in the radiation exposure circuit.

f. For device classes H and K, subgroups 1 and 2 in table V, method 5005 of MIL-STD-883 shall be tested as appropriate for device construction.

g. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38534.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-7603.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0512.

6.6 Sources of supply. Sources of supply are listed in QML-38534. The vendors listed in QML-38534 have submitted a certificate of compliance (see 3.7 herein) to DSCC-VA and have agreed to this drawing.

TABLE III. Pin functions.

Terminal symbol	I/O	Description
D00	I/O	Data bus bit 0 (LSB).
D02	I/O	Data bus bit 2.
D04	I/O	Data bus bit 4.
D06	I/O	Data bus bit 6.
D08	I/O	Data bus bit 8.
D10	I/O	Data bus bit 10.
D12	I/O	Data bus bit 12.
D14	I/O	Data bus bit 14.
RTAD1	I	Remote terminal address bit 1.
RTAD0	I	Remote terminal address bit 0 (LSB).
RTAD4	I	Remote terminal address bit 4 (MSB).
+5 V logic	I	+5 V supply input for digital logic section.
TAG CLK	I	External Time Tag Clock Input, for BC/RT modes.
-VB	I	Input power supply connection for the B channel transceiver. -15 V for device types 01and 03. -12 V for device types 02 and 04.
GNDB	-	Ground B. Power supply return connection for the B channel transceiver.
TX/RX-B	I/O	Transmit/receive transceiver-B. Input/output to the coupling transformer that connects to the B channel of the 1553 bus.
LOGIC GND	I/O	Logic ground. Power supply return for the digital logic section.
A01	I/O	Address bit 1.
A03	I/O	Address bit 3.
A05	I/O	Address bit 5.
A07	I/O	Address bit 7.
A09	I/O	Address bit 9.
A11	I/O	Address bit 11.
A13	I/O	Address bit 13.
A15	I/O	Address bit 15.
$\overline{\text{MEMOE}}$/ADDR LAT	I/O	Memory Output Enable/Address Latch. In transparent mode, used to enable data outputs for external RAM. In buffered mode, input used to configure the internal address buffers.

TABLE III. Pin functions - Continued.

Terminal symbol	I/O	Description
$\overline{\text{MEMENA-OUT}}$	O	Memory enable out. Logic 0 output enables external RAM. Used with $\overline{\text{MEMOE}}$ to read data or with MEMWR to write data into external RAM.
CLOCK IN	I	Clock input. 16 MHz TTL clock.
MEM/$\overline{\text{REG}}$	I	Memory/register. Input from CPU to select memory or register data transfer.
$\overline{\text{STRBD}}$	I	Strobe data. Used in conjunction with $\overline{\text{SELECT}}$ to initiate a data transfer cycle to/from CPU.
TRANSPARENT/ BUFFERED	I	Used to select between the transparent and buffered modes for the host processor interface.
D11	I/O	Data bus bit 11.
D13	I/O	Data bus bit 13.
D15	I/O	Data bus bit 15 (MSB).
RTAD3	I	Remote terminal address bit 3.
RTAD2	I	Remote terminal address bit 2.
RTADP	I	Remote terminal address parity input.
RD/$\overline{\text{WR}}$	I	Read/write. Input from the CPU which defines the data bustransfer as a read or write operation.
GNDA	-	Ground A. Power supply return connection for the A channel transceiver.
-VA	I	Input power supply connection for the A channel transceiver. -15 V for device types 01 and 03. -12 V for device types 02 and 04.
TX/RX-A	I/O	Transmit receive transceiver-A. Input/output to the coupling transformer that connects to the A channel of the 1553 bus.
D01	I/O	Data bus bit 1.
D03	I/O	Data bus bit 3.
D05	I/O	Data bus bit 5.
D07	I/O	Data bus bit 7.
D09	I/O	Data bus bit 9.
+5 VB	I	+5 V power supply connection for the B channel transceiver.
$\overline{\text{TX/RX-B}}$	I/O	Transmit/receive transceiver-B. Inverted I/O to coupling transformer that connects to channel B of the 1553 bus.

TABLE III. Pin functions - Continued.

Terminal symbol	I/O	Description
A00	I/O	Address bit 0 (LSB).
A02	I/O	Address bit 2.
A04	I/O	Address bit 4.
A06	I/O	Address bit 6.
A08	I/O	Address bit 8.
A10	I/O	Address bit 10.
A12	I/O	Address bit 12.
A14	I/O	Address bit 14.
$\overline{\text{MEMWR/ZEROWAIT}}$	O	Memory write. Output pulse to write data into memory.
$\overline{\text{MEMENA-IN/}}$ TRIGGERSEL	I	Memory enable in. Enables internal RAM only; connect directly to MEMENA-OUT.
$\overline{\text{INCMD}}$	O	In command. Indicates BC to RTU currently in message transfer sequence.
$\overline{\text{MSTRCLR}}$	I	Master clear. Power-on reset from CPU.
$\overline{\text{INT}}$	O	Interrupt. Interrupt pulse line to CPU.
$\overline{\text{IOEN}}$	O	Input/output enable. Output to enable external buffers/latches connecting the hybrid to the address/data bus.
$\overline{\text{SELECT}}$	I	Select. Input from the CPU. When active selects device for operation.
$\overline{\text{READYD}}$	O	Ready data. When active indicates data has been received from, or is available to, the CPU.
+5 VA	I	+5 V input power supply connection for the channel A transceiver.
$\overline{\text{TX/RX-A}}$	I/O	Transmit/receive transceiver-A. Inverted I/O to the coupling transformer that connects to channel A of the 1553 bus.
$\overline{\text{DTREQ/16/8}}$	I/O	Data Transfer Request or 16 Bit/8 Bit Transfer Mode Select. In transparent mode, active low output signal used to request access to the ram interface bus (address, data, and control buses). In buffered mode, input signal used to select between the 16 bit data transfer mode (16/8 = Logic 1) and the 8 bit data transfer mode (16/8 = Logic 0).

TABLE III. Pin functions - Continued.

Terminal symbol	I/O	Description
MEMWR/ZEROWAIT	I/O	Memory Write or Zero Wait State. In transparent m to strobe data into internal or external RAM (normally to strobe data into internal or external RAM (normally connected to the WR signal on external ram chips). In buffered mode, input signal used to select between the zero wait state mode (ZEROWAIT = logic 0) and the non-zero wait buffered mode, input signal used to select between the zero state mode (ZEROWAIT = logic 1).
MEMENA-IN/ TRIGGER SEL	I	Memory Enable Input or Trigger Select. In transparent mode, active low Chip Select (CS) input to the 4K X 16 of internal shared RAM. If only internal RAM is used connect directly to MEMENA-OUT. In buffered mode, input signal used to indicate the order in which byte pairs are transfered to or from the BU-65170/61580 by the host processor. This signal has no operation in the 16-bit buffered mode. In the 8-bit buffered mode, TRIGGER SEL should be asserted high (logic 1) if the byte oder for both read operations and write operations is MSB followed LSB. TRIGGER SEL should be asserted low (logic 0) if the byte oder for both read operations and write operations is LSB followed MSB.
DTACK POLARITY SEL	I/O	Data Transfer Acknowledge or Polarity Select. In transparent mode, active low output signal used to indicate acceptance of the ram interface bus in response to a data transfer grant (DTGRT). In 16-bit buffered mode (TRANSPARENT/BUFFERED = LOGIC 0 AND 16/8 = LOGIC 1), input signal used to control the logic sense of the RD/WR signal. If POLARITY SEL is connected to logic 1, RD/WR should be asserted high (logic 1) for a read operation and low (logic 0) for a write operation. If POLARITY SEL is connected to logic 0, RD/WR should be asserted low (logic 0) for a read operation and high (logic 1) for a write operation. In 8-bit buffered mode (TRANSPARENT/BUFFERED = LOGIC 0 AND 16/8 = LOGIC 0), input signal used to control the logic sense of the MSB/LSB signal. If POLARITY SEL is connected to logic 0, MSB/LSB should be asserted low (logic 0) to indicate the transfer of the least significant byte and high (logic 1) to indicate the transfer of the most significant byte. If POLARITY SEL is connected to logic 1, MSB/LSB should be asserted high (logic 1) to indicate the transfer of the least significant byte and low (logic 0) to indicate the transfer of the most significant byte.
DTGRT/MSB/LSB	I	Data Transfer Grant or Most Significant Byte/Least Significant Byte. In transparent mode, active low input signal asserted, in response to the DTREQ output, to indicate that control of the ram interface bus has been granted to the BU-65170/61580. In buffered mode, input signal used to indicate which byte is currently begin transfered (MSB or LSB). The logic sense of MSB/LSB is controlled by the POLARITY SEL input. MSB/LSB is only used in the 8-bit buffered mode.
SSFLAG/EXT TRIG	I	Sub System Flag/External Trigger Input. In the Remote Terminal mode, if this input is asserted low, the subsystem flag bit will be set in the device's RT Status Word. In the Bus Controller mode if the external BC Start option is enabled (bit 7 of Configuration Register #1), a low to high transition on this input will issue a BC Start command, starting execution of the current bc frame. In the Monitor mode if the external trigger is enabled (bit 7 of Configuration Register #1), a low to high transition on this input will issue a monitor trigger. This input has no effect in RT mode.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 98-05-14

Approved sources of supply for SMD 5962-96887 are listed below for immediate acquisition only and shall be added to QML-38534 during the next revision. QML-38534 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of QML-38534.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9688701HXA	19645	BU61582D1-140
5962-9688701HXC	19645	BU61582D1-110
5962-9688701HYA	19645	BU61582F1-140
5962-9688701HYC	19645	BU61582F1-110
5962-9688701HZA	19645	BU61582G1-140
5962-9688701HZC	19645	BU61582G1-110
5962-9688702HXA	19645	BU61582D2-140
5962-9688702HXC	19645	BU61582D2-110
5962-9688702HYA	19645	BU61582F2-140
5962-9688702HYC	19645	BU61582F2-110
5962-9688702HZA	19645	BU61582G2-140
5962-9688702HZC	19645	BU61582G2-110
5962-9688703HXA	19645	BU61583D1-140
5962-9688703HXC	19645	BU61583D1-110
5962-9688703HYA	19645	BU61583F1-140
5962-9688703HYC	19645	BU61583F1-110
5962-9688703HZA	19645	BU61583G1-140
5962-9688703HZC	19645	BU61583G1-110
5962-9688704HXA	19645	BU61583D2-140
5962-9688704HXC	19645	BU61583D2-110
5962-9688704HYA	19645	BU61583F2-140
5962-9688704HYC	19645	BU61583F2-110
5962-9688704HZA	19645	BU61583G2-140
5962-9688704HZC	19645	BU61583G2-110

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9688705HXA	19645	BU61582D0-140
5962-9688705HXC	19645	BU61582D0-110
5962-9688705HYA	19645	BU61582F0-140
5962-9688705HYC	19645	BU61582F0-110
5962-9688705HZA	19645	BU61582G0-140
5962-9688705HZC	19645	BU61582G0-110
5962-9688706HXA	19645	BU61583D0-140
5962-9688706HXC	19645	BU61583D0-110
5962-9688706HYA	19645	BU61583F0-140
5962-9688706HYC	19645	BU61583F0-110
5962-9688706HZA	19645	BU61583G0-140
5962-9688706HZC	19645	BU61583G0-110

1/ The lead finish shown for each PIN, representing a hermetic package, is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
19645	ILC Data Device Corporation 105 Wilbur Place Bohemia, NY 11716-2482

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in this information bulletin.