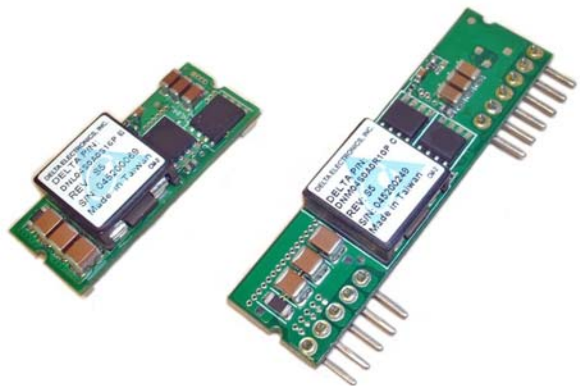
DELPHI SERIES



FEATURES

- High efficiency: 96% @ 5.0Vin, 3.3V/10A out
- Small size and low profile: (SIP)
  50.8x 13.4x 8.0 mm (2.00" x 0.53" x 0.31")
- Signle-in-line (SIP) packaging
- Standard footprint
- Voltage and resistor-based trim
- Pre-bias startup
- Output voltage tracking
- No minimum load required
- Output voltage programmable from
  0.75Vdc to 3.3Vdc via external resistor
- Fixed frequency operation
- Input UVLO, output OTP, OCP
- Remote ON/OFF
- Remote sense
- ISO 9001, TL 9000, ISO 14001, QS9000, OHSAS18001 certified manufacturing facility
- UL/cUL 60950 (US & Canada) Recognized, and TUV (EN60950) Certified
- CE mark meets 73/23/EEC and 93/68/EEC directives

Delphi DNM, Non-Isolated Point of Load DC/DC Power Modules: 2.8-5.5Vin, 0.75-3.3V/10A out

The Delphi Series DNM04, 2.8-5.5V input, single output, non-isolated Point of Load DC/DC converters are the latest offering from a world leader in power system and technology and manufacturing -- Delta Electronics, Inc. The DNM04 series provides a programmable output voltage from 0.75V to 3.3V using an external resistor. The DNM series has flexible and programmable tracking and sequencing features to enable a variety of startup voltages as well as sequencing and tracking between power modules. This product family is available in a surface mount or SIP package and provides up to 10A of current in an industry standard footprint. With creative design technology and optimization of component placement, these converters possess outstanding electrical and thermal performance and extremely high reliability under highly stressful operating conditions.

OPTIONS

- Negative On/Off logic
- Tracking feature
- SMD package

APPLICATIONS

- Telecom/DataCom
- Distributed power architectures
- Servers and workstations
- LAN/WAN applications
- Data processing applications

DATASHEET
DS_DNM04SIP10_05292006

TECHNICAL SPECIFICATIONS

(T_A = 25°C, airflow rate = 300 LFM, V_{in} = 2.8Vdc and 5.5Vdc, nominal Vout unless otherwise noted.)

PARAMETER	NOTES and CONDITIONS	DNM04S0A0R10PFA			
		Min.	Typ.	Max.	Units
ABSOLUTE MAXIMUM RATINGS					
Input Voltage (Continuous)		0		5.8	Vdc
Tracking Voltage				Vin,max	Vdc
Operating Temperature	Refer to Figure 45 for measuring point	-40		+125	°C
Storage Temperature		-55		+125	°C
INPUT CHARACTERISTICS					
Operating Input Voltage	Vout ≦ Vin –0.5	2.8		5.5	V
Input Under-Voltage Lockout					
Turn-On Voltage Threshold			2.2		V
Turn-Off Voltage Threshold			2.0		V
Maximum Input Current	Vin=2.8V to 5.5V, Io=Io,max			10	A
No-Load Input Current			70	100	mA
Off Converter Input Current			20	30	mA
Inrush Transient	Vin=2.8V to 5.5V, Io=Io,min to Io,max			0.1	A^2S
Recommended Inout Fuse				15	A
OUTPUT CHARACTERISTICS					
Output Voltage Set Point	Vin=5V, Io=100% Io, max, Tc=25℃	-2.0	Vo,set	+2.0	% Vo,set
Output Voltage Adjustable Range		0.7525		3.63	V
Output Voltage Regulation					
Over Line	Vin=2.8V to 5.5V		0.3		% Vo,set
Over Load	Io=Io,min to Io,max		0.4		% Vo,set
Over Temperature	Tc=-40℃ to 100℃		0.8		% Vo,set
Total Output Voltage Range	Over sample load, line and temperature	-3.0		+3.0	% Vo,set
Output Voltage Ripple and Noise	5Hz to 20MHz bandwidth				
Peak-to-Peak	Full Load, 1µF ceramic, 10µF tantalum		25	50	mV
RMS	Full Load, 1µF ceramic, 10µF tantalum		8	15	mV
Output Current Range		0		10	A
Output Voltage Over-shoot at Start-up				5	% Vo,set
Output DC Current-Limit Inception			220	280	% Io
Output Short-Circuit Current (Hiccup Mode)	Io,s/c		3.5		Adc
DYNAMIC CHARACTERISTICS					
Dynamic Load Response	10µF Tan & 1µF Ceramic load cap, 2.5A/µs				
Positive Step Change in Output Current	50% Io, max to 100% Io, max		200	300	mV
Negative Step Change in Output Current	100% Io, max to 50% Io, max		200	300	mV
Setting Time to 10% of Peak Devitation			25		µs
Turn-On Transient	Io=Io.max				
Start-Up Time, From On/Off Control	Vin=Vin,min, Vo=10% of Vo,set		4	6	ms
Start-Up Time, From Input	Vo=10% of Vo,set		4	6	ms
Output Voltage Rise Time	Time for Vo to rise from 10% to 90% of Vo,set		4	8	ms
Maximum Output Startup Capacitive Load	Full load; ESR ≧**1mΩ**			1000	µF
	Full load; ESR ≧**10mΩ**			5000	µF
EFFICIENCY					
Vo=3.3V	Vi=5V, 100% Load		96.0		%
Vo=2.5V	Vi=5V, 100% Load		94.2		%
Vo=1.8V	Vi=5V, 100% Load		92.4		%
Vo=1.5V	Vi=5V, 100% Load		91.4		%
Vo=1.2V	Vi=5V, 100% Load		90.0		%
Vo=0.75V	Vi=5V, 100% Load		86.3		%
FEATURE CHARACTERISTICS					
Switching Frequency			300		kHz
ON/OFF Control, (Negative logic)					
Logic Low Voltage	Module On, Von/off	-0.2		0.3	V
Logic High Voltage	Module Off, Von/off	1.5		Vin,max	V
Logic Low Current	Module On, Ion/off			10	µA
Logic High Current	Module Off, Ion/off		0.2	1	mA
ON/OFF Control, (Positive Logic)					
Logic High Voltage	Module On, Von/off			Vin,max	V
Logic Low Voltage	Module Off, Von/off	-0.2		0.3	V
Logic Low Current	Module On, Ion/off		0.2	1	mA
Logic High Current	Module Off, Ion/off			10	µA
Tracking Slew Rate Capability		0.1		2	V/msec
Tracking Delay Time	Delay from Vin.min to application of tracking voltage	10			ms
Tracking Accuracy	Power-up 2V/mS		100	200	mV
	Power-down 1V/mS		200	400	mV
Remote Sense Range				0.1	V
GENERAL SPECIFICATIONS					
MTBF	Io=100% of Io, max; Ta=25°C		21.91		M hours
Weight			10		grams
Over-Temperature Shutdown	Refer to Figure 45 for measuring point		130		°C

ELECTRICAL CHARACTERISTICS CURVES

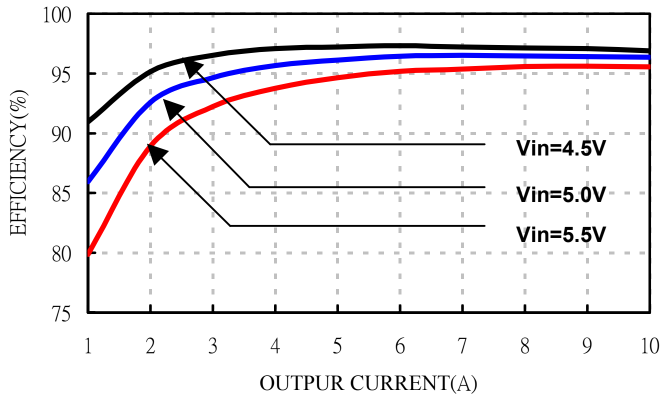


Figure 1: *Converter efficiency vs. output current (3.3V out)*

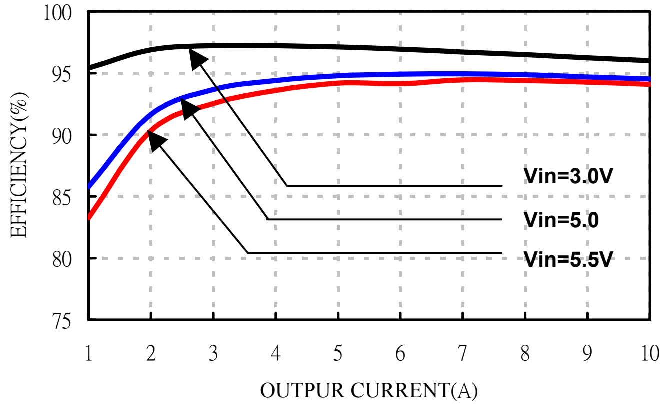


Figure 2: *Converter efficiency vs. output current (2.5V out)*

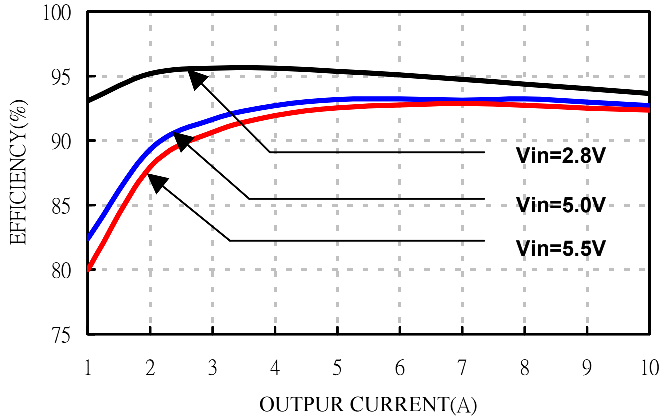


Figure 3: *Converter efficiency vs. output current (1.8V out)*

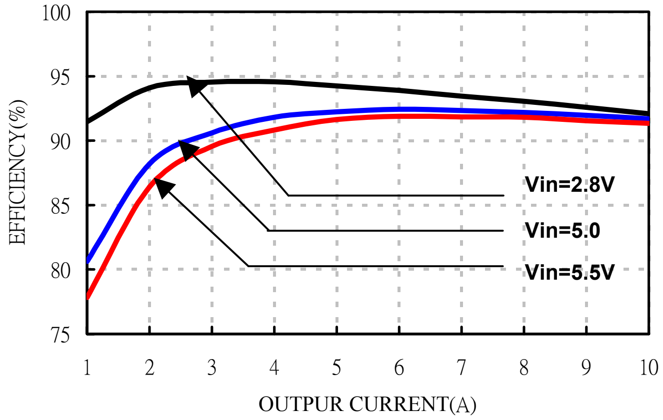


Figure 4: *Converter efficiency vs. output current (1.5V out)*

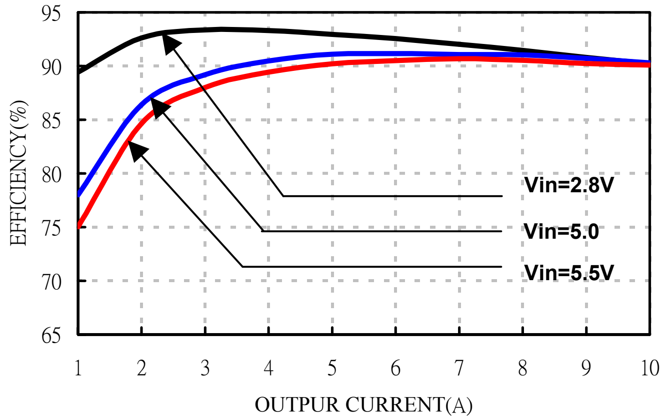


Figure 5: *Converter efficiency vs. output current (1.2V out)*

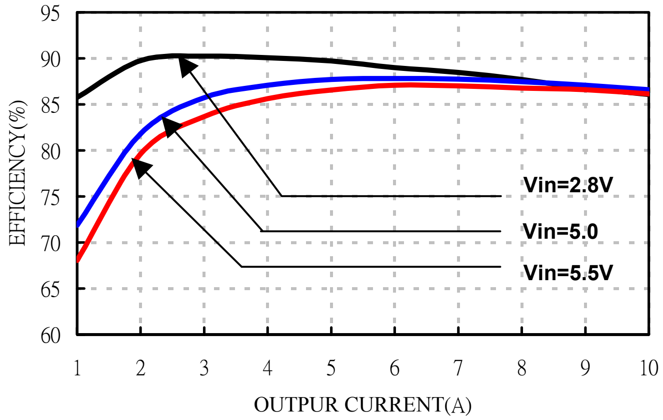


Figure 6: *Converter efficiency vs. output current (0.75V out)*

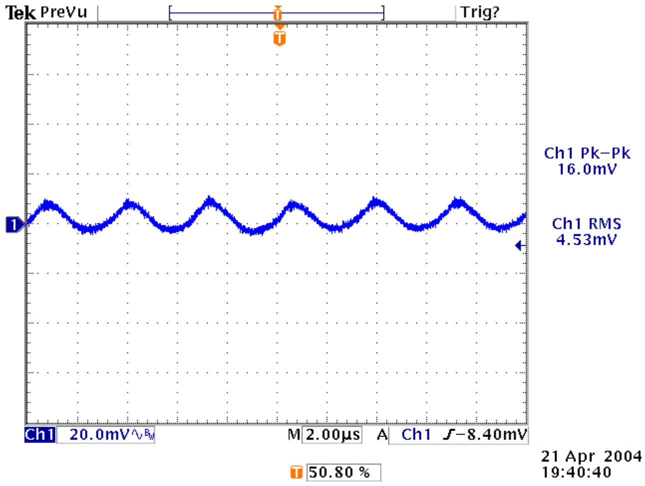


Figure 7: *Output ripple & noise at 3.3Vin, 2.5V/10A out*

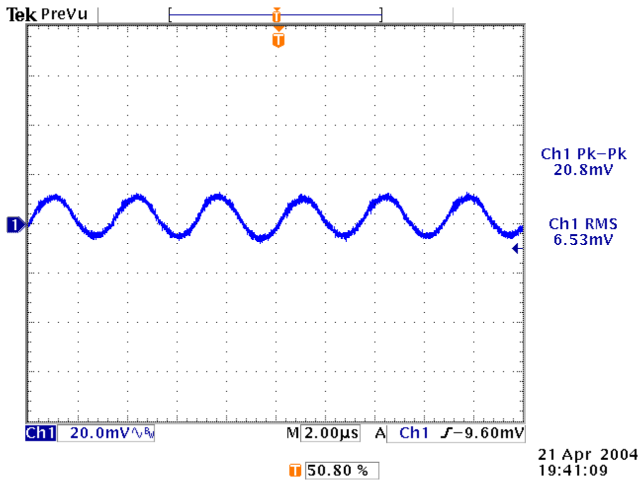


Figure 8: *Output ripple & noise at 3.3Vin, 1.8V/10A out*

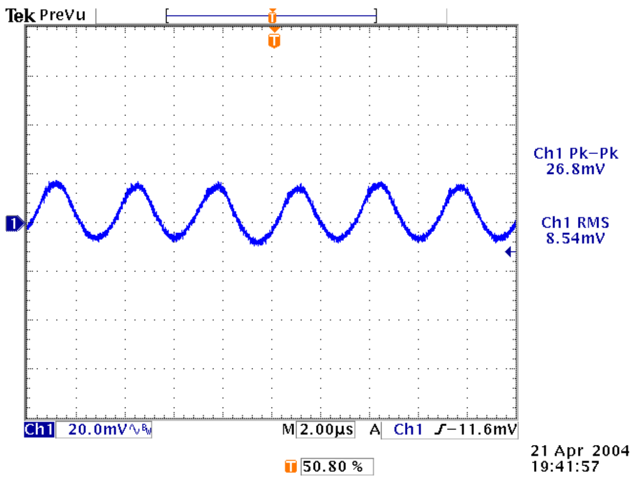


Figure 9: *Output ripple & noise at 5Vin, 3.3V/10A out*

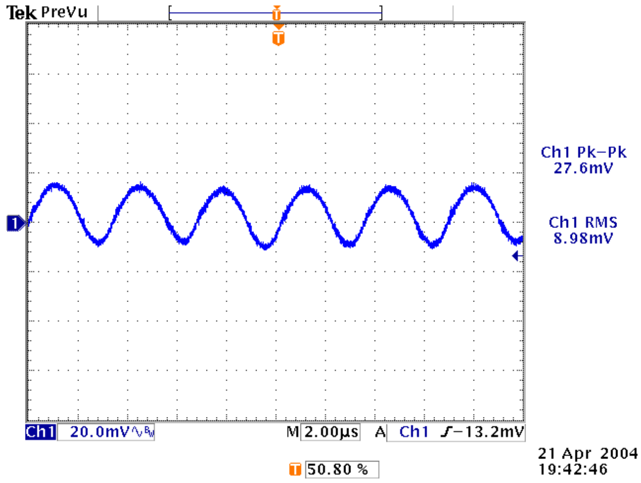


Figure 10: *Output ripple & noise at 5Vin, 1.8V/10A out*

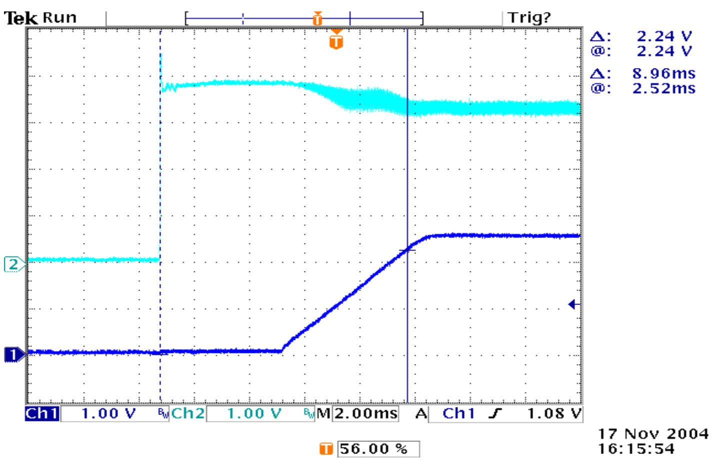


Figure 11: *Turn on delay time at 3.3Vin, 2.5V/10A out*

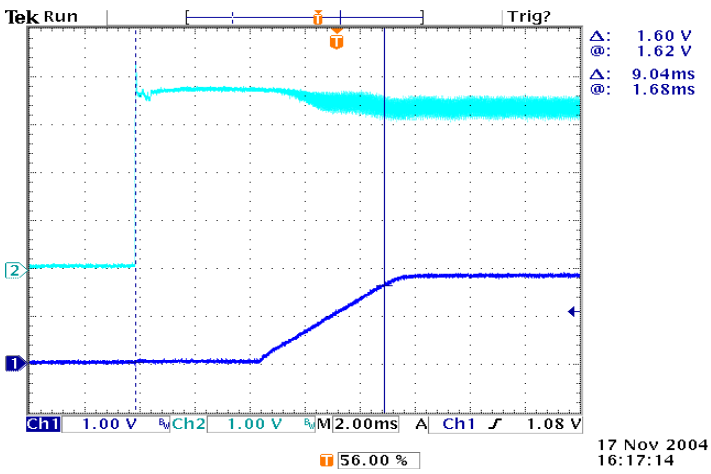


Figure 12: *Turn on delay time at 3.3Vin, 1.8V/10A out*

ELECTRICAL CHARACTERISTICS CURVES

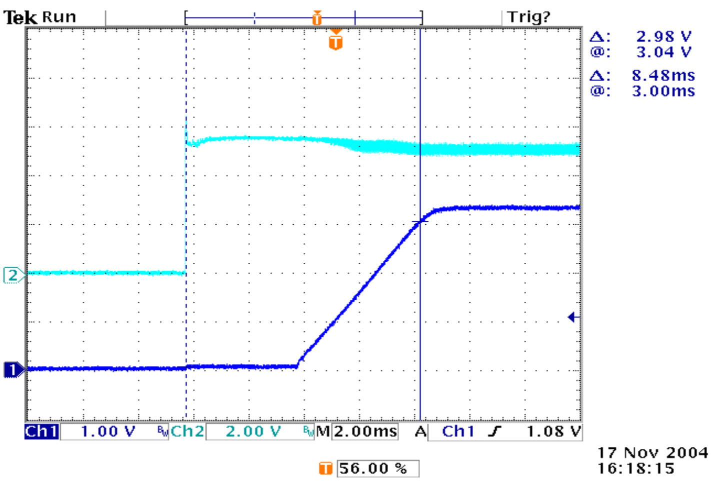


Figure 13: *Turn on delay time at 5Vin, 3.3V/10A out*

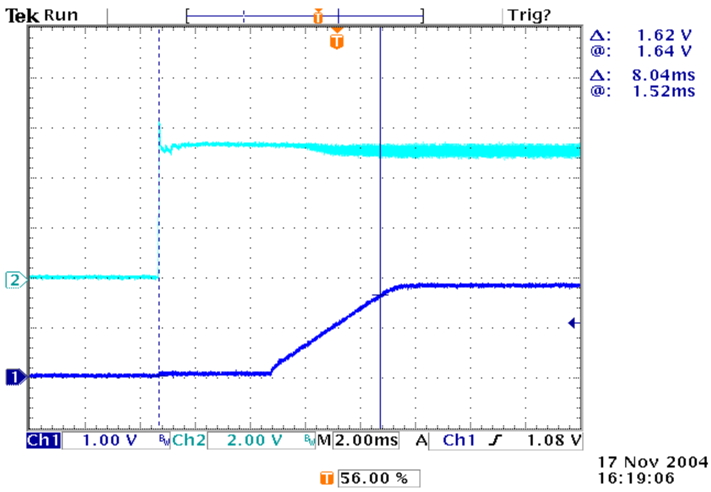


Figure 14: *Turn on delay time at 5Vin, 1.8V/10A out*

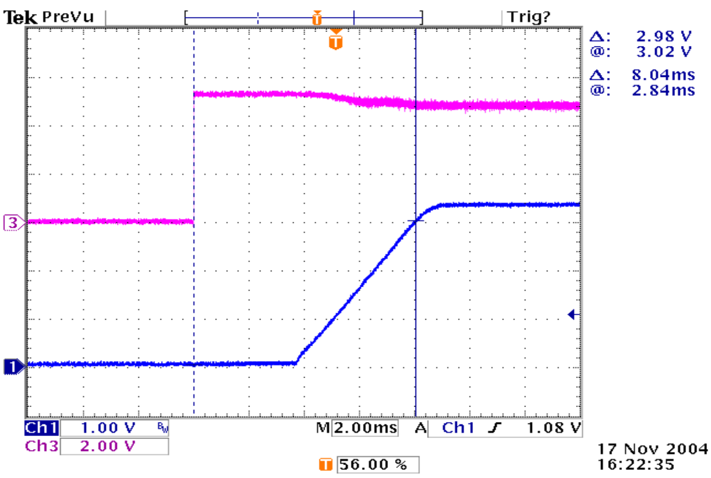


Figure 15: *Turn on delay time at remote turn on 5Vin, 3.3V/16A out*

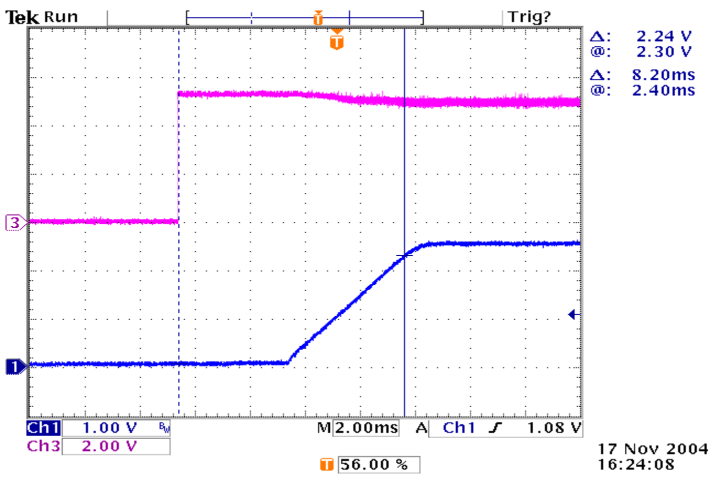


Figure 16: *Turn on delay time at remote turn on 3.3Vin, 2.5V/16A out*

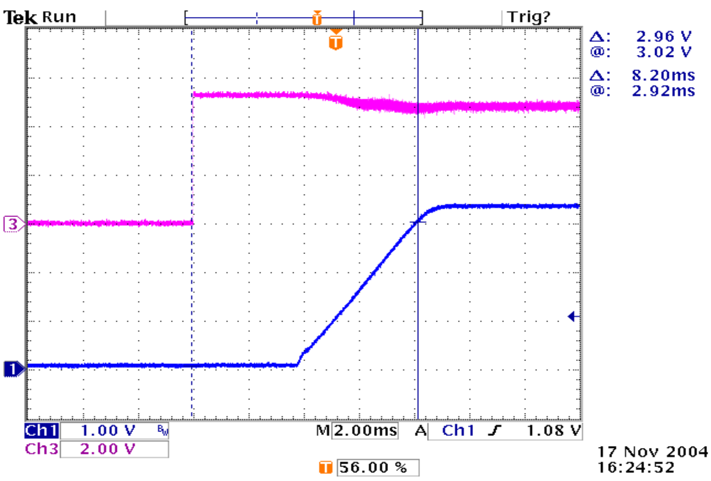


Figure 17: *Turn on delay time at remote turn on with external capacitors (Co= 5000 µF) 5Vin, 3.3V/16A out*

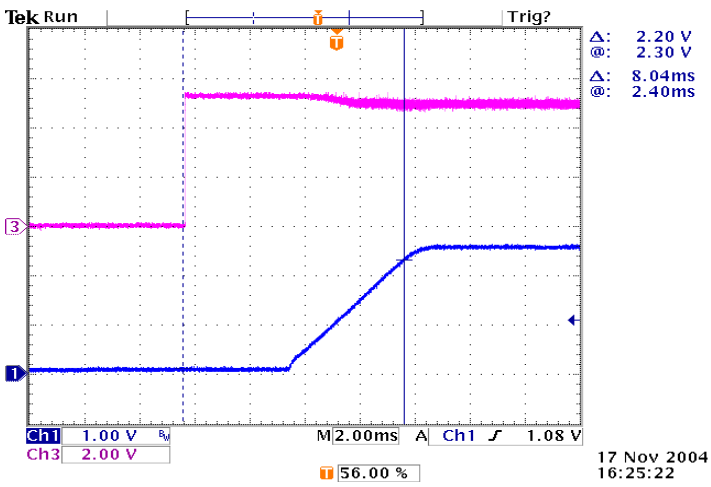


Figure 18: *Turn on delay time at remote turn on with external capacitors (Co= 5000 µF) 3.3Vin, 2.5V/16A out*

ELECTRICAL CHARACTERISTICS CURVES

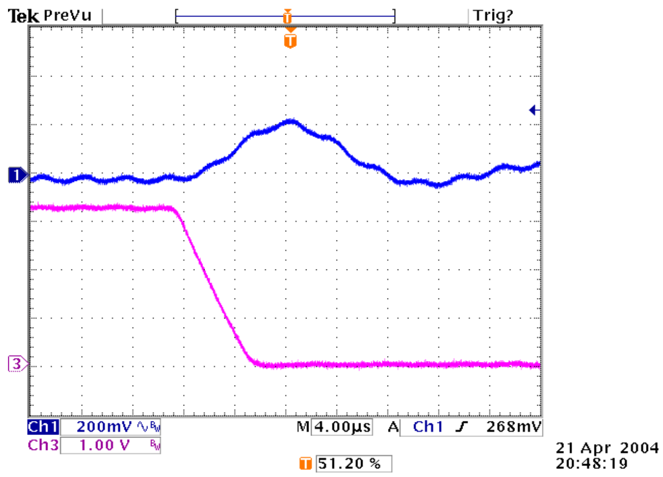


Figure 19: *Typical transient response to step load change at 2.5A/µS from 100% to 50% of Io, max at 5Vin, 3.3Vout (Cout = 1uF ceramic, 10µF tantalum)*

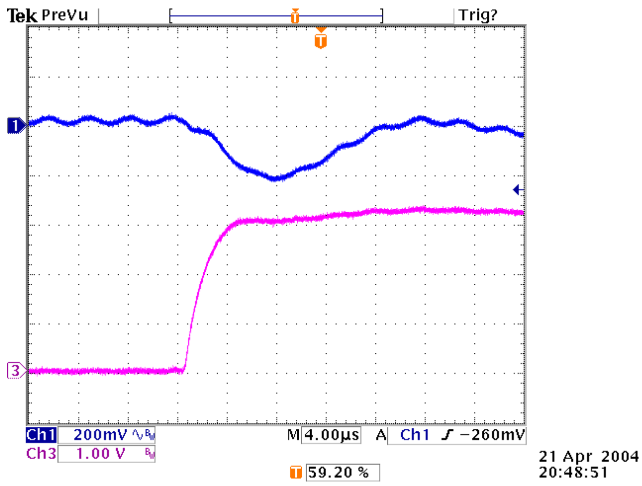


Figure 20: *Typical transient response to step load change at 2.5A/µS from 50% to 100% of Io, max at 5Vin, 3.3Vout (Cout =1uF ceramic, 10µF tantalum)*

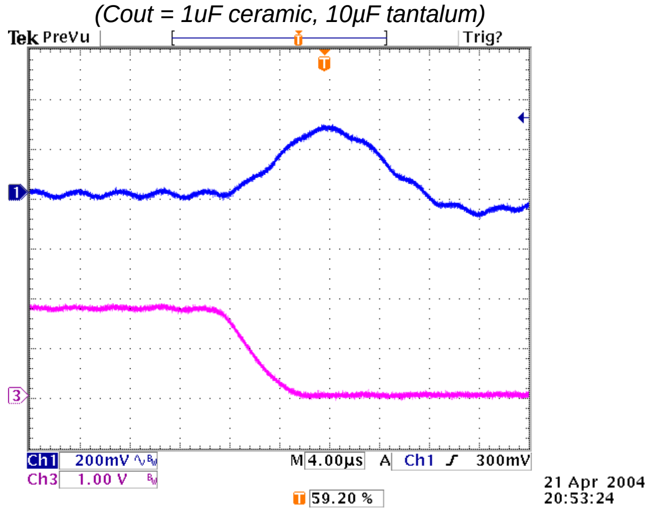


Figure 21: *Typical transient response to step load change at 2.5A/µS from 100% to 50% of Io, max at 5Vin, 1.8Vout (Cout =1uF ceramic, 10µF tantalum)*

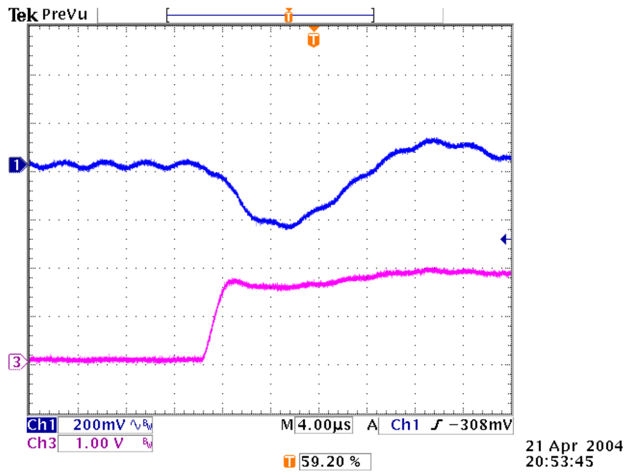


Figure 22: *Typical transient response to step load change at 2.5A/µS from 50% to 100% of Io, max at 5Vin, 1.8Vout (Cout = 1uF ceramic, 10µF tantalum)*

ELECTRICAL CHARACTERISTICS CURVES

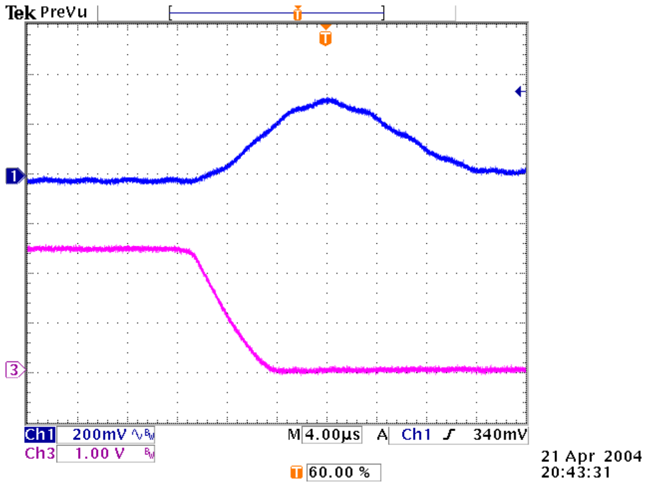


Figure 23: *Typical transient response to step load change at 2.5A/µS from 100% to 50% of Io, max at 3.3Vin, 2.5Vout (Cout =1uF ceramic, 10µF tantalum)*

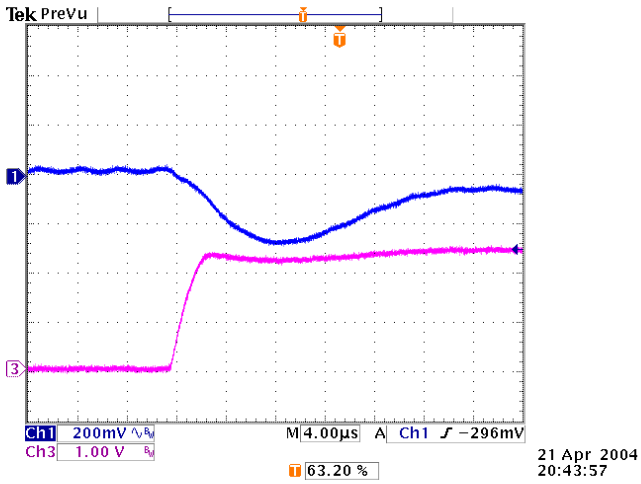


Figure 24: *Typical transient response to step load change at 2.5A/µS from 50% to 100% of Io, max at 3.3Vin, 2.5Vout (Cout =1uF ceramic, 10µF tantalum)*

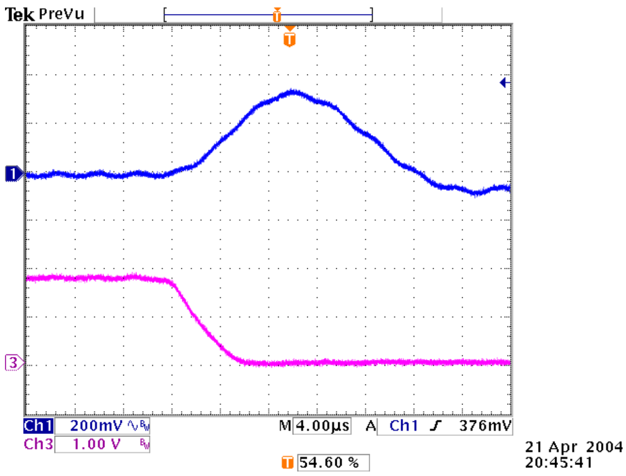


Figure 25: *Typical transient response to step load change at 2.5A/µS from 100% to 50% of Io, max at 3.3Vin, 1.8Vout (Cout =1uF ceramic, 10µF tantalum)*

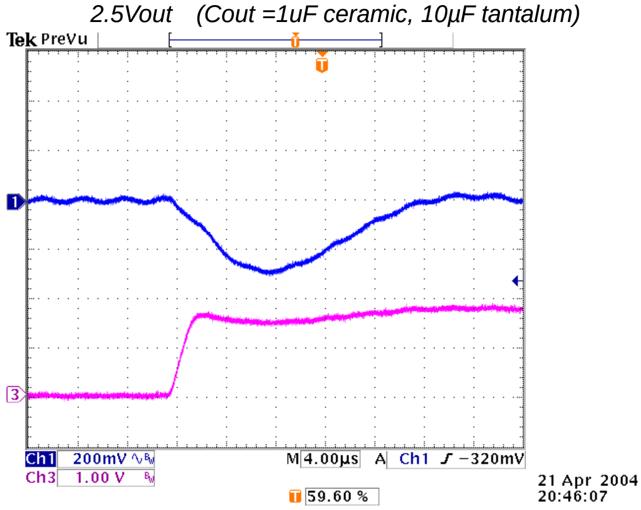


Figure 26: *Typical transient response to step load change at 2.5A/µS from 50% to 100% of Io, max at 3.3Vin, 1.8Vout (Cout = 1uF ceramic, 10µF tantalum)*

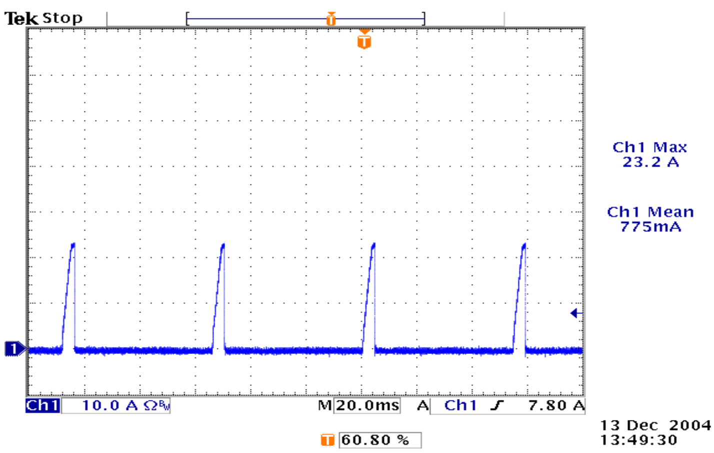


Figure 27: *Output short circuit current 5Vin, 0.75Vout*

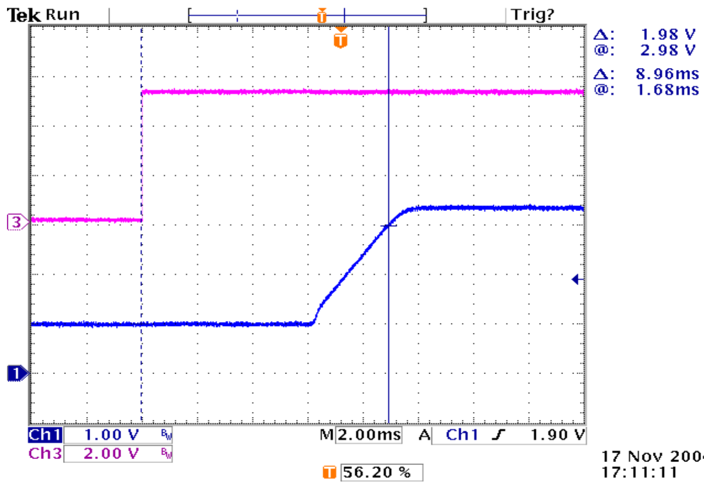
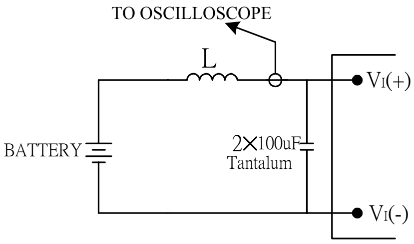


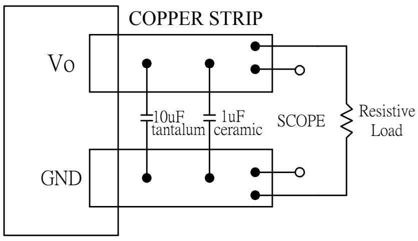
Figure 28:*Turn on with Prebias 5Vin, 3.3V/0A out, Vbias =1.0Vdc*

TEST CONFIGURATIONS



Note: Input reflected-ripple current is measured with a simulated source inductance. Current is measured at the input of the module.

Figure 29: *Input reflected-ripple test setup*



Note: Use a 10μF tantalum and 1μF capacitor. Scope measurement should be made using a BNC cable.

Figure 30: *Peak-peak output noise and startup transient measurement test setup.*

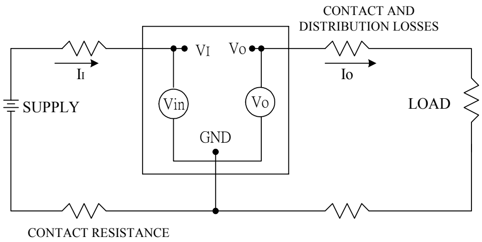


Figure 31: *Output voltage and efficiency measurement test setup*

Note: All measurements are taken at the module terminals. When the module is not soldered (via socket), place Kelvin connections at module terminals to avoid measurement errors due to contact resistance.

$$\eta = \left(\frac{Vo \times Io}{Vi \times Ii}\right) \times 100 \quad \%$$

DESIGN CONSIDERATIONS

Input Source Impedance

To maintain low noise and ripple at the input voltage, it is critical to use low ESR capacitors at the input to the module. Figure 32 shows the input ripple voltage (mVp-p) for various output models using 200 μF(2 x100uF) low ESR tantalum capacitor (KEMET p/n: T491D107M016AS, AVX p/n: TAJD107M106R, or equivalent) in parallel with 47 μF ceramic capacitor (TDK p/n:C5750X7R1C476M or equivalent). Figure 33 shows much lower input voltage ripple when input capacitance is increased to 400 μF (4 x 100 μF) tantalum capacitors in parallel with 94 μF (2 x 47 μF) ceramic capacitor.

The input capacitance should be able to handle an AC ripple current of at least:

$$Irms = Iout\sqrt{\frac{Vout}{Vin}\left(1-\frac{Vout}{Vin}\right)} \quad Arms$$

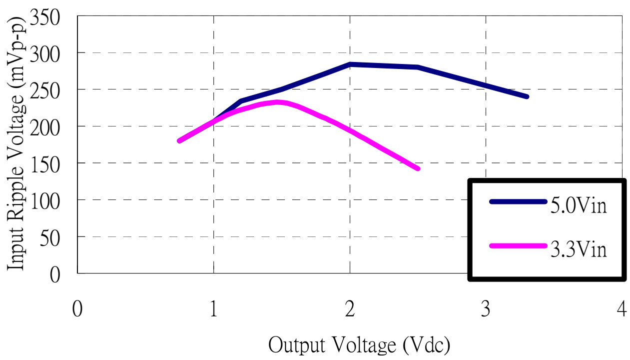


Figure 32: *Input voltage ripple for various output models, IO = 10 A (CIN = 2x100 μF tantalum // 47 μF ceramic)*

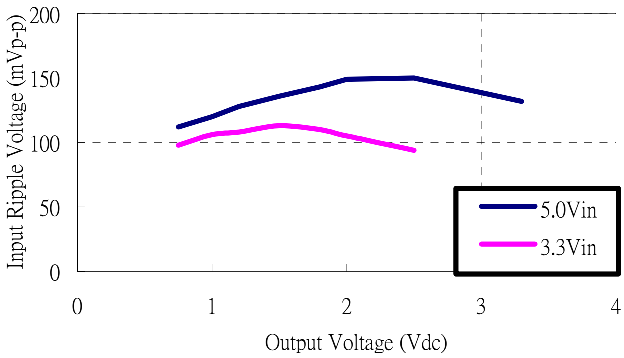


Figure 33: *Input voltage ripple for various output models, IO = 10 A (CIN = 4x100 μF tantalum // 2x47 μF ceramic)*

DESIGN CONSIDERATIONS (CON.)

The power module should be connected to a low ac-impedance input source. Highly inductive source impedances can affect the stability of the module. An input capacitance must be placed close to the modules input pins to filter ripple current and ensure module stability in the presence of inductive traces that supply the input voltage to the module.

Safety Considerations

For safety-agency approval the power module must be installed in compliance with the spacing and separation requirements of the end-use safety agency standards.

For the converter output to be considered meeting the requirements of safety extra-low voltage (SELV), the input must meet SELV requirements. The power module has extra-low voltage (ELV) outputs when all inputs are ELV.

The input to these units is to be provided with a maximum 15A time-delay fuse in the ungrounded lead.

FEATURES DESCRIPTIONS

Remote On/Off

The DNM/DNL series power modules have an On/Off pin for remote On/Off operation. Both positive and negative On/Off logic options are available in the DNM/DNL series power modules.

For positive logic module, connect an open collector (NPN) transistor or open drain (N channel) MOSFET between the On/Off pin and the GND pin (see figure 34). Positive logic On/Off signal turns the module ON during the logic high and turns the module OFF during the logic low. When the positive On/Off function is not used, leave the pin floating or tie to Vin (module will be On).

For negative logic module, the On/Off pin is pulled high with an external pull-up resistor (see figure 35). Negative logic On/Off signal turns the module OFF during logic high and turns the module ON during logic low. If the negative On/Off function is not used, leave the pin floating or tie to GND. (module will be On)

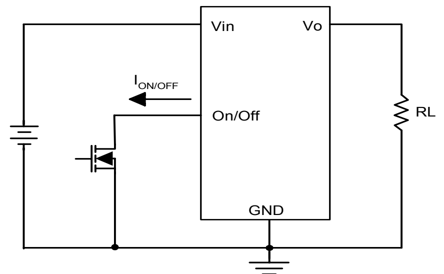


Figure 34: *Positive remote On/Off implementation*

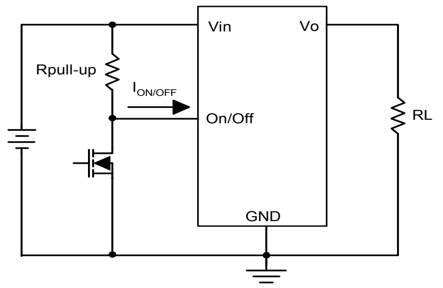


Figure 35: *Negative remote On/Off implementation*

Over-Current Protection

To provide protection in an output over load fault condition, the unit is equipped with internal over-current protection. When the over-current protection is triggered, the unit enters hiccup mode. The units operate normally once the fault condition is removed.

FEATURES DESCRIPTIONS (CON.)

Over-Temperature Protection

The over-temperature protection consists of circuitry that provides protection from thermal damage. If the temperature exceeds the over-temperature threshold the module will shut down. The module will try to restart after shutdown. If the over-temperature condition still exists during restart, the module will shut down again. This restart trial will continue until the temperature is within specification

Remote Sense

The DNM/DNL provide Vo remote sensing to achieve proper regulation at the load points and reduce effects of distribution losses on output line. In the event of an open remote sense line, the module shall maintain local sense regulation through an internal resistor. The module shall correct for a total of 0.5V of loss. The remote sense line impedance shall be < 10Ω.

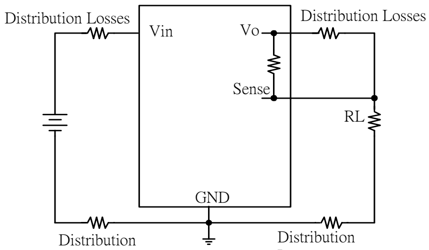


Figure 36: *Effective circuit configuration for remote sense operation*

Output Voltage Programming

The output voltage of the DNM/DNL can be programmed to any voltage between 0.75Vdc and 3.3Vdc by connecting one resistor (shown as Rtrim in Figure 37) between the TRIM and GND pins of the module. Without this external resistor, the output voltage of the module is 0.7525 Vdc. To calculate the value of the resistor Rtrim for a particular output voltage Vo, please use the following equation:

$$Rtrim = \left[\frac{21070}{Vo - 0.7525} - 5110\right]\Omega$$

For example, to program the output voltage of the DNL module to 1.8Vdc, Rtrim is calculated as follows:

$$Rtrim = \left[\frac{21070}{1.8 - 0.7525} - 5110\right]\Omega = 15K\Omega$$

DNL can also be programmed by apply a voltage between the TRIM and GND pins (Figure 38). The following equation can be used to determine the value of Vtrim needed for a desired output voltage Vo:

$$Vtrim = 0.7 - 0.1698 \times (Vo - 0.7525)$$

For example, to program the output voltage of a DNL module to 3.3 Vdc, Vtrim is calculated as follows

$$Vtrim = 0.7 - 0.1698 \times (3.3 - 0.7525) = 0.267V$$

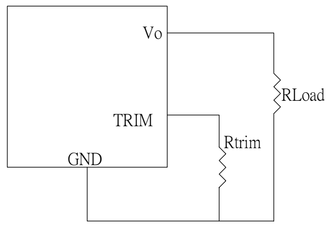


Figure 37: *Circuit configuration for programming output voltage using an external resistor*

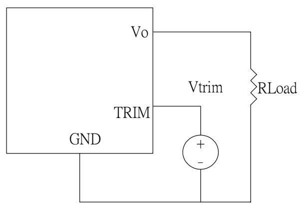


Figure 38: *Circuit Configuration for programming output voltage using external voltage source*

Table 1 provides Rtrim values required for some common output voltages, while Table 2 provides value of external voltage source, Vtrim, for the same common output voltages. By using a 1% tolerance trim resistor, set point tolerance of ±2% can be achieved as specified in the electrical specification.

Table 1

Vo(V)	Rtrim(KΩ)
0.7525	Open
1.2	41.97
1.5	23.08
1.8	15.00
2.5	6.95
3.3	3.16

Table 2

Vo(V)	Vtrim(V)
0.7525	Open
1.2	0.624
1.5	0.573
1.8	0.522
2.5	0.403
3.3	0.267

FEATURE DESCRIPTIONS (CON.)

The amount of power delivered by the module is the voltage at the output terminals multiplied by the output current. When using the trim feature, the output voltage of the module can be increased, which at the same output current would increase the power output of the module. Care should be taken to ensure that the maximum output power of the module must not exceed the maximum rated power (Vo.set x Io.max ≤ P max).

Voltage Margining

Output voltage margining can be implemented in the DNL modules by connecting a resistor, $R_{margin-up}$, from the Trim pin to the ground pin for margining-up the output voltage and by connecting a resistor, $R_{margin-down}$, from the Trim pin to the output pin for margining-down. Figure 39 shows the circuit configuration for output voltage margining. If unused, leave the trim pin unconnected. A calculation tool is available from the evaluation procedure which computes the values of $R_{margin-up}$ and $R_{margin-down}$ for a specific output voltage and margin percentage.

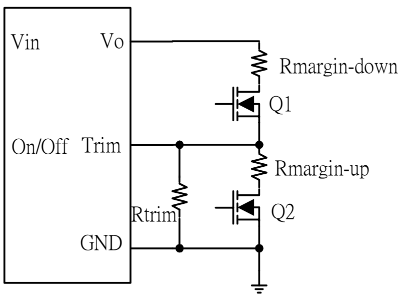


***Figure 39:** Circuit configuration for output voltage margining*

Voltage Tracking

The DNM/DNL family was designed for applications that have output voltage tracking requirements during power-up and power-down. The devices have a TRACK pin to implement three types of tracking method: sequential, ratio-metric and simultaneous. TRACK simplifies the task of supply voltage tracking in a power system by enabling modules to track each other, or any external voltage, during power-up and power-down.

By connecting multiple modules together, customers can get multiple modules to track their output voltages to the voltage applied on the TRACK pin.

The DNL family has 3 different option codes for TRACK function

The DNL family has 3 different option codes for TRACK function.

Option code A: the output voltage TRACK characteristic can be achieved when the output voltage of PS2 follows the output voltage of PS1 on a volt-to-volt basis. (Figure 41)

Option code B: No TRACK function

Option code C: Implementation of advanced power tracking techniques is based on connecting the power good signal or selecting proper value for external resistor R1 (Figure 40 to Figure 43).

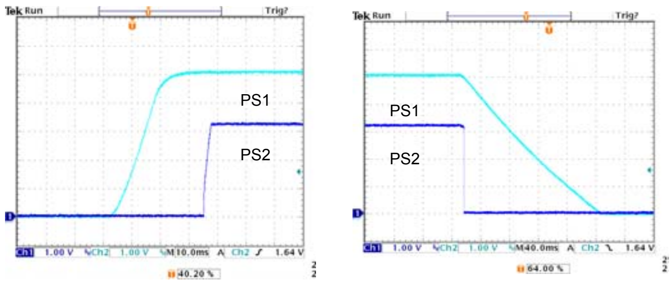


***Figure 40:** Sequential*

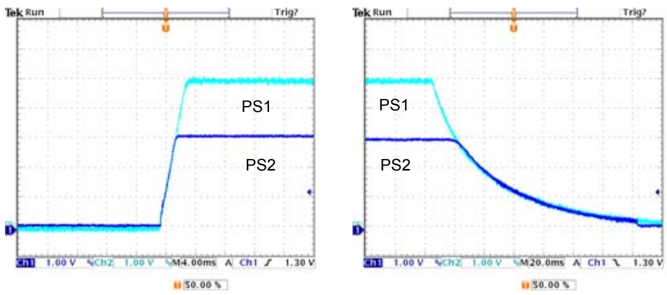


***Figure 41:** Simultaneous*

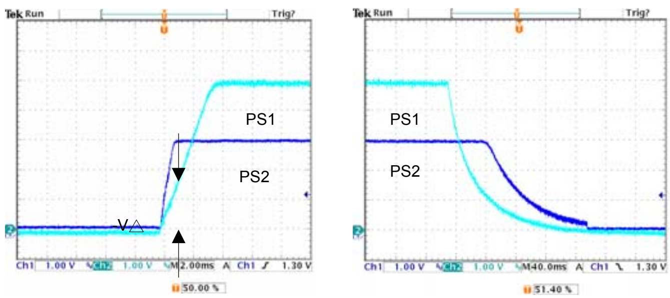


***Figure 42:** Ratio-metric*

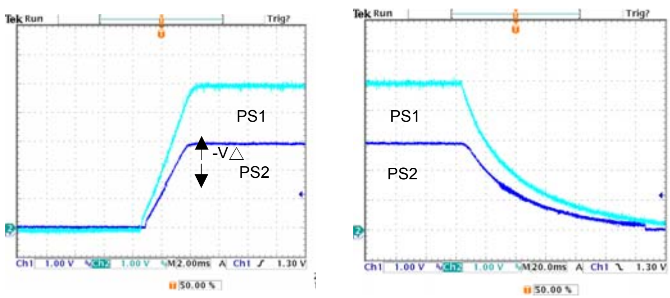
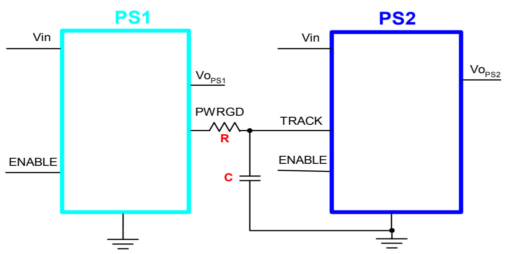


***Figure 43:** Ratio-metric*

FEATURE DESCRIPTIONS (CON.)

Sequential

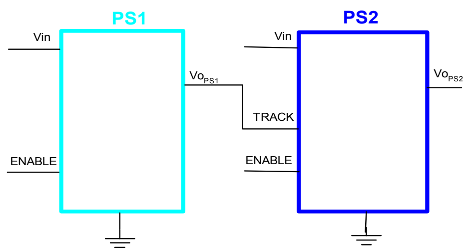
Sequential start-up (Figure 40) is implemented by connecting the power good pin of PS1 to the TRACK pin of PS2 with a resistor–capacitor (RC) circuit. Suggest to use 1μF ceramic capacitor and 2KΩ resistor here. Besides, this configuration requires PS1 to have a power good function.



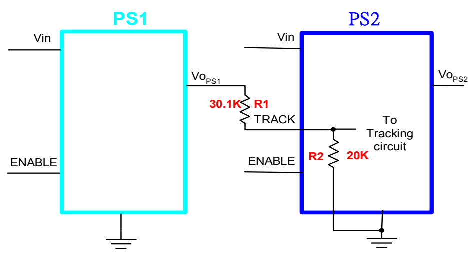
Simultaneous

Simultaneous tracking (Figure 41) is implemented by using a voltage divider around the TRACK pin. The objective is to minimize the voltage difference between the power supply outputs during power up and down.

For type A (DNX0A0XXXX **A**), the simultaneous tracking can be accomplished by connecting Vo_{PS1} to the TRACK pin of PS2 where the voltage divider is inside the PS2.



For type C (DNX0A0XXXX **C**), the simultaneous tracking can be accomplished by putting R1 equal to 30.1KΩ through Vo_{PS1} to the TRACK pin of PS2.



Ratio-Metric

Ratio–metric is implemented by selecting the resistor values of the voltage divider on the TRACK pin. To simplify the tracking design, set initial value of R2 equal to 20KΩ at internal circuit and adjust resistor R1 for the different tracking method. The circuit diagram of Ratio-Metric is the same as **Simultaneous** when Vo_{PS2} tracks the Vo_{PS1}.

For Ratio-Metric applications that need the outputs of PS1 and PS2 go to the regulation set point at the same time (Figure 43), use the following equation (1) to calculate the value of resistor R1,

set $\triangle V = Vo_{set,PS1} - Vo_{set,PS2}$ and $\triangle V$ will be negative.

$$R1 = \frac{[(Vo_{set,PS2} + \Delta V) - Vref]}{Vref} * 20K\Omega \text{ --------------(1)}$$

Note:

1. $Vref = 0.4 \times Vo_{set,PS2}$
2. $\triangle V$ is the maximum difference of voltage between PS1 and PS2 supply voltage.

For Ratio-Metric applications that need the PS2 supply voltage rises first at power up and falls second at power down (Figure 42), use the following equation (2) to calculate the value of resistor R1,

set $\triangle V \leqq 0.4 \times Vo_{set,PS2}$ and $\triangle V$ will be negative.

$$R1 = \frac{[(Vo_{set,ps2} - \Delta V) - Vref]}{Vref} * 20K\Omega \text{ ------------------(2)}$$

Note:

1. $Vref = 0.4 \times Vo_{set,PS2}$

$\triangle V$ is defined as the voltage difference between Vo_{PS1} and Vo_{PS2} when Vo_{PS2} reaches its rated voltage.

THERMAL CONSIDERATIONS

Thermal management is an important part of the system design. To ensure proper, reliable operation, sufficient cooling of the power module is needed over the entire temperature range of the module. Convection cooling is usually the dominant mode of heat transfer.

Hence, the choice of equipment to characterize the thermal performance of the power module is a wind tunnel.

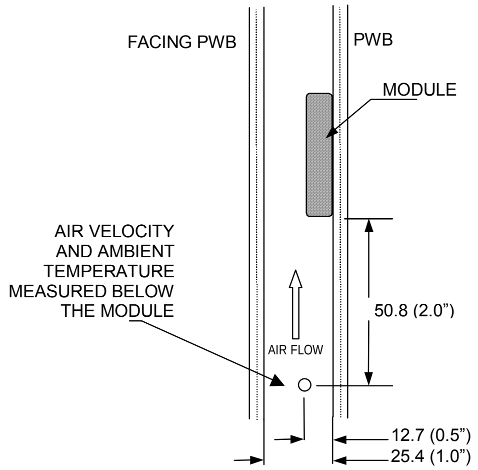
Thermal Testing Setup

Delta's DC/DC power modules are characterized in heated vertical wind tunnels that simulate the thermal environments encountered in most electronics equipment. This type of equipment commonly uses vertically mounted circuit cards in cabinet racks in which the power modules are mounted.

The following figure shows the wind tunnel characterization setup. The power module is mounted on a test PWB and is vertically positioned within the wind tunnel. The height of this fan duct is constantly kept at 25.4mm (1'').

Thermal Derating

Heat can be removed by increasing airflow over the module. To enhance system reliability, the power module should always be operated below the maximum operating temperature. If the temperature exceeds the maximum module temperature, reliability of the unit may be affected.



Note: Wind Tunnel Test Setup Figure Dimensions are in millimeters and (Inches)

Figure 44: *Wind tunnel test setup*

THERMAL CURVES

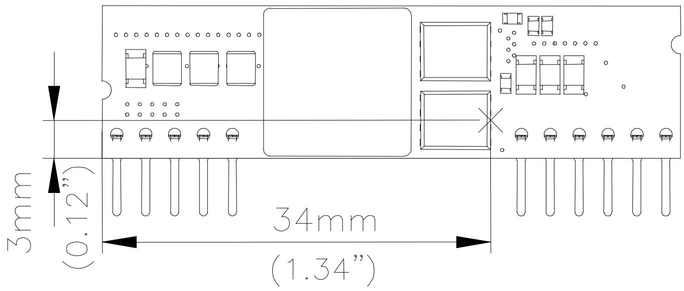


Figure 45: *Temperature measurement location*
** The allowed maximum hot spot temperature is defined at 125℃*

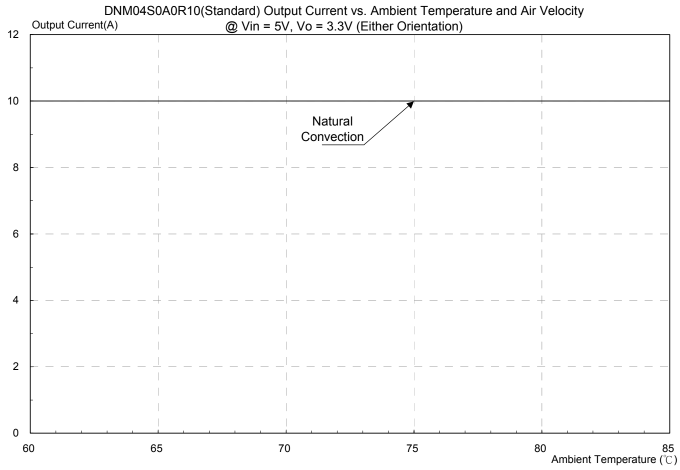


Figure 46: *DNM04S0A0R10 (Standard) Output current vs. ambient temperature and air velocity@Vin=5V, Vo=3.3V(Either Orientation)*

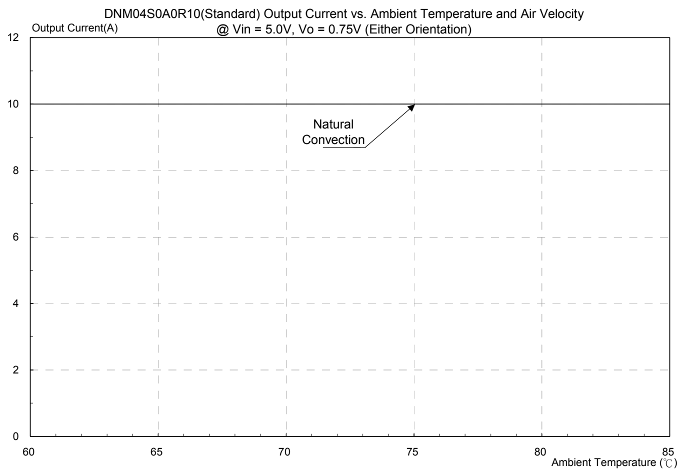


Figure 47: *DNM04S0A0R10(Standard) Output current vs. ambient temperature and air velocity@Vin=5V, Vo=0.75V(Either Orientation)*

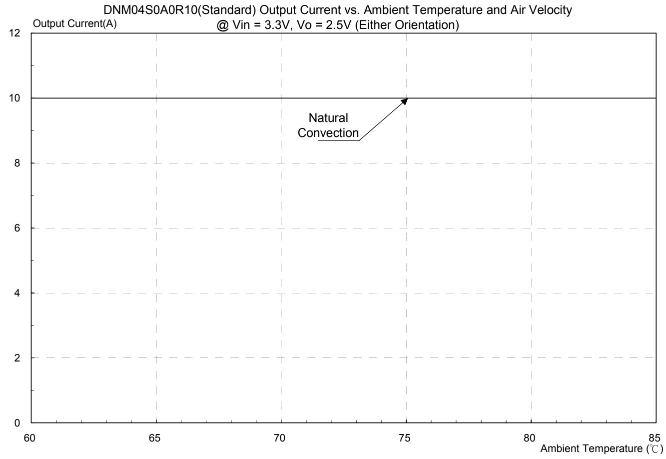


Figure 48: *DNM04S0A0R10 (Standard) Output current vs. ambient temperature and air velocity@Vin=5V, Vo=2.5V(Either Orientation)*

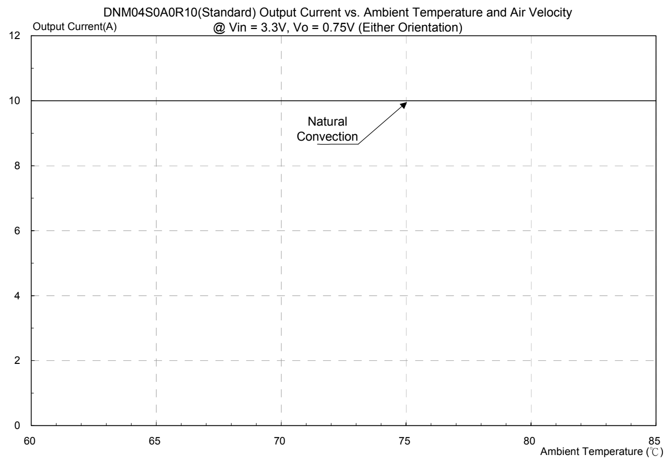
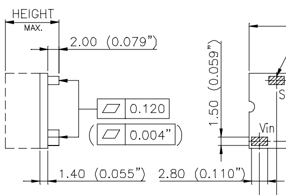


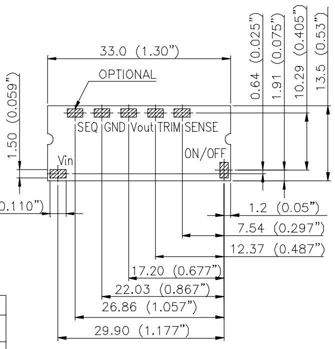
Figure 49: *DNM04S0A0R10 (Standard) Output current vs. ambient temperature and air velocity@ Vin=5V, Vo=0.75V(Either Orientation)*

MECHANICAL DRAWING

SMD PACKAGE (OPTIONAL)



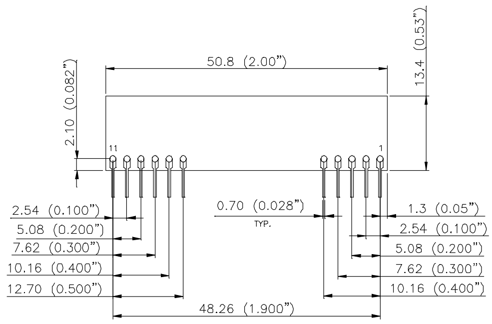
SIDE VIEW



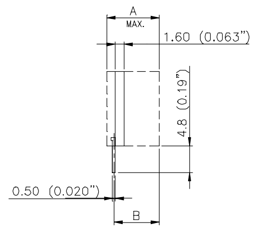
BOTTOM VIEW

	HEIGHT
04S	8.3 (0.33")
12S	9.7 (0.38")

SIP PACKAGE

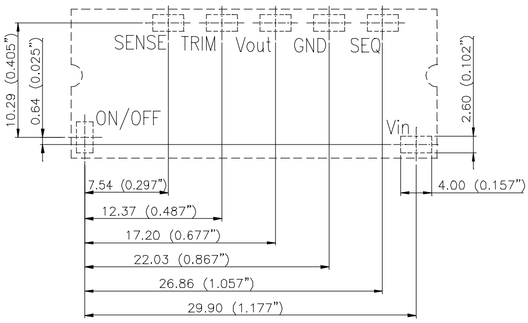


BACK VIEW

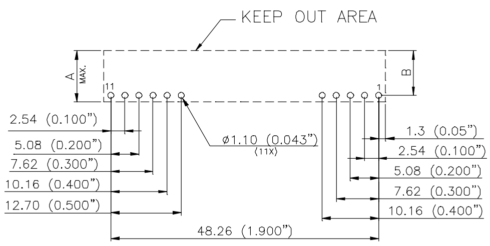


SIDE VIEW

	A	B
04S	8.0 (0.31")	6.75 (0.265")
12S	9.5 (0.37")	8.15 (0.320")



RECOMMENDED P.W.B PAD LAYOUT



	A	B
04S	8.0 (0.31")	6.75 (0.265")
12S	9.5 (0.37")	8.15 (0.320")

PIN#	Function
1	Vo
2	Vo
3	Vo SENSE
4	Vo
5	GND
6	GND
7	Vi
8	Vi
9	TRACK
10	TRIM
11	ON/OFF

→ OPTIONAL (pin 9)

RECOMMENDED P.W.B PAD LAYOUT

NOTES:
DIMENSIONS ARE IN MILLIMETERS AND (INCHES)
TOLERANCES: X.Xmm±0.5mm(X.XX in.±0.02 in.)
X.XXmm±0.25mm(X.XXX in.±0.010 in.)

PART NUMBERING SYSTEM

DNM	04	S	0A0	R	10	P	F	A
Product Series	Input Voltage	Numbers of Outputs	Output Voltage	Package Type	Output Current	On/Off logic		Option Code
DNL - 16A DNM - 10A DNS - 6A	04 - 2.8~5.5V 12 - 9~14V	S - Single	0A0 - Programmable	R - SIP S - SMD	10 - 10A	N- negative P- positive	F- RoHS 6/6 (Lead Free)	A - Standard Function: Sequencing B - No tracking pin C - Tracking feature

MODEL LIST

Model Name	Packaging	Input Voltage	Output Voltage	Output Current	Efficiency 5.0Vin, 100% load
DNM04S0A0R10PFA	SIP	2.8 ~ 5.5Vdc	0.75 V~ 3.3Vdc	10A	96.0% (3.3V)
DNM04S0A0S10PFA	SMD	2.8 ~ 5.5Vdc	0.75 V~ 3.3Vdc	10A	96.0% (3.3V)

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