HARRIS SEMICONDUCTOR

DG411, DG412, DG413

Monolithic Quad SPST, CMOS Analog Switches

August 1997

Features

- ON-Resistance ..... <35Ω Max
- Low Power Consumption (P_D) ..... <35µW
- Fast Switching Action
  - t_{ON} ..... <175ns
  - t_{OFF} ..... <145ns
- Low Charge Injection
- Upgrade from DG211/DG212
- TTL, CMOS Compatible
- Single or Split Supply Operation

Applications

- Audio Switching
- Battery Operated Systems
- Data Acquisition
- Hi-Rel Systems
- Sample and Hold Circuits
- Communication Systems
- Automatic Test Equipment

Description

The DG411 series monolithic CMOS analog switches are drop-in replacements for the popular DG211 and DG212 series devices. They include four independent single pole throw (SPST) analog switches, and TTL and CMOS compatible digital inputs.

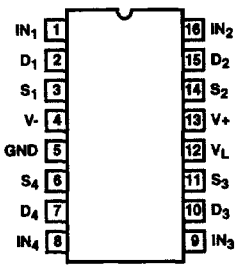
These switches feature lower analog ON resistance (<35Ω) and faster switch time (t_{ON} < 175ns) compared to the DG211 or DG212. Charge injection has been reduced, simplifying sample and hold applications.

The improvements in the DG411 series are made possible by using a high voltage silicon-gate process. An epitaxial layer prevents the latch-up associated with older CMOS technologies. The 44V maximum voltage range permits controlling $40V_{P-P}$ signals. Power supplies may be single-ended from +5V to +34V, or split from ±5V to ±20V.

The four switches are bilateral, equally matched for AC or bidirectional signals. The ON resistance variation with analog signals is quite low over a 15V analog input ange. The switches in the DG411 and DG412 are identical, differing only in the polarity of the selection logic. Two of the switches in the DG413 (#1 and #4) use the logic of the DG211 and DG411 (i.e., a logic "0" turns the switch ON) and the other two switches use DG212 and DG412 positive logic. This permits independent control of turn-on and turn-off times for SPDT configurations, permitting "break-before-make" or "make-before-break" operation with a minimum of external logic.

Pinout

DG411, DG412, DG413
(CERDIP, PDIP, SOIC)
TOP VIEW



Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
DG411AK/883	-55 to 125	16 Ld CERDIP	F16.3
DG411DJ	-40 to 85	16 Ld PDIP	E16.3
DG411DY	-40 to 85	16 Ld SOIC	M16.15
DG411EJ (Note)	-40 to 85	16 Ld PDIP	E16.3
DG411EY (Note)	-40 to 85	16 Ld SOIC	M16.15
DG412AK/883	-55 to 125	16 Ld CERDIP	F16.3
DG412DJ	-40 to 85	16 Ld PDIP	E16.3
DG412DY	-40 to 85	16 Ld SOIC	M16.15
DG412EJ (Note)	-40 to 85	16 Ld PDIP	E16.3
DG412EY (Note)	-40 to 85	16 Ld SOIC	M16.15
DG413AK/883	-55 to 125	16 Ld CERDIP	F16.3
DG413DJ	-40 to 85	16 Ld PDIP	E16.3
DG413DY	-40 to 85	16 Ld SOIC	M16.15
DG413EJ (Note)	-40 to 85	16 Ld PDIP	E16.3
DG413EY (Note)	-40 to 85	16 Ld SOIC	M16.15

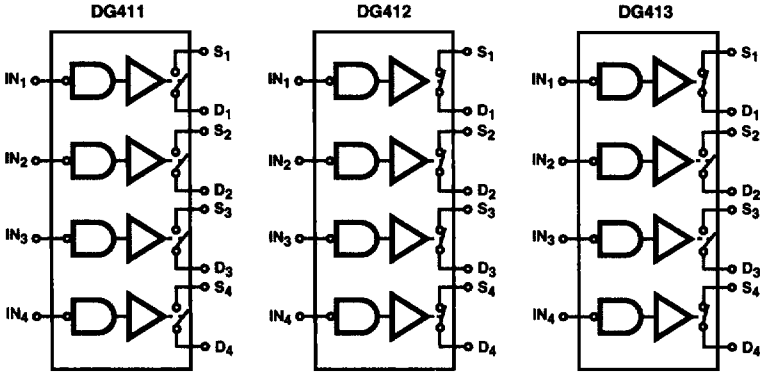
NOTE: Extended Processing Flow

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **3282.4**

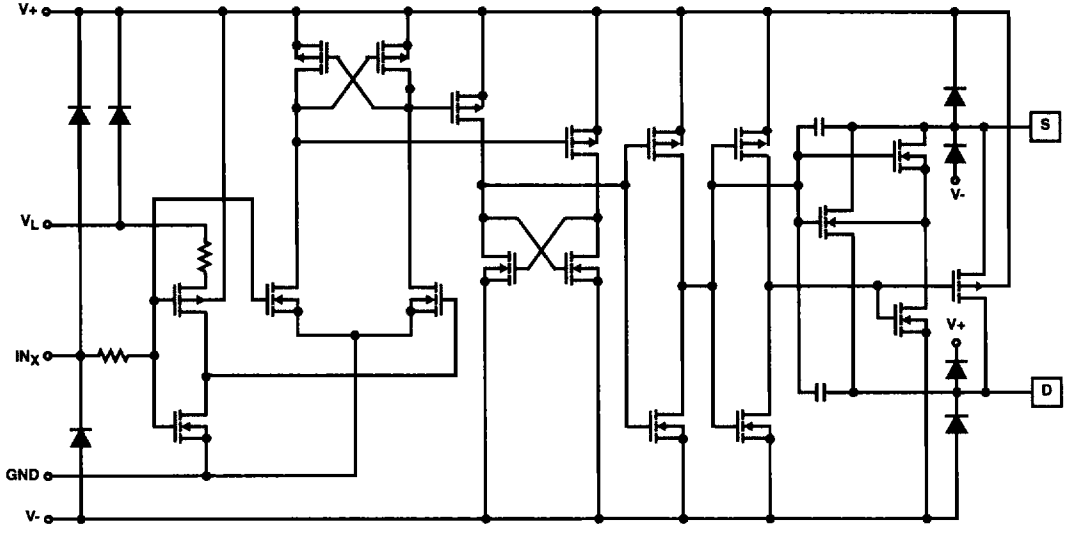
Functional Diagrams

Four SPST Switches per Package Switches Shown for Logic "1" Input



Typical Schematic Diagram

(Typical Channel)



Absolute Maximum Ratings

V+ to V- 44V
GND to V- 25V
V_L ..... (GND -0.3V) to (V+) +0.3V
Digital Inputs, V_S, V_D (Note 1) ..... (V-) -2V to (V+) + 2V or 30mA, Whichever Occurs First
Continuous Current (Any Terminal) 30mA
Current, S or D (Pulsed 1ms, 10% Duty Cycle) 100mA

Operating Conditions

Operating Voltage Range ..... ±20V (Max)
Operating Temperature Range ..... -40°C to 85°C
Input Low Voltage ..... 0.8V (Max)
Input High Voltage ..... 2.4V (Min)
Input Rise and Fall Time ..... ≤20ns
Operating Temperature
(D Suffix) ..... -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
PDIP Package	100	N/A
SOIC Package	115	N/A
CERDIP Package	75	20

Maximum Junction Temperature (Plastic Packages) ..... 150°C
Maximum Junction Temperature (Ceramic Package) ..... 175°C
Maximum Storage Temperature Range ..... -65°C to 125°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:
1. Signals on S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Test Conditions: V+ = +15V, V- = -15V, V_L = 5V, V_{IN} = 2.4V, 0.8V (Note 3), Unless Otherwise Specified

PARAMETER	TEST CONDITIONS		(NOTE 4) TEMP (°C)	D SUFFIX -40°C TO 85°C (NOTE 5) MIN	(NOTE 6) TYP	(NOTE 5) MAX	UNITS
DYNAMIC CHARACTERISTICS							
Turn-ON Time, t_{ON}	R_L = 300Ω, C_L = 35pF, V_S = ±10V, (See Figure 7)		25	-	110	175	ns
			Hot	-	-	220	ns
Turn-OFF Time, t_{OFF}			25	-	100	145	ns
			Hot	-	-	160	ns
Break-Before-Make Time Delay	DG413 Only, R_L = 300Ω, C_L = 35pF		25	-	25	-	ns
Charge Injection, Q	C_L = 10nF, V_G = 0V, R_G = 0Ω		25	-	5	-	pC
OFF Isolation	R_L = 50Ω, C_L = 5pF, f = 1MHz		25	-	68	-	dB
Crosstalk (Channel-to-Channel)			25	-	85	-	dB
Source OFF Capacitance, $C_{S(OFF)}$	f = 1MHz		25	-	9	-	pF
Drain OFF Capacitance, $C_{D(OFF)}$			25	-	9	-	pF
Channel ON Capacitance, $C_{D(ON)} + C_{S(ON)}$			25	-	35	-	pF
DIGITAL CONTROL							
Input Current V_{IN} Low, I_{IL}	V_{IN} Under Test = 0.8V		Full	-0.5	0.005	0.5	µA
Input Current V_{IN} High, I_{IH}	V_{IN} Under Test = 2.4V		Full	-0.5	0.005	0.5	µA
ANALOG SWITCH							
Analog Signal Range, V_{ANALOG}	I_S = ∓10mA		Full	-15	-	15	V
Drain-Source ON Resistance, $r_{DS(ON)}$	I_S = -10mA, V_D = ±8.5V, V+ = 13.5V, V- = -13.5V		25	-	25	35	Ω
			Full	-	-	45	Ω
Switch OFF Leakage Current, $I_{S(OFF)}$	V+ = 16.5V, V- = -16.5V	V_D = ±15.5V, V_S = ∓15.5V	25	-0.25	±0.1	0.25	nA
			Full	-5	-	+5	nA
Switch OFF Leakage Current, $I_{D(OFF)}$		V_D = ±15.5V, V_S = ∓15.5V	25	-0.25	±0.1	0.25	nA
			Full	-5	-	+5	nA
Channel ON Leakage Current, $I_{D(ON)} + I_{S(ON)}$		$V_S = V_D$ = ±15.5V	25	-0.4	±0.1	0.4	nA
			Full	-10	-	+10	nA

13 SWITCHES

Electrical Specifications Test Conditions: V+ = +15V, V- = -15V, V_L = 5V, V_{IN} = 2.4V, 0.8V (Note 3), Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 4) TEMP (°C)	D SUFFIX -40°C TO 85°C (NOTE 5) MIN	(NOTE 6) TYP	(NOTE 5) MAX	UNITS
POWER SUPPLY CHARACTERISTICS						
Positive Supply Current, I+	V+ = 16.5V, V- = -16.5V, V_{IN} = 0V or 5V	25	-	0.0001	1	µA
		Hot		-	5	µA
Negative Supply Current, I-		25	-1	-0.0001	-	µA
		Hot	-5	-	-	µA
Logic Supply Current, I_L		25	-	0.0001	1	µA
		Hot	-	-	5	µA
Ground Current, I_{GND}		25	-1	-0.0001	-	µA
		Hot	-5	-	-	µA

Electrical Specifications (Unipolar Supplies) Test Conditions: V+ = +12V, V- = 0V, V_L = 5V, V_{IN} = 2.4V, 0.8V (Note 3), Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	(NOTE 4) TEMP (°C)	D SUFFIX -40°C TO 85°C (NOTE 5) MIN	(NOTE 6) TYP	(NOTE 5) MAX	UNITS
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	R_L = 300Ω, C_L = 35pF, V_S = ±8V, (See Figure 7)	25	-	175	250	ns
		Hot	-	-	315	ns
Turn-OFF Time, t_{OFF}		25	-	95	125	ns
		Hot	-	-	140	ns
Break-Before-Make Time Delay	DG413 Only, R_L = 300Ω, C_L = 35pF, V_S = 8V	25	-	25	-	ns
Charge Injection, Q	C_L = 10nF, V_G = 6.0V, R_G = 0Ω	25	-	25	-	pC
ANALOG SWITCH						
Analog Signal Range, V_{ANALOG}		Full	0	-	12	V
Drain-Source ON Resistance, $r_{DS(ON)}$	I_S = -10mA, V_D = 3V, 8V, V+ = 10.8V	25	-	40	80	Ω
		Full	-	-	100	Ω
POWER SUPPLY CHARACTERISTICS						
Positive Supply Current, I+	V+ = 13.2V, V- = 0V, V_{IN} = 0V or 5V	25	-	0.0001	1	µA
		Hot		-	5	µA
Negative Supply Current, I-		25	-1	-0.0001	-	µA
		Hot	-5	-	-	µA
Logic Supply Current, I_L		25	-	0.0001	1	µA
		Hot	-	-	5	µA
Ground Current, I_{GND}		25	-1	-0.0001	-	µA
		Hot	-5	-	-	µA

NOTES:

3. V_{IN} = input voltage to perform proper function.
4. Hot = as determined by the operating temperature suffix.
5. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
6. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Typical Performance Curves

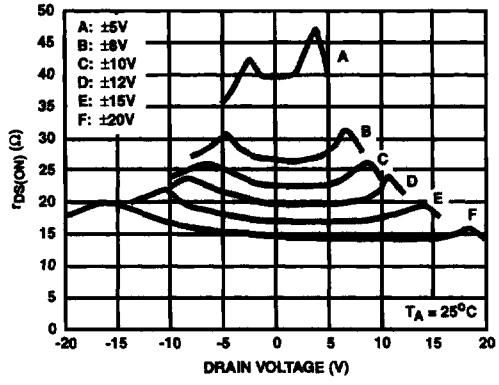


FIGURE 1. ON-RESISTANCE vs V_D AND POWER SUPPLY VOLTAGE

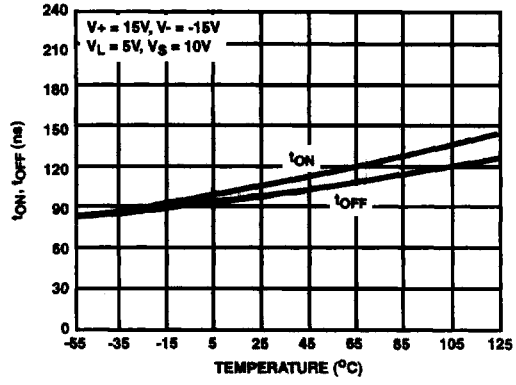


FIGURE 2. SWITCHING TIME vs TEMPERATURE

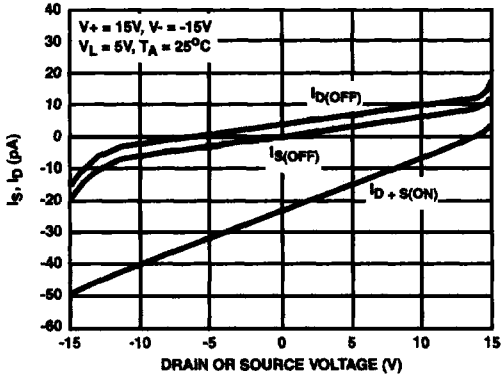


FIGURE 3. LEAKAGE CURRENT vs ANALOG VOLTAGE

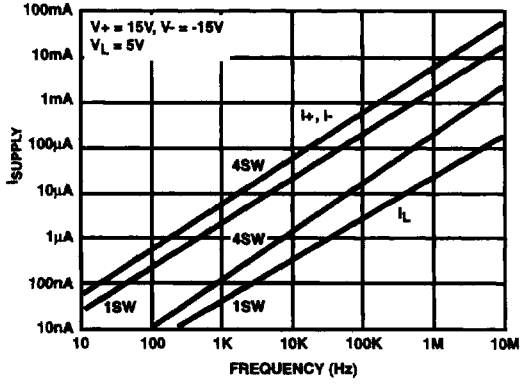


FIGURE 4. SUPPLY CURRENT vs INPUT SWITCHING FREQUENCY

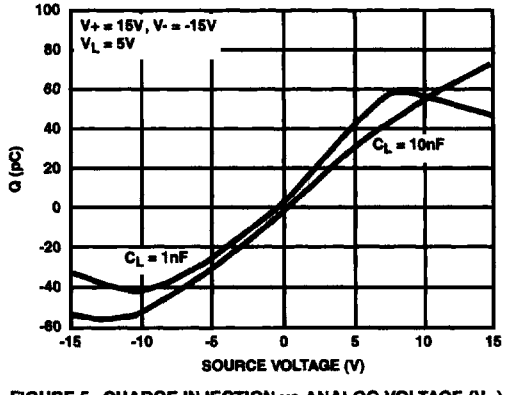


FIGURE 5. CHARGE INJECTION vs ANALOG VOLTAGE (V_D)

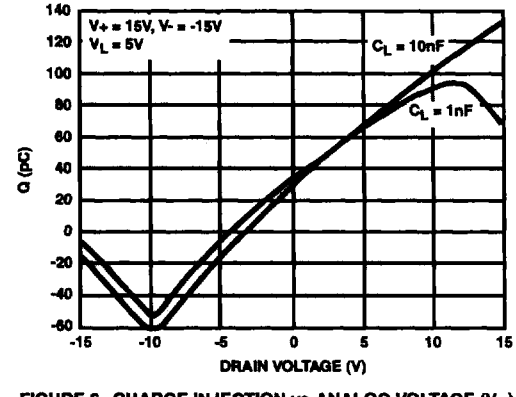


FIGURE 6. CHARGE INJECTION vs ANALOG VOLTAGE (V_S)

13

SWITCHES

Pin Descriptions

PIN	SYMBOL	DESCRIPTION
1	IN_1	Logic Control for Switch 1.
2	D_1	Drain (Output) Terminal for Switch 1.
3	S_1	Source (Input) Terminal for Switch 1.
4	V-	Negative Power Supply Terminal.
5	GND	Ground Terminal (Logic Common).
6	S_4	Source (Input) Terminal for Switch 4.
7	D_4	Drain (Output) Terminal for Switch 4.
8	IN_4	Logic Control for Switch 4.
9	IN_3	Logic Control for Switch 3.
10	D_3	Drain (Output) Terminal for Switch 3.
11	S_3	Source (Input) Terminal for Switch 3.
12	V_L	Logic Reference Voltage.
13	V+	Positive Power Supply Terminal (Substrate).
14	S_2	Source (Input) Terminal for Switch 2.
15	D_2	Drain (Output) Terminal for Switch 2.
16	IN_2	Logic Control for Switch 2.

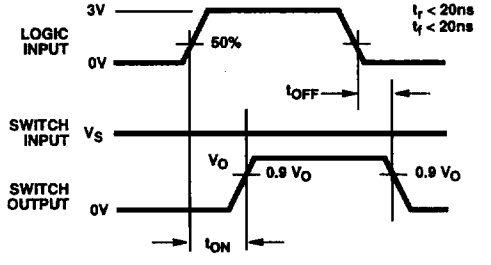
TRUTH TABLE

LOGIC	DG411 SWITCH	DG412 SWITCH	DG413 SWITCH 1, 4	DG413 SWITCH 2, 3
0	ON	OFF	OFF	ON
1	OFF	ON	ON	OFF

NOTE: Logic "0" ≤0.8V. Logic "1" ≥2.4V.

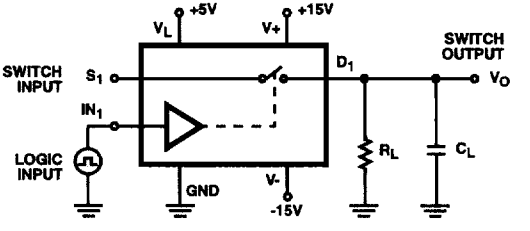
Test Circuits and Waveforms

V_O is the steady state output with the switch on. Feedthrough via switch capacitance may result in spikes at the leading and trailing edge of the output waveform.



NOTE: Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 7A.



Repeat test for all IN and S.
For load conditions, see Specifications C_L (includes fixture and stray capacitance).

$$V_O = V_S \frac{R_L}{R_L + r_{DS(ON)}}$$

FIGURE 7B.

FIGURE 7. SWITCHING TIME

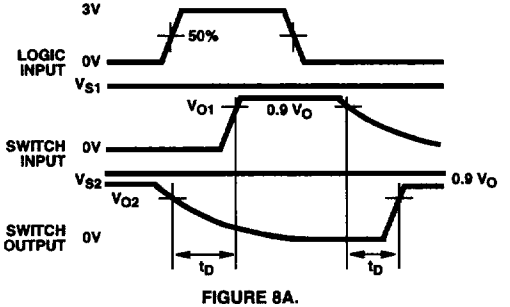


FIGURE 8A.

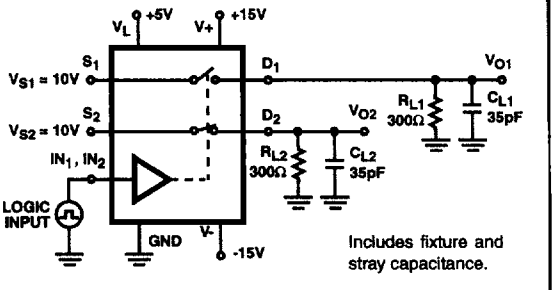


FIGURE 8B.

FIGURE 8. BREAK-BEFORE-MAKE

Test Circuits and Waveforms (Continued)

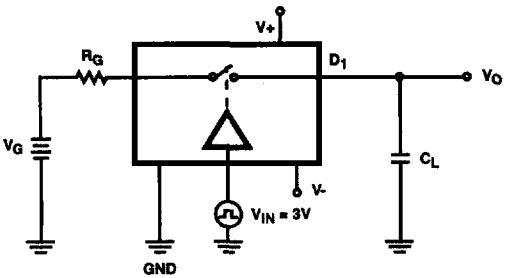
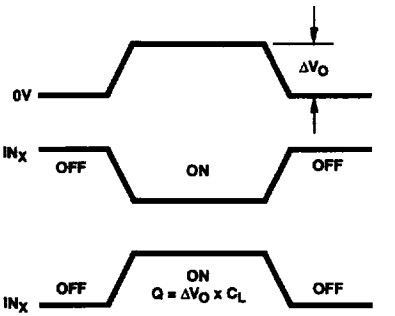


FIGURE 9A.



NOTE: IN_X dependent on switch configuration input polarity determined by sense of switch.

FIGURE 9B.

FIGURE 9. CHARGE INJECTION

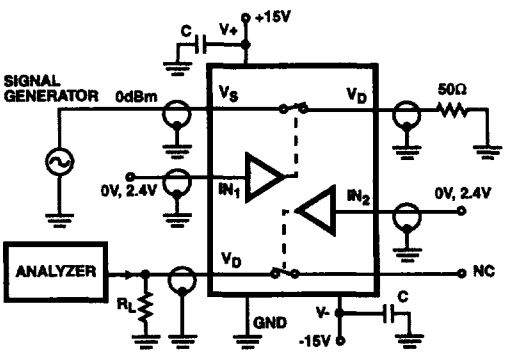


FIGURE 10. CROSSTALK

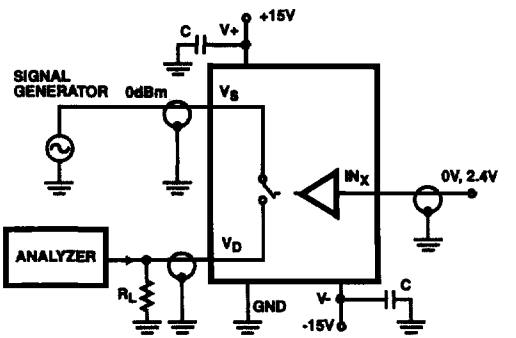


FIGURE 11. OFF ISOLATION

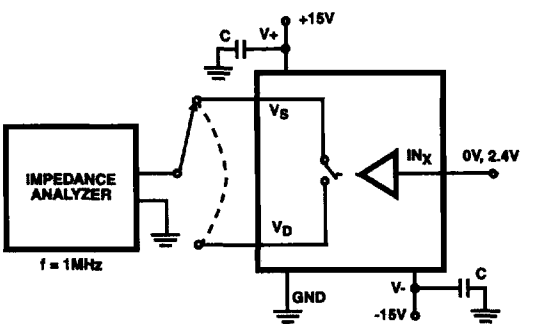


FIGURE 12. SOURCE/DRAIN CAPACITANCES

Typical Applications

Single Supply Operation

The DG411, DG412, DG413 can be operated with unipolar supplies from 5V to 44V. These devices are characterized and tested for unipolar supply operation at 12V to facilitate the majority of applications. To function properly, 12V are tied to Pin 13 and 0V are tied to Pin 4.

NOTE: Pin 12 still requires 5V for TTL compatible switching.

Summing Amplifier

When driving a high impedance, high capacitance load such as shown in Figure 9, where the inputs to the summing amplifier have some noise filtering, it is necessary to have shunt switches for rapid discharge of the filter capacitor, thus preventing offsets from occurring at the output.

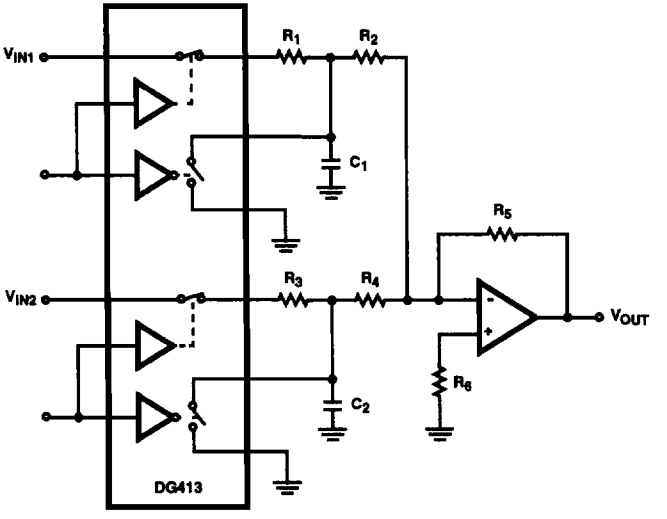


FIGURE 13. SUMMING AMPLIFIER

Die Characteristics

DIE DIMENSIONS:

2760µm x 1780µm x 485µm ±25µm

METALLIZATION:

Type: SiAl
Thickness: 12kÅ ±1kÅ

PASSIVATION:

Type: Nitride
Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY:

1.5×10^5 A/cm^2

Metallization Mask Layout

DG411, DG412, DG413