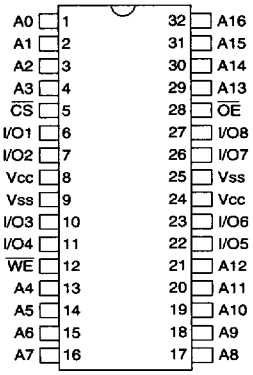
128Kx8 SRAM *ADVANCED**

PIN CONFIGURATION
TOP VIEW



PIN DESCRIPTION

A_{0-16}	Address Inputs
I/O_{0-7}	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	+3.3V Power
V_{SS}	Ground

PLASTIC PLUS™ FEATURES

- Access Times 15, 17, 20ns
- Standard Commercial Off-The-Shelf (COTS) Memory Devices for Extended Temperature Range
- JEDEC Standard 32 pin Plastic 0.4" SOJ Package
- Electrical and Speed Characteristics for:
  - Military Temperature (-55°C to +125°C)
  - Industrial Temperature (-40°C to +85°C)
- Burn-in and Temperature Cycling Available
- Organized as 128K x 8
- Center Power/Ground Pins (Revolutionary)
- 3.3 Volt Power Supply
- Low Power CMOS
- Reliability Test Data Available:
  - High Temperature Operating Life
  - High Temperature Storage
  - Pressure Cooker Test
  - Wet High Temperature Operating Life
  - Thermal Shock
  - Temperature Cycling

* *This data sheet describes a product that may or may not be under development and is subject to change or cancellation without notice.*

PLASTIC PLUS™ SRAM

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature (Mil.)	T_A	-55	+125	°C
Operating Temperature (Ind.)	T_A	-40	+85	°C
Storage Temperature	T_{STG}	-65	+150	°C
Signal Voltage Relative to GND	V_G	-0.5	4.6	V
Supply Voltage	V_{CC}	-0.5	5.5	V

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active
L	H	H	Out Disable	High Z	Active

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	3.0	3.6	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	-0.3	+0.8	V
Operating Temperature (Mil.)	T_A	-55	+125	°C
Operating Temperature (Ind.)	T_A	-40	+85	°C

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Condition	Max	Unit
Input capacitance	C_{IN}	V_{IN} = 0V, f = 1.0MHz	6	pF
Output capacitance	C_{OUT}	V_{OUT} = 0V, f = 1.0MHz	8	pF

This parameter is guaranteed by design but not tested.

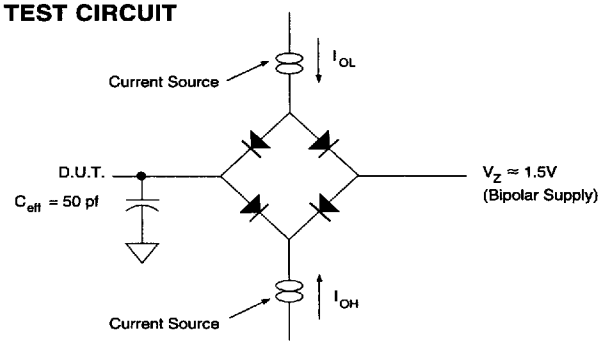
DC CHARACTERISTICS

(V_{CC} = 3.3V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	Min	Max	Units
Input Leakage Current	I_{LI}	V_{CC} = 3.3, V_{IN} = GND to V_{CC}		10	µA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = GND to V_{CC}		10	µA
Operating Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 5MHz, V_{CC} = 3.3		120	mA
Standby Current	I_{SB}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, f = 5MHz, V_{CC} = 3.3		8	mA
Output Low Voltage	V_{OL}	I_{OL} = 8mA		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4mA	2.4		V

SRAM

AC TEST CIRCUIT



AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 2.5	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z_0 = 75 Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

AC CHARACTERISTICS

(VCC = 3.3V, VSS = 0V, TA = -55°C to +125°C)

Parameter Read Cycle	Symbol	-15		-17		-20		Units
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	15		17		20		ns
Address Access Time	tAA		15		17		20	ns
Output Hold from Address Change	tOH	0		0		0		ns
Chip Select Access Time	tACS		15		17		20	ns
Output Enable to Output Valid	tOE		10		11		12	ns
Chip Select to Output in Low Z	tCLZ1	3		3		3		ns
Output Enable to Output in Low Z	tOLZ1	2		2		2		ns
Chip Disable to Output in High Z	tCHZ1		8		9		10	ns
Output Disable to Output in High Z	tOHZ1		8		9		10	ns

1. This parameter is guaranteed by design but not tested.

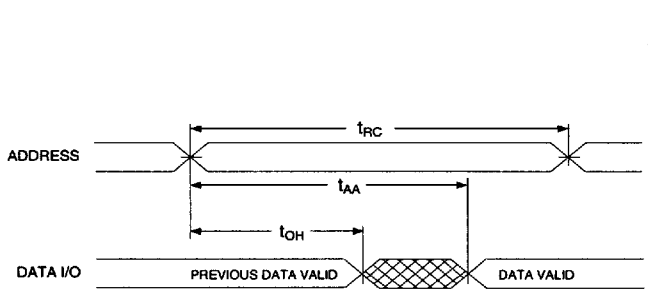
AC CHARACTERISTICS

(VCC = 3.3V, TA = -55°C to +125°C)

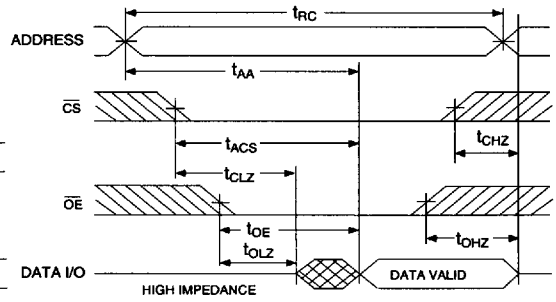
Parameter Write Cycle	Symbol	-15		-17		-20		Units
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	15		17		20		ns
Chip Select to End of Write	tCW	13		14		15		ns
Address Valid to End of Write	tAW	13		14		15		ns
Data Valid to End of Write	tDW	10		11		12		ns
Write Pulse Width	tWP	13		14		15		ns
Address Setup Time	tAS	0		0		0		ns
Address Hold Time	tAH	0		0		0		ns
Output Active from End of Write	tOW1	3		4		5		ns
Write Enable to Output in High Z	tWHZ1		8		8		10	ns
Data Hold Time	tDH	0		0		0		ns

1. This parameter is guaranteed by design but not tested.

TIMING WAVEFORM - READ CYCLE

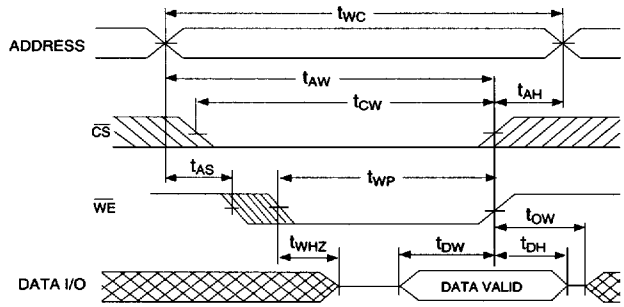


READ CYCLE 1 ($\overline{CS}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH})



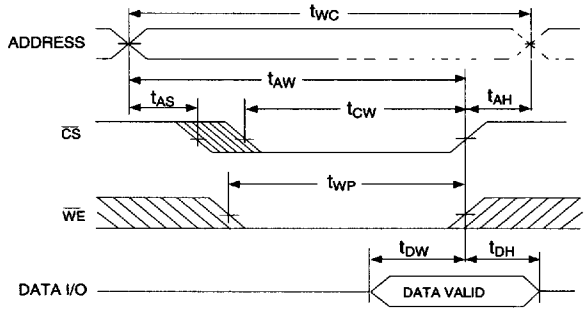
READ CYCLE 2 ($\overline{WE}$ = V_{IH})

WRITE CYCLE - $\overline{WE}$ CONTROLLED



WRITE CYCLE 1, $\overline{WE}$ CONTROLLED

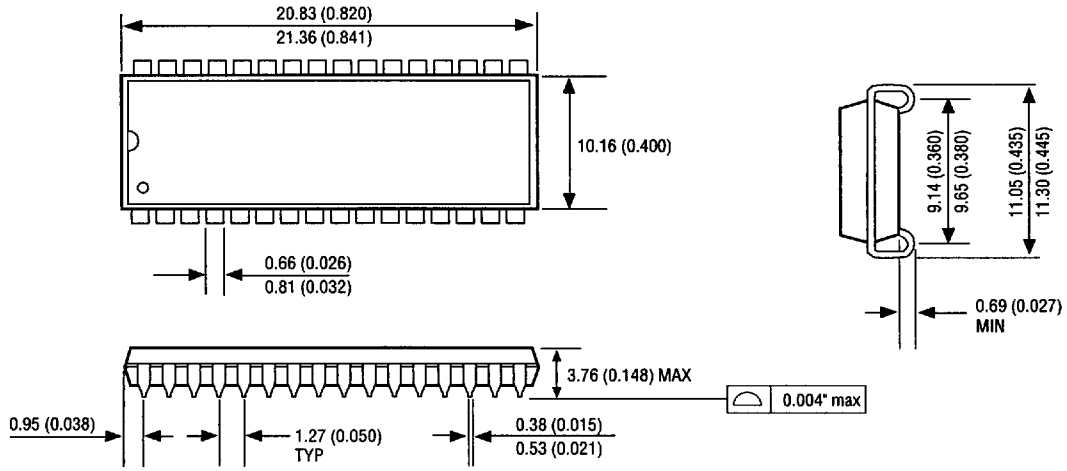
WRITE CYCLE - $\overline{CS}$ CONTROLLED



WRITE CYCLE 2, $\overline{CS}$ CONTROLLED

SRAM

PACKAGE DIMENSION



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION

W P S 128K 8 V X - XXX RJ X X

- **SPECIAL PROCESS:**
  - Blank = CMOS
  - B = Bi CMOS
- **DEVICE GRADE:**
  - M = Military Temperature -55°C to +125°C
  - I = Industrial Temperature -40°C to +85°C
- **PACKAGE:**
  - RJ = Revolutionary SOJ
- **ACCESS TIME (ns)**
- **IMPROVEMENT MARK**
  - B = Burn-in
  - T = Temperature Cycling
  - C = Burn-in and Temperature Cycle
- **Low Voltage Supply 3.3V ± 10%**
- **ORGANIZATION, 128K x 8**
- **SRAM**
- **PLASTIC PLUS™**
- **WHITE MICROELECTRONICS**

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