SRAM MODULE

256K x 32 SRAM

FEATURES
- High speed: 15, 20 and 25ns
- High-density 1MB design
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ functions
- Industry-standard pinout
- All inputs and outputs are TTL-compatible
- Low profile

OPTIONS   MARKING
- Timing
  - 15ns access   -15
  - 20ns access   -20
  - 25ns access   -25
- Packages
  - 64-pin SIMM   M
  - 64-pin ZIP   Z
- 2V data retention (optional)   L
- 2V data retention, low power (optional) LP
- Part Number Example: MT8S25632Z-15 L

NOTE: Not all combinations of speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

GENERAL DESCRIPTION

The MT8S25632 is a high-speed SRAM memory module containing 262,144 words organized in a x32-bit configuration. The module consists of eight 256K x 4 fast SRAMs mounted on a 64-pin, double-sided, FR4-printed circuit board.

Data is written into the SRAM memory when write enable ($\overline{WE}$) and chip enable ($\overline{CE}$) inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and output enable ($\overline{OE}$) are LOW. $\overline{CE}$ and/or $\overline{OE}$ can set the output in High-Z for additional flexibility in system design and memory expansion.

PD0 and PD1 identify the module's density allowing interchangeable use of alternate density, industry standard modules. Four chip enable inputs, ($\overline{CE1}$, $\overline{CE2}$, $\overline{CE3}$ and $\overline{CE4}$) are used to enable the module's 4 bytes independently.

The Micron SRAM family uses a high-speed, low-power CMOS design in a four-transistor memory cell featuring double-layer metal, double-layer polysilicon technology.

PIN ASSIGNMENT (Top View)

64-Pin SIMM (SE3)
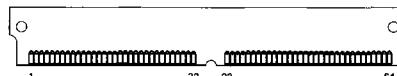
64-Pin ZIP (SG-1)
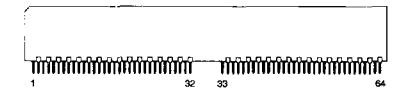
PIN #	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	Vss	17	A2	33	$\overline{CE4}$	49	A4
2	PD0	18	A9	34	$\overline{CE3}$	50	A11
3	PD1	19	DQ13	35	A17	51	A5
4	DQ1	20	DQ5	36	A16	52	A12
5	DQ9	21	DQ14	37	$\overline{OE}$	53	Vcc
6	DQ2	22	DQ6	38	Vss	54	A13
7	DQ10	23	DQ15	39	DQ25	55	A6
8	DQ3	24	DQ7	40	DQ17	56	DQ21
9	DQ11	25	DQ16	41	DQ26	57	DQ29
10	DQ4	26	DQ8	42	DQ18	58	DQ22
11	DQ12	27	Vss	43	DQ27	59	DQ30
12	Vcc	28	$\overline{WE}$	44	DQ19	60	DQ23
13	A0	29	A15	45	DQ28	61	DQ31
14	A7	30	A14	46	DQ20	62	DQ24
15	A1	31	$\overline{CE2}$	47	A3	63	DQ32
16	A8	32	$\overline{CE1}$	48	A10	64	Vss

All module components may be powered from a single +5V supply and all inputs and outputs are fully TTL-compatible.

The "L" and "LP" versions each provide a 70 percent reduction in CMOS standby current (I_{SB2}) over the standard version. The "LP" version also provides a 90 percent reduction in TTL standby current (I_{SB1}) through the use of gated inputs on the $\overline{WE}$, $\overline{OE}$ and address lines, which also facilitates the design of battery backed systems. That is, the gated inputs simplify the design effort and circuitry required to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

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FUNCTIONAL BLOCK DIAGRAM

PRESENCE-DETECT   U1-U8 = MT5C1005DJ
PD0 = Vss
PD1 = Vss
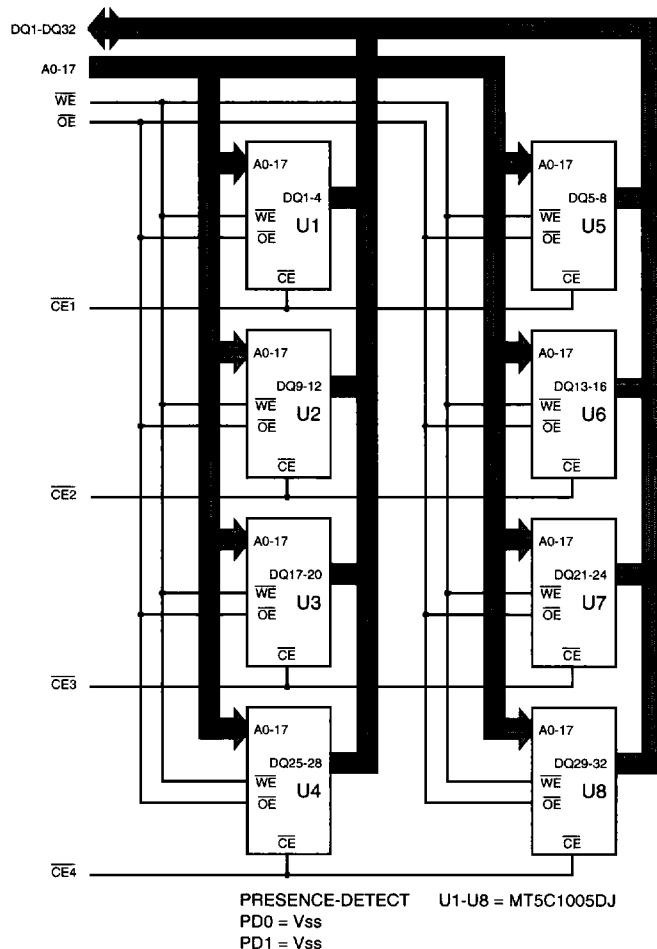
TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -1V to +7V
Storage Temperature .... -55°C to +125°C
Power Dissipation 8W
Short Circuit Output Current 50mA
Voltage on Any Pin Relative to Vss .... -1V to Vcc +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage			V_{IH}	2.2	Vcc+1	V	1
Input Low (Logic 0) Voltage			V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ Vcc	A0-A17, $\overline{WE}$, $\overline{OE}$	I_{LI1}	-40	40	μA	
		$\overline{CE1}$-$\overline{CE4}$	I_{LI2}	-10	10	μA	
Input/Output Leakage Current	Output(s) disabled 0V ≤ V_{OUT} ≤ Vcc	DQ1-DQ32	I_{LO}	-5	5	μA	
Output High Voltage	I_{OH} = -4.0mA		V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA		V_{OL}		0.4	V	1
Supply Voltage			Vcc	4.5	5.5	V	1

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX			UNITS	NOTES
				-15	-20	-25		
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; Vcc = MAX f = MAX = 1/^{t}RC outputs open	Icc	856	1,560	1,280	1,160	mA	3, 13
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; Vcc = MAX f = MAX = 1/^{t}RC outputs open	I_{SB1}	296	600	440	400	mA	13
	LP version only	I_{SB1}	10.4	24	24	24	mA	13
	$\overline{CE}$ ≥ Vcc -0.2V; Vcc = MAX V_{IN} ≤ Vss +0.2V or V_{IN} ≥ Vcc -0.2V; f = 0	I_{SB2}	3.2	40	40	40	mA	13
	L and LP versions only	I_{SB2}	2.4	12	12	12	mA	13

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance; A0-A17, $\overline{WE}$, $\overline{OE}$	T_A = 25°C; f = 1 MHz Vcc = 5V	C_{I1}	60	pF	4
Input Capacitance; $\overline{CE1}$-$\overline{CE4}$		C_{I2}	15	pF	4
Input/Output Capacitance: DQ1-DQ32		$C_{I/O}$	10	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) ($0°C \le T_A \le 70°C$; Vcc = 5V ±10%)

DESCRIPTION	SYM	-15 MIN	-15 MAX	-20 MIN	-20 MAX	-25 MIN	-25 MAX	UNITS	NOTES
READ Cycle									
READ cycle time	t_{RC}	15		20		25		ns	
Address access time	t_{AA}		15		20		25	ns	
Chip Enable access time	t_{ACE}		15		20		25	ns	
Output hold from address change	t_{OH}	3		3		5		ns	
Chip Enable to output in Low-Z	t_{LZCE}	5		5		5		ns	7
Chip disable to output in High-Z	t_{HZCE}		6		8		10	ns	6, 7
Chip Enable to power-up time	t_{PU}	0		0		0		ns	
Chip disable to power-down time	t_{PD}		15		20		25	ns	
Output Enable access time	t_{AOE}		6		6		8	ns	
Output Enable to output in Low-Z	t_{LZOE}	0		0		0		ns	
Output disable to output in High-Z	t_{HZOE}		5		6		10	ns	6
WRITE Cycle									
WRITE cycle time	t_{WC}	15		20		25		ns	
Chip Enable to end of write	t_{CW}	10		12		15		ns	
Address valid to end of write	t_{AW}	10		12		15		ns	
Address setup time	t_{AS}	0		0		0		ns	
Address hold from end of write	t_{AH}	0		0		0		ns	
WRITE pulse width	t_{WP1}	9		12		15		ns	
WRITE pulse width	t_{WP2}	12		15		15		ns	
Data setup time	t_{DS}	7		8		10		ns	
Data hold time	t_{DH}	0		0		0		ns	
Write disable to output in Low-Z	t_{LZWE}	3		3		3		ns	7
Write Enable to output in High-Z	t_{HZWE}		6		8		10	ns	6, 7

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AC TEST CONDITIONS

|	
Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2
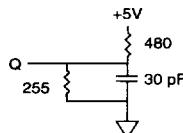
Fig. 1 OUTPUT LOAD EQUIVALENT
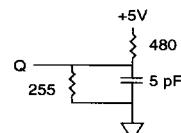

Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < $^tRC/2$.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^tHZCE, ^tHZOE and ^tHZWE are specified with C_L = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^tHZCE is less than ^tLZCE and ^tHZWE is less than ^tLZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^tRC=Read Cycle Time
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Typical values are measured at 5V, 25°C and 25ns cycle time.
14. Typical values are measured at 25°C.

## DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP Versions Only)

| DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			V_{DR}	2			V	
Data Retention Current L Version	$\overline{CE}$ ≥ (Vcc -0.2V) V_{IN} ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	I_{CCDR}		280	1,200	μA	14
		Vcc = 3V			480	2,000	μA	14
Data Retention Current LP Version	$\overline{CE}$ ≥ (Vcc -0.2V)	Vcc = 2V	I_{CCDR}		280	1,200	μA	14
		Vcc = 3V	I_{CCDR}		240	2,000	μA	14
Chip Deselect to Data Retention Time			^tCDR	0			ns	4
Operation Recovery Time			^tR	^tRC			ns	4,11

LOW Vcc DATA-RETENTION WAVEFORM
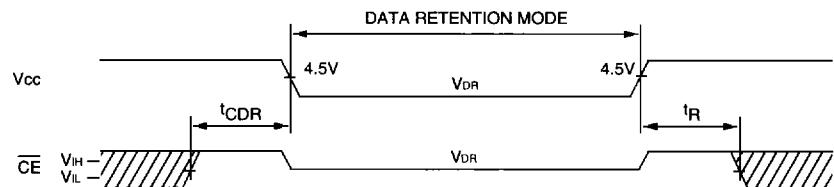
READ CYCLE NO. 1 [8, 9]
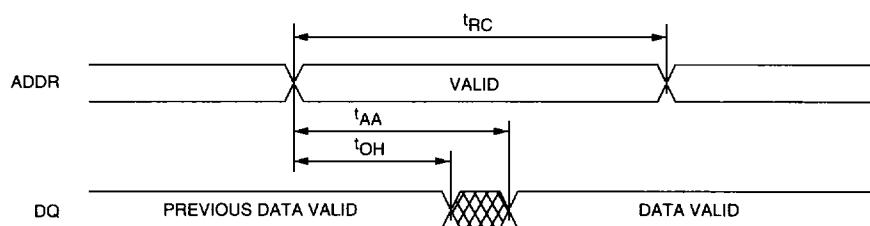
READ CYCLE NO. 2 [7, 8, 10]
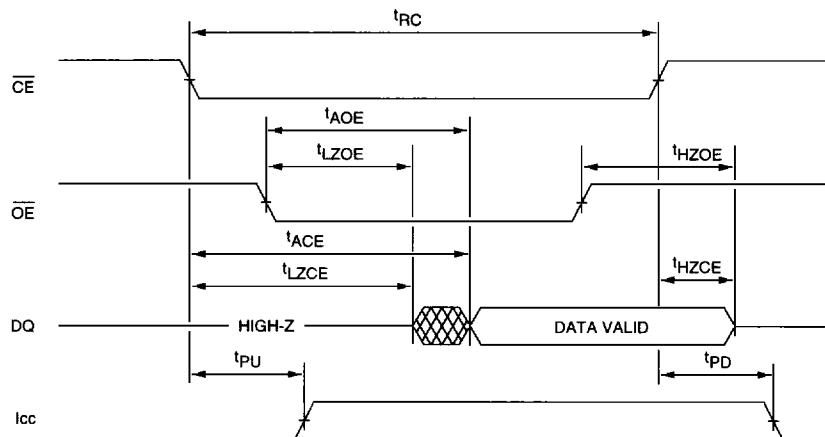
## WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)
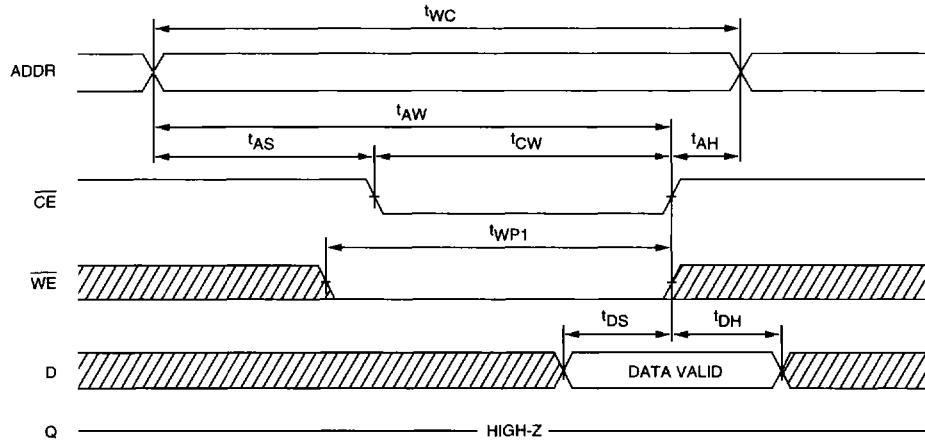
WRITE CYCLE NO. 2 [12]
(Write Enable Controlled)
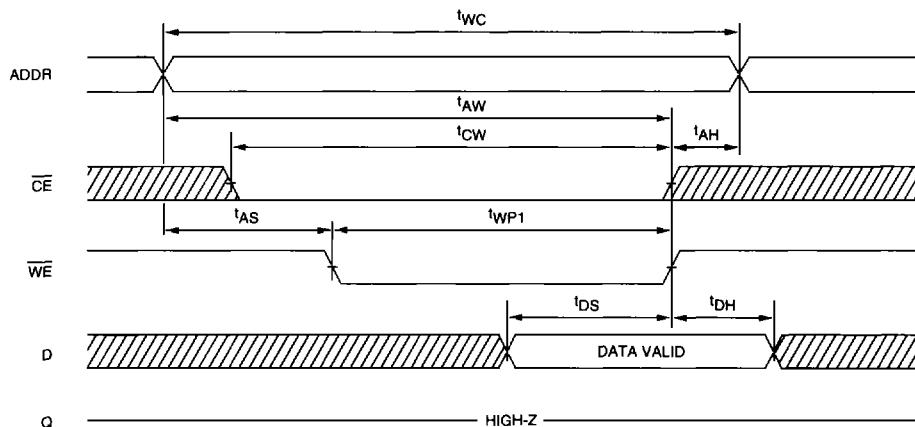
▨ DON'T CARE

▨ UNDEFINED

NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

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WRITE CYCLE NO. 3 [7, 12]
(Write Enable Controlled)

Legend:
- ⧄ DON'T CARE
- ⧅ UNDEFINED
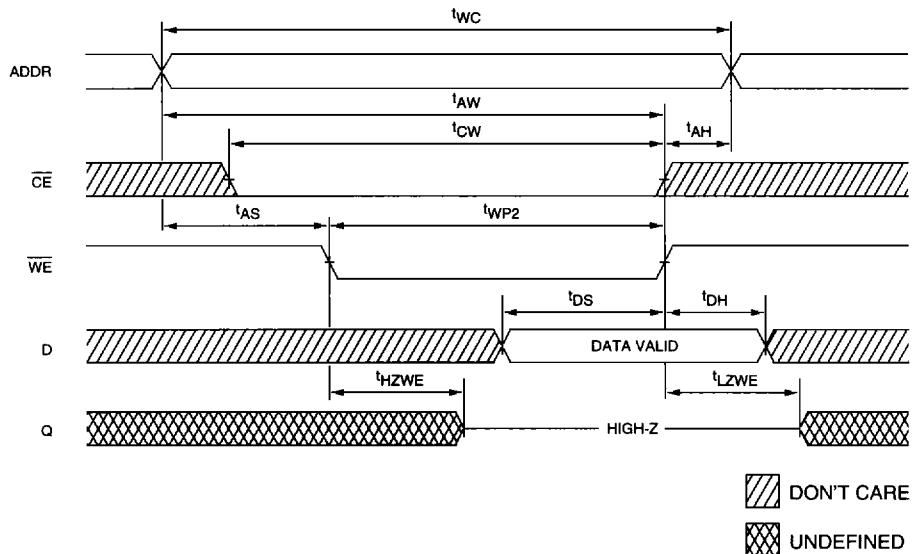
NOTE: Output enable ($\overline{OE}$) is active (LOW).