SRAM

256K x 1 SRAM

FEATURES

- High speed: 10*, 12*, 15, 20, 25 and 35ns
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ option
- All inputs and output are TTL compatible

OPTIONS — MARKING

- Timing

10ns access	-10*
12ns access	-12*
15ns access	-15
20ns access	-20
25ns access	-25
35ns access	-35

- Packages

Plastic DIP (300 mil)	None
Plastic SOJ (300 mil)	DJ

NOTE: Available in ceramic packages tested to meet military specifications. Please refer to Micron's *Military Data Book*.

• 2V data retention	L
• 2V data retention, low power	LP

- Temperature

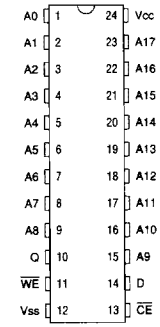
Industrial	(-40°C to +85°C)	IT
Automotive	(-40°C to +125°C)	AT
Extended	(-55°C to +125°C)	XT

- Part Number Example: MT5C2561DJ-15 LP IT

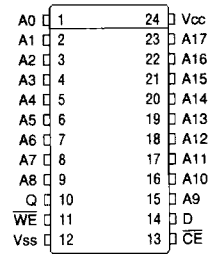
*Preliminary

PIN ASSIGNMENT (Top View)

24-Pin DIP
(SA-3)



24-Pin SOJ
(SD-1)



GENERAL DESCRIPTION

The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

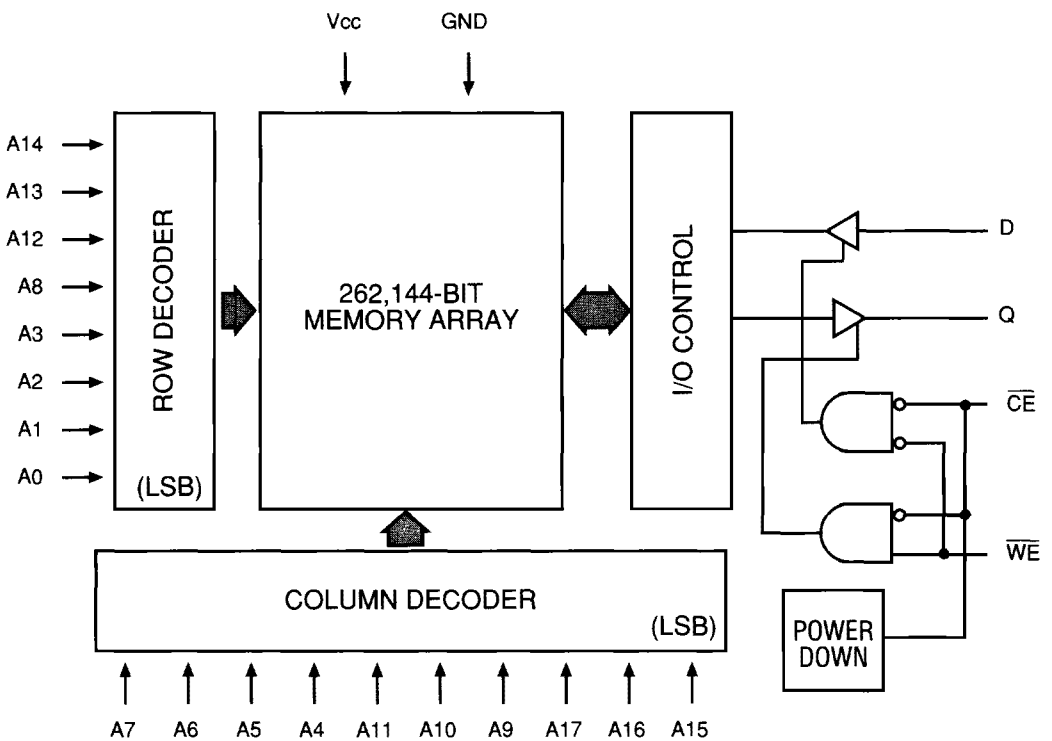
For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) with all organizations. This enhancement can place the outputs in High-Z for additional flexibility in system design. The x1 configuration features separate data input and output.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

The "LP" version provides a reduction in both operating current (I_{CC}) and TTL standby current (I_{SB1}). The latter is achieved through the use of gated inputs on the $\overline{WE}$ and address lines, which also facilitates the design of battery backed systems. That is, the gated inputs simplify the design effort and circuitry required to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	OUTPUT	POWER
STANDBY	H	X	HIGH-Z	STANDBY
READ	L	H	Q	ACTIVE
WRITE	L	L	HIGH-Z	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA
Voltage on any pin relative to V_{SS} ..... -1V to V_{CC} +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

				MAX							
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-10+†	-12+†	-15†	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{CC}	85	180	160	140	120	110	90	mA	3, 14
	"LP" VERSION	I_{CC}	65	-	-	-	110	100	80	mA	3, 14
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{SB1}	11	45	40	30	30	25	25	mA	14
	"LP" VERSION	I_{SB1}	3	-	-	-	7	7	7	mA	14
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	0.6	5	5	5	5	5	7	mA	14

+Preliminary
† LP version not available with this speed.

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz V_{CC} = 5V	C_I	6	pF	4
Output Capacitance		C_O	5	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION		-10*		-12*		-15		-20		-25		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle															
READ cycle time	tRC	10		12		15		20		25		35		ns	
Address access time	tAA		10		12		15		20		25		35	ns	
Chip Enable access time	tACE		10		12		15		20		25		35	ns	
Output hold from address change	tOH	2		3		3		3		5		5		ns	
Chip Enable to output in Low-Z	tLZCE	3		4		4		4		6		6		ns	7
Chip disable to output in High-Z	tHZCE		6		8		8		9		9		15	ns	6, 7
Chip Enable to power-up time	tPU	0		0		0		0		0		0		ns	
Chip disable to power-down time	tPD		10		12		15		20		25		35	ns	
WRITE Cycle															
WRITE cycle time	tWC	10		12		15		20		25		30		ns	
Chip Enable to end of write	tCW	9		10		10		15		15		20		ns	
Address valid to end of write	tAW	9		10		10		15		15		20		ns	
Address setup time	tAS	0		0		0		0		0		0		ns	
Address hold from end of write	tAH	0		0		0		0		0		0		ns	
WRITE pulse width	tWP	9		10		10		15		15		20		ns	
Data setup time	tDS	6		7		7		10		10		15		ns	
Data hold time	tDH	0		0		0		0		0		0		ns	
Write disable to output in Low-Z	tLZWE	3		4		4		4		5		5		ns	7
Write Enable to output in High-Z	tHZWE		6		7		7		10		10		15	ns	6, 7

*Preliminary

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

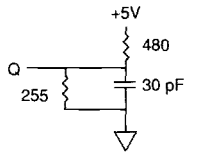


Fig. 1 OUTPUT LOAD EQUIVALENT

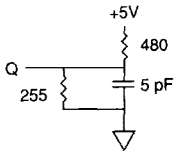


Fig. 2 OUTPUT LOAD EQUIVALENT

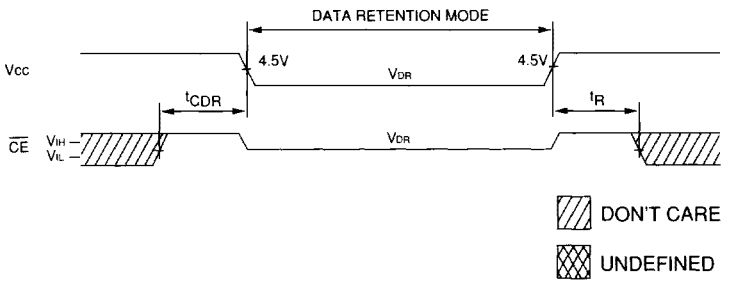
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE, and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Refer to the IT/XT/AT section of Micron's *SRAM Data Book* for applicable non-commercial temperature range specifications.
14. Typical values are measured at 5V, 25°C and 20ns cycle time.

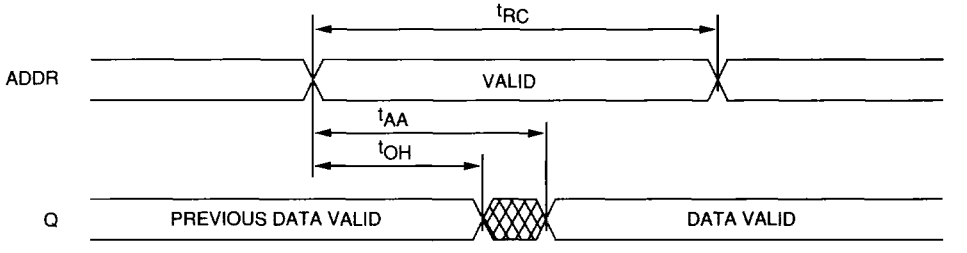
DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP Versions Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			V_{DR}	2			V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	I_{CCDR}		35	300	µA	
		Vcc = 3V	I_{CCDR}		90	500	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0			ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

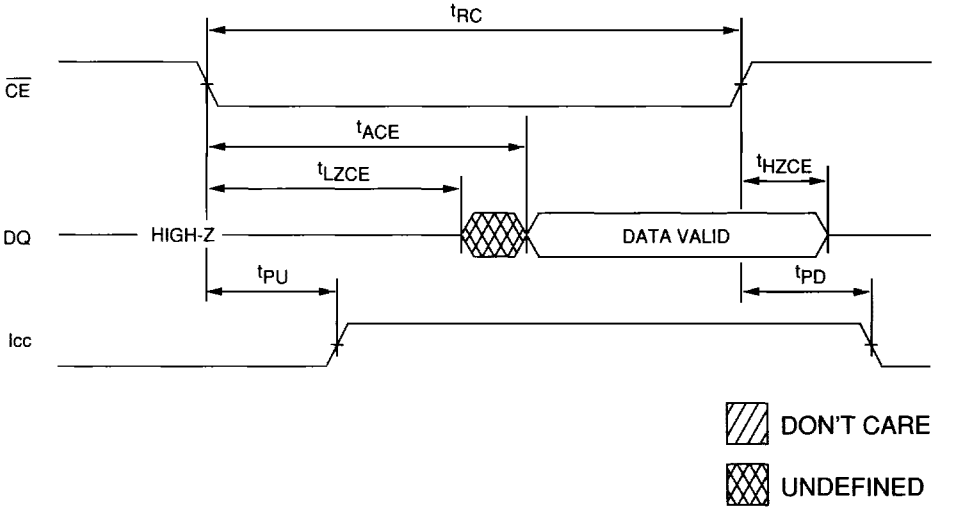
LOW Vcc DATA RETENTION WAVEFORM



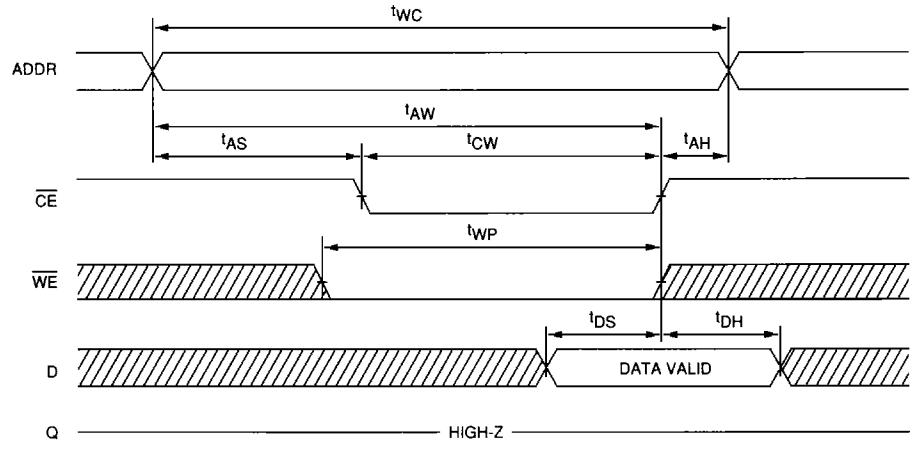
READ CYCLE NO. 1 [8, 9]



READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)



WRITE CYCLE NO. 2 [7, 12]
(Write Enable Controlled)