DESCRIPTION:

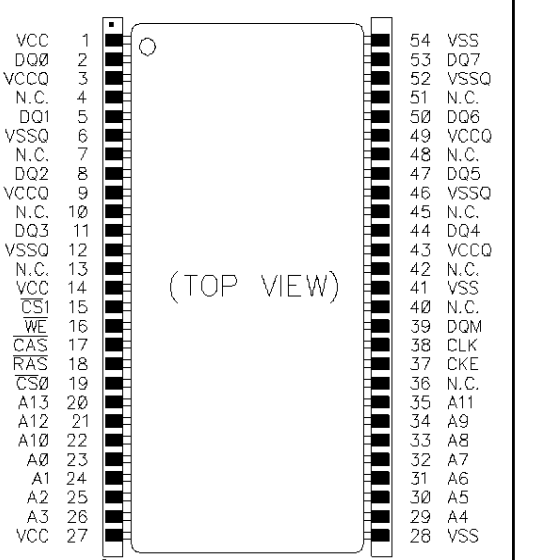
The *M-Densus* series is a family of interchangeable memory modules. The 128 Megabit SDRAM is a member of this family which utilizes the new and innovative space saving TSOP stacking technology. The modules are constructed with 8 Meg x 8 SDRAMs.

This 64 Megabit based *M-Densus* module, the DPSD16MX8RKY5 has been designed to fit in the same footprint as the 8 Meg x 8 SDRAM TSOP monolithic and 64 Megabit SDRAM based family of *M-Densus* modules. This allows the memory board designer to upgrade the memory in their products without redesigning the memory board, thus saving time and money.

FEATURES:

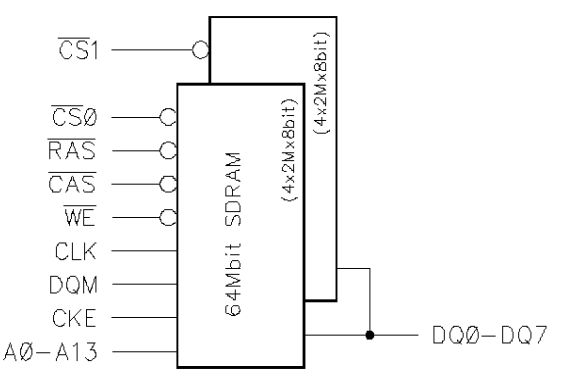
- Configuration Available:
  16 Meg x 8 (2 banks of 2M x 4 x 8 bits)
- Clock Frequency: 83, 100 MHz (max.)
- 3.3V Supply
- LVTTL Compatible I/O
- Four Bank Operation
- Programmable Burst Type, Burst Length, and CAS Latency
- 4096 Cycles / 64 ms
- Auto and Self Refresh
- Package: TSOP Leadless Stack

PIN-OUT DIAGRAM



PIN NAMES	
A0 - A13	Row Address: A0 - A11 Column Address: A0 - A9 Bank Select: A12, A13
DQ0 - DQ7	Data In / Data Out
$\overline{CAS}$	Column Address Strobes
$\overline{RAS}$	Row Address Enables
$\overline{WE}$	Data Write Enable
DQM	Data Input/Output Mask
CKE	Clock Enable
CLK	System Clock
$\overline{CS0}$, $\overline{CS1}$	Chip Selects
V_{CC}/V_{SS}	Power Supply/Ground
V_{CCQ}/V_{SSQ}	Data Output Power/Ground
N.C.	No Connect

FUNCTIONAL BLOCK DIAGRAM

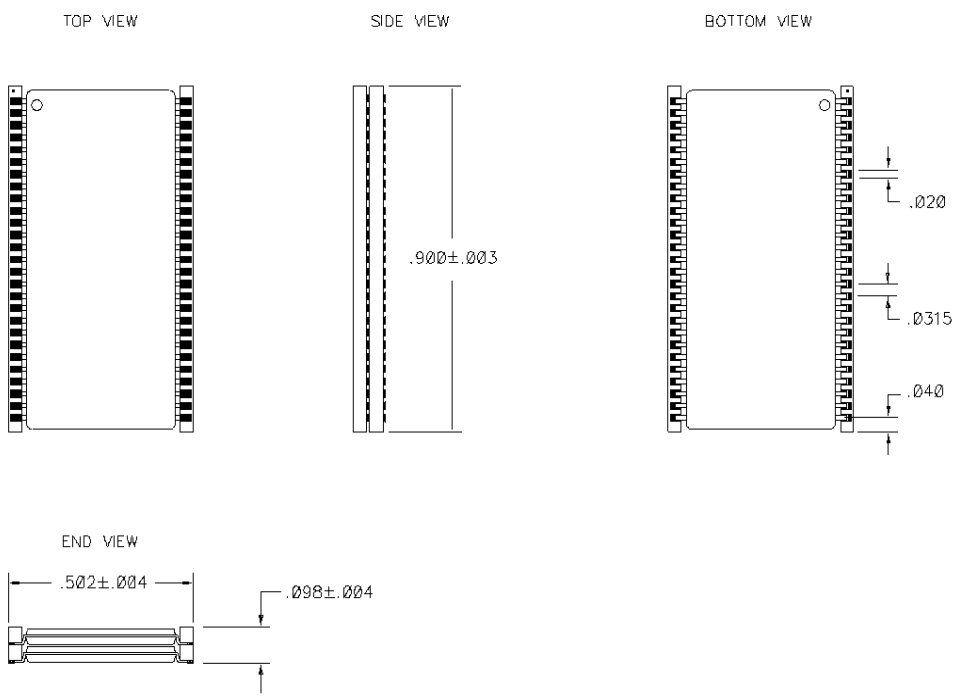


ORDERING INFORMATION

DP	S	D	16M	X	8	R	KY5	–	nn	C
PREFIX	DESIG	TYPE	MEMORY DEPTH	DESIG	MEMORY WIDTH	DESIG	PACKAGE		SPEED	GRADE

- GRADE: C — COMMERCIAL 0°C to +70°C
- SPEED: 10 — 10ns (100MHz); 12 — 12ns (83MHz)
- PACKAGE: KY5 — SPECIAL STACKABLE TSOP (T-STACK)
- DESIG: R — 64 MEGABIT BASED
- MEMORY WIDTH: 8 — MEMORY MODULE WITHOUT SUPPORT LOGIC
- DESIG: X — CMOS DRAM
- TYPE: D — SYNCHRONOUS
- MEMORY DEPTH: 16M
- DESIG: S
- PREFIX: DP

MECHANICAL DRAWING



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