

### DESCRIPTION:

The DPS512S8EJ4/EL4/RJ4/RL4 surface mount SRAM modules are a revolutionary memory subsystems using Dense-Pac Microsystems' new 2nd Generation Stacking Technology. The module combines four Stackable Chip Carriers (SCC), each containing a 128Kx8 SRAM die, integrated into an encapsulated leaded substrate with decoder logic. The complete module assembly is fully compatible with the JEDEC Standard fast 512Kx8 SRAM monolithics in 32 pin or 36 pin, 400-mil wide surface mount packages.

By using SCCs, the 2nd Generation Stack family of modules offers a higher board density of memory than available with conventional through-hole, surface mount, module, or hybrid techniques.

### APPLICATION NOTE:

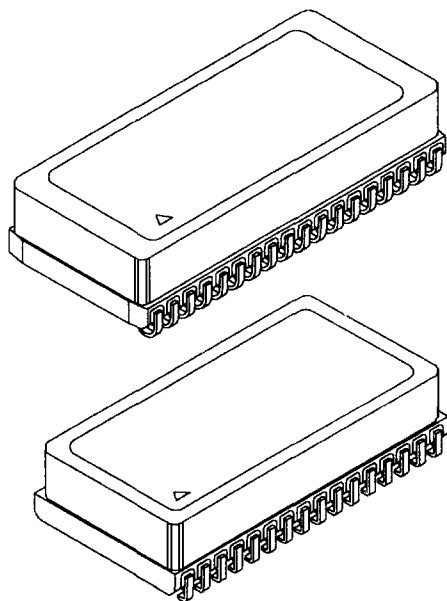
This device has internal solder connections that will reflow at temperatures above 231°C. This temperature should not be exceeded during initial soldering to the PCB, or during any removal process from the PCB.

### FEATURES:

- Organization: 524,288 by 8 bit configuration
- Fast Access Times: 20\*, 25, 30, 35, 45ns (max.)
- TTL Compatible Inputs and Outputs
- Common I/O with Three State Outputs
- Fully Static Operation - No Clock or Refresh
- Fully Compatible with 512Kx8 SRAM Monolithics
- 400 mil Surface Mount Packages

- Available Packages:  
Evolutionary 32-Pin:  
    'J' Leaded Stack  
    'L' Leaded Stack  
Revolutionary 36-Pin:  
    'J' Leaded Stack  
    'L' Leaded Stack

\* Available in Commercial Only.



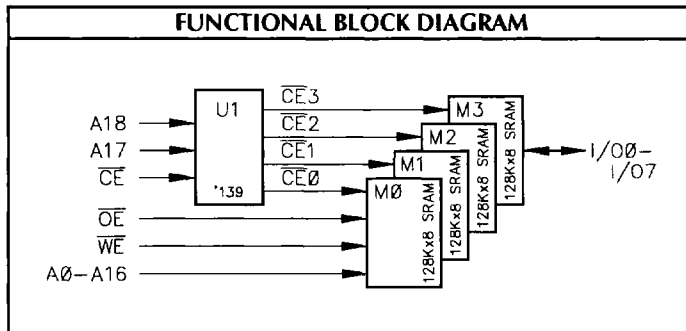
**PIN-OUT DIAGRAM  
(32-Pin Evolutionary)**

|      |    |    |                 |
|------|----|----|-----------------|
| A18  | 1  | 32 | VDD             |
| A16  | 2  | 31 | A15             |
| A14  | 3  | 30 | A17             |
| A12  | 4  | 29 | $\overline{WE}$ |
| A7   | 5  | 28 | A13             |
| A6   | 6  | 27 | A8              |
| A5   | 7  | 26 | A9              |
| A4   | 8  | 25 | A11             |
| A3   | 9  | 24 | $\overline{OE}$ |
| A2   | 10 | 23 | A10             |
| A1   | 11 | 22 | $\overline{CE}$ |
| A0   | 12 | 21 | I/O7            |
| I/O0 | 13 | 20 | I/O6            |
| I/O1 | 14 | 19 | I/O5            |
| I/O2 | 15 | 18 | I/O4            |
| VSS  | 16 | 17 | I/O3            |

**PIN-OUT DIAGRAM  
(36-Pin Revolutionary)**

|                 |    |    |                 |
|-----------------|----|----|-----------------|
| A0              | 1  | 36 | N.C.            |
| A1              | 2  | 35 | A18             |
| A2              | 3  | 34 | A17             |
| A3              | 4  | 33 | A16             |
| A4              | 5  | 32 | A15             |
| $\overline{CE}$ | 6  | 31 | $\overline{OE}$ |
| I/O0            | 7  | 30 | I/O7            |
| I/O1            | 8  | 29 | I/O6            |
| VDD             | 9  | 28 | VSS             |
| VSS             | 10 | 27 | VDD             |
| I/O2            | 11 | 26 | I/O5            |
| I/O3            | 12 | 25 | I/O4            |
| $\overline{WE}$ | 13 | 24 | A14             |
| A5              | 14 | 23 | A13             |
| A6              | 15 | 22 | A12             |
| A7              | 16 | 21 | A11             |
| A8              | 17 | 20 | A10             |
| A9              | 18 | 19 | N.C.            |

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

|                 |                   |
|-----------------|-------------------|
| A0 - A18        | Address Inputs    |
| I/O0 - I/O7     | Data Input/Output |
| $\overline{CE}$ | Chip Enable       |
| $\overline{WE}$ | Write Enable      |
| $\overline{OE}$ | Output Enable     |
| $V_{DD}$        | Power (+5.0V)     |
| $V_{SS}$        | Ground            |
| N.C.            | No Connect        |

RECOMMENDED OPERATING RANGE<sup>1</sup>

| Symbol          | Characteristic        |    | Min.              | Typ. | Max.                 | Unit |
|-----------------|-----------------------|----|-------------------|------|----------------------|------|
| V <sub>DD</sub> | Supply Voltage        |    | 4.5               | 5.0  | 5.5                  | V    |
| V <sub>IH</sub> | Input HIGH Voltage    |    | 2.2               |      | V <sub>DD</sub> +0.3 | V    |
| V <sub>IL</sub> | Input LOW Voltage     |    | -0.5 <sup>2</sup> |      | 0.8                  | V    |
| T <sub>A</sub>  | Operating Temperature | C  | 0                 | +25  | +70                  | °C   |
|                 |                       | CI | -40               | -25  | +85                  |      |

TRUTH TABLE

| Mode         | $\overline{CE}$ | $\overline{WE}$ | $\overline{OE}$ | I/O Pin | Supply Current |
|--------------|-----------------|-----------------|-----------------|---------|----------------|
| Not Selected | H               | X               | X               | HIGH-Z  | Standby        |
| DOUT Disable | L               | H               | H               | HIGH-Z  | Active         |
| Read         | L               | H               | L               | DOUT    | Active         |
| Write        | L               | L               | X               | DIN     | Active         |

H = HIGH

L = LOW

X = Don't Care

DC OUTPUT CHARACTERISTICS

| Symbol   | Parameter    | Conditions               | Min. | Max. | Unit |
|----------|--------------|--------------------------|------|------|------|
| $V_{IH}$ | HIGH Voltage | $I_{OH} = -4.0\text{mA}$ | 2.4  | -    | V    |
| $V_{IL}$ | LOW Voltage  | $I_{OL} = 8.0\text{mA}$  |      | 0.4  | V    |

ABSOLUTE MAXIMUM RATINGS<sup>3</sup>

| Symbol     | Parameter                         | Max.                   | Unit |
|------------|-----------------------------------|------------------------|------|
| $T_{STC}$  | Storage Temperature               | -65 to +150            | °C   |
| $T_{BIAS}$ | Temperature Under Bias            | -40 to +85             | °C   |
| $V_{DD}$   | Supply Voltage <sup>1</sup>       | -0.5 to +7.0           | V    |
| $V_{ID}$   | Input/Output Voltage <sup>1</sup> | -0.5 to $V_{DD} + 0.5$ | V    |

CAPACITANCE<sup>4</sup>:  $T_A = 25^\circ\text{C}$ ,  $F = 1.0\text{MHz}$ 

| Symbol           | Parameter         | Max. | Unit | Condition     |
|------------------|-------------------|------|------|---------------|
| C <sub>ADR</sub> | Address Input     | 50   | pF   | $V_{IN} = 0V$ |
| C <sub>CE</sub>  | Chip Enable       | 20   |      |               |
| C <sub>WE</sub>  | Write Enable      | 45   |      |               |
| C <sub>OE</sub>  | Output Enable     | 45   |      |               |
| C <sub>I/O</sub> | Data Input/Output | 50   |      |               |

DC OPERATING CHARACTERISTICS: Over operating ranges

| Symbol    | Characteristics             | Test Conditions                                                                                                    | TYP. | COMMERCIAL |      | INDUSTRIAL <sup>†</sup> |      | Unit          |
|-----------|-----------------------------|--------------------------------------------------------------------------------------------------------------------|------|------------|------|-------------------------|------|---------------|
|           |                             |                                                                                                                    |      | Min.       | Max. | Min.                    | Max. |               |
| $I_{IN}$  | Input Leakage Current       | $V_{IN} = 0V$ to $V_{DD}$                                                                                          |      | -20        | +20  | -20                     | +20  | $\mu\text{A}$ |
| $I_{OUT}$ | Output Leakage Current      | $V_{I/O} = 0V$ to $V_{DD}$ , $\overline{CE}$ or $\overline{OE} = V_{IH}$ , or $\overline{WE} = V_{IL}$             |      | -40        | +40  | -40                     | +40  | $\mu\text{A}$ |
| $I_{CC}$  | Operating Supply Current    | Cycle = min., Duty = 100%, $I_{OUT} = 0\text{mA}$                                                                  | 145  |            | 200  |                         | 200  | mA            |
| $I_{SB1}$ | Full Standby Supply Current | $V_{IN} \geq V_{DD} - 0.2V$ or $V_{IN} \leq V_{SS} + 0.2V$ , $\overline{CE} \geq V_{DD} - 0.2V$ , $f = 0\text{Hz}$ | 1.6  |            | 20   |                         | 20   | mA            |
| $I_{SB2}$ | Standby Current             | $\overline{CE} = V_{IH}$ , $V_{IN} = V_{IH}$ or $V_{IN}$                                                           | 60   |            | 80   |                         | 80   | mA            |
| $V_{OL}$  | Output Low Voltage          | $I_{OUT} = 8.0\text{mA}$                                                                                           |      |            | 0.4  |                         | 0.4  | V             |
| $V_{OH}$  | Output High Voltage         | $I_{OUT} = -4.0\text{mA}$                                                                                          |      | 2.4        |      | 2.4                     |      | V             |

<sup>†</sup> Not available in 20ns.

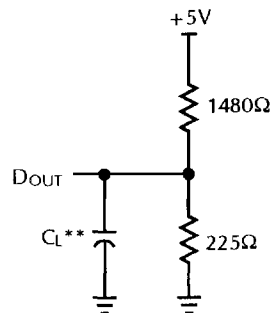
| AC TEST CONDITIONS                       |            |
|------------------------------------------|------------|
| Input Pulse Levels                       | 0V to 3.0V |
| Input Pulse Rise and Fall Times          | 5ns *      |
| Input and Output Timing Reference Levels | 1.5V       |

\* Transition measured between 0.8V and 2.2V.

| Output Load |                |                                                                                                                          |
|-------------|----------------|--------------------------------------------------------------------------------------------------------------------------|
| Load        | C <sub>L</sub> | Parameters Measured                                                                                                      |
| 1           | 100pF          | except t <sub>LZ</sub> , t <sub>OLZ</sub> , t <sub>HZ</sub> , t <sub>OHZ</sub> , t <sub>WHZ</sub> , and t <sub>WLZ</sub> |
| 2           | 5pF            | t <sub>LZ</sub> , t <sub>OLZ</sub> , t <sub>HZ</sub> , t <sub>OHZ</sub> , t <sub>WHZ</sub> , and t <sub>WLZ</sub>        |

Figure 1. Output Load

\*\* Including Probe and Jig Capacitance.



| AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges |                  |                                        |        |      |      |      |      |      |      |      |      |      |      |
|---------------------------------------------------------------------------------|------------------|----------------------------------------|--------|------|------|------|------|------|------|------|------|------|------|
| No.                                                                             | Symbol           | Parameter                              | 20ns † |      | 25ns |      | 30ns |      | 35ns |      | 45ns |      | Unit |
|                                                                                 |                  |                                        | Min.   | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. |      |
| 1                                                                               | t <sub>RC</sub>  | Read Cycle Time                        | 20     |      | 25   |      | 30   |      | 35   |      | 45   |      | ns   |
| 2                                                                               | t <sub>AA</sub>  | Address Access Time                    |        | 20   |      | 25   |      | 30   |      | 35   |      | 45   | ns   |
| 3                                                                               | t <sub>CO</sub>  | Chip Enable to Output Valid            |        | 20   |      | 25   |      | 30   |      | 35   |      | 45   | ns   |
| 4                                                                               | t <sub>OE</sub>  | Output Enable to Output Valid          |        | 5    |      | 6    |      | 8    |      | 10   |      | 12   | ns   |
| 5                                                                               | t <sub>LZ</sub>  | Chip Enable to Output in LOW-Z 4, 5    | 5      |      | 5    |      | 5    |      | 5    |      | 5    |      | ns   |
| 6                                                                               | t <sub>OLZ</sub> | Output Enable to Output in LOW-Z 4, 5  | 0      |      | 0    |      | 0    |      | 0    |      | 0    |      | ns   |
| 7                                                                               | t <sub>HZ</sub>  | Chip Enable to Output in HIGH-Z 4, 5   |        | 12   |      | 13   |      | 15   |      | 20   |      | 25   | ns   |
| 8                                                                               | t <sub>OHZ</sub> | Output Enable to Output in HIGH-Z 4, 5 |        | 5    |      | 6    |      | 10   |      | 12   |      | 12   | ns   |
| 9                                                                               | t <sub>OH</sub>  | Output Hold from Address Change        | 5      |      | 5    |      | 5    |      | 5    |      | 5    |      | ns   |

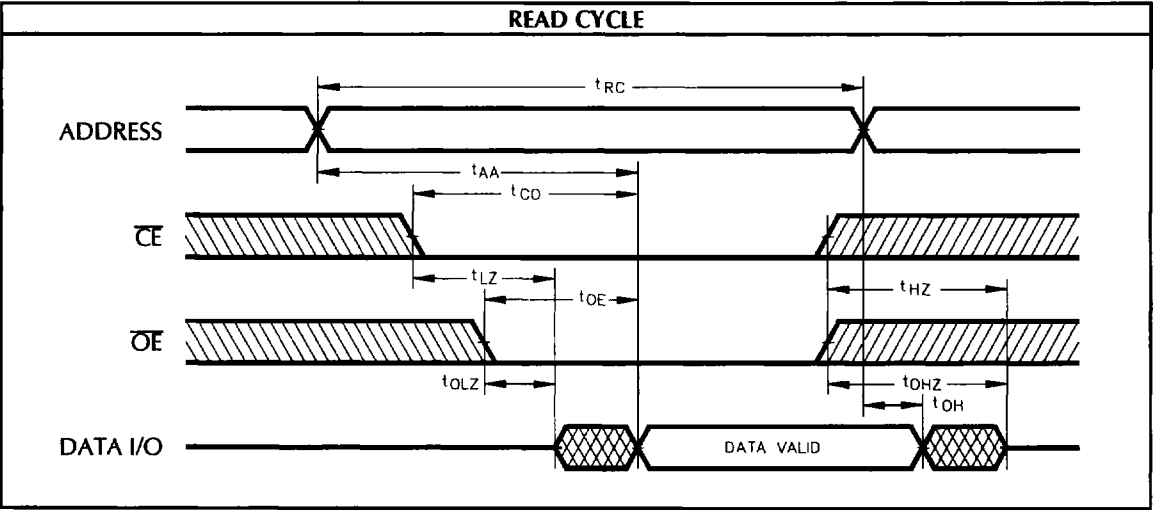
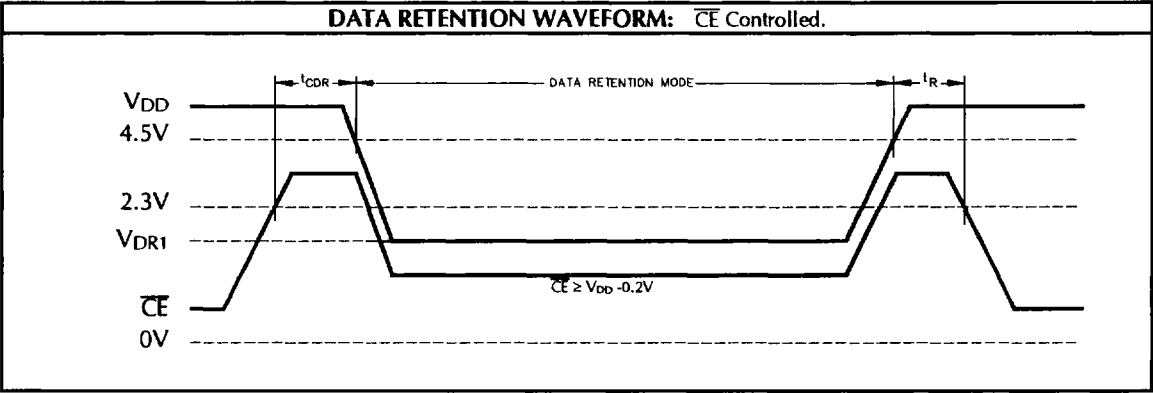
| AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE: Over operating ranges <sup>6, 7</sup> |                  |                                                  |        |      |      |      |      |      |      |      |      |      |      |
|--------------------------------------------------------------------------------------------------|------------------|--------------------------------------------------|--------|------|------|------|------|------|------|------|------|------|------|
| No.                                                                                              | Symbol           | Parameter                                        | 20ns † |      | 25ns |      | 30ns |      | 35ns |      | 45ns |      | Unit |
|                                                                                                  |                  |                                                  | Min.   | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. |      |
| 10                                                                                               | t <sub>WC</sub>  | Write Cycle Time                                 | 20     |      | 25   |      | 30   |      | 35   |      | 45   |      | ns   |
| 11                                                                                               | t <sub>AW</sub>  | Address Valid to End of Write                    | 17     |      | 20   |      | 20   |      | 25   |      | 30   |      | ns   |
| 12                                                                                               | t <sub>CW</sub>  | Chip Enable to End of Write                      | 17     |      | 20   |      | 20   |      | 25   |      | 30   |      | ns   |
| 13                                                                                               | t <sub>AS</sub>  | Address Set-up Time ***                          | 0      |      | 0    |      | 0    |      | 0    |      | 0    |      | ns   |
| 14                                                                                               | t <sub>WP</sub>  | Write Pulse Width                                | 15     |      | 15   |      | 20   |      | 20   |      | 25   |      | ns   |
| 15                                                                                               | t <sub>WR</sub>  | Write Recovery Time                              | 5      |      | 5    |      | 5    |      | 5    |      | 5    |      | ns   |
| 16                                                                                               | t <sub>WHZ</sub> | Write Enable to Output in HIGH-Z <sup>4, 5</sup> |        | 7    |      | 8    |      | 10   |      | 12   |      | 15   | ns   |
| 17                                                                                               | t <sub>DW</sub>  | Data to Write Time Overlap                       | 7      |      | 8    |      | 10   |      | 12   |      | 15   |      | ns   |
| 18                                                                                               | t <sub>DH</sub>  | Data Hold Time from Write Time                   | 5      |      | 5    |      | 5    |      | 5    |      | 5    |      | ns   |
| 19                                                                                               | t <sub>OW</sub>  | Output Active from End of Write                  | 5      |      | 5    |      | 5    |      | 5    |      | 5    |      | ns   |

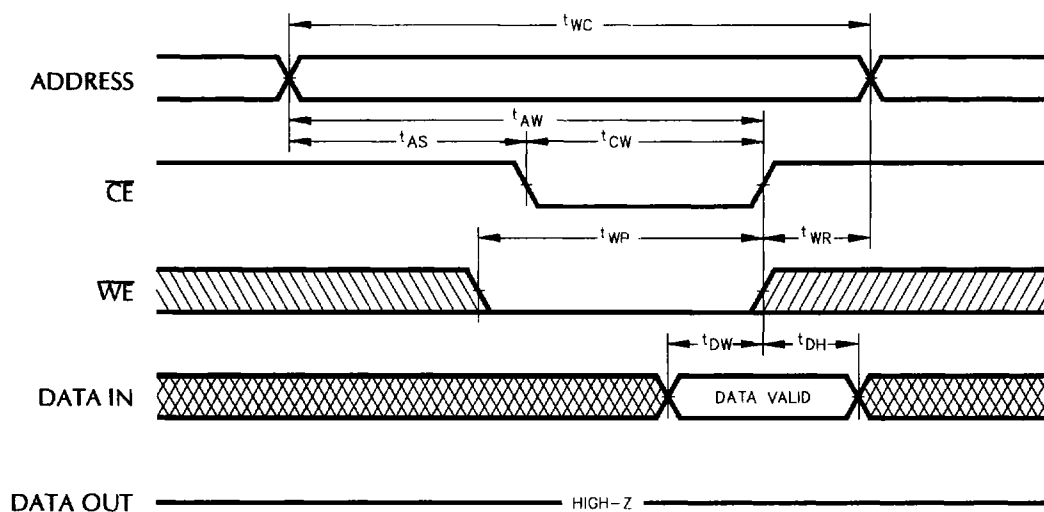
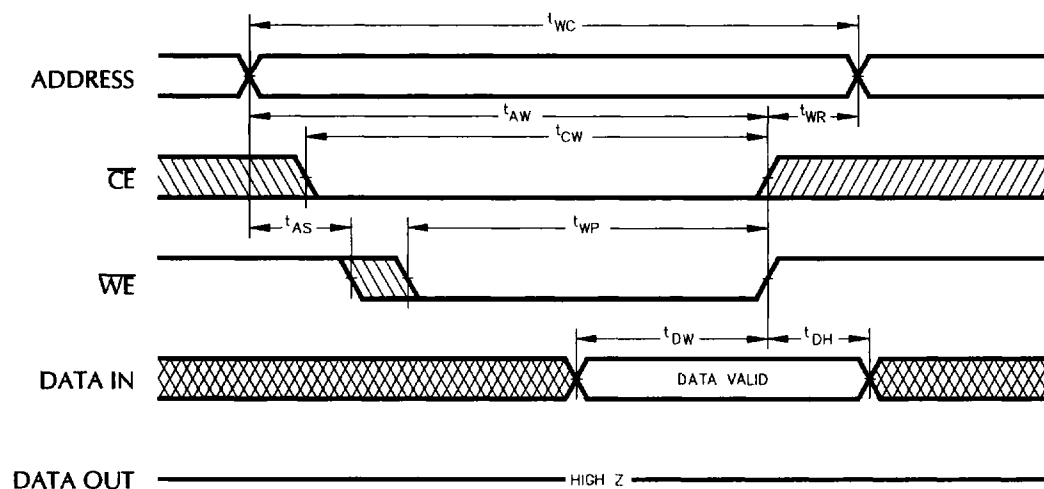
† Available in commercial only.

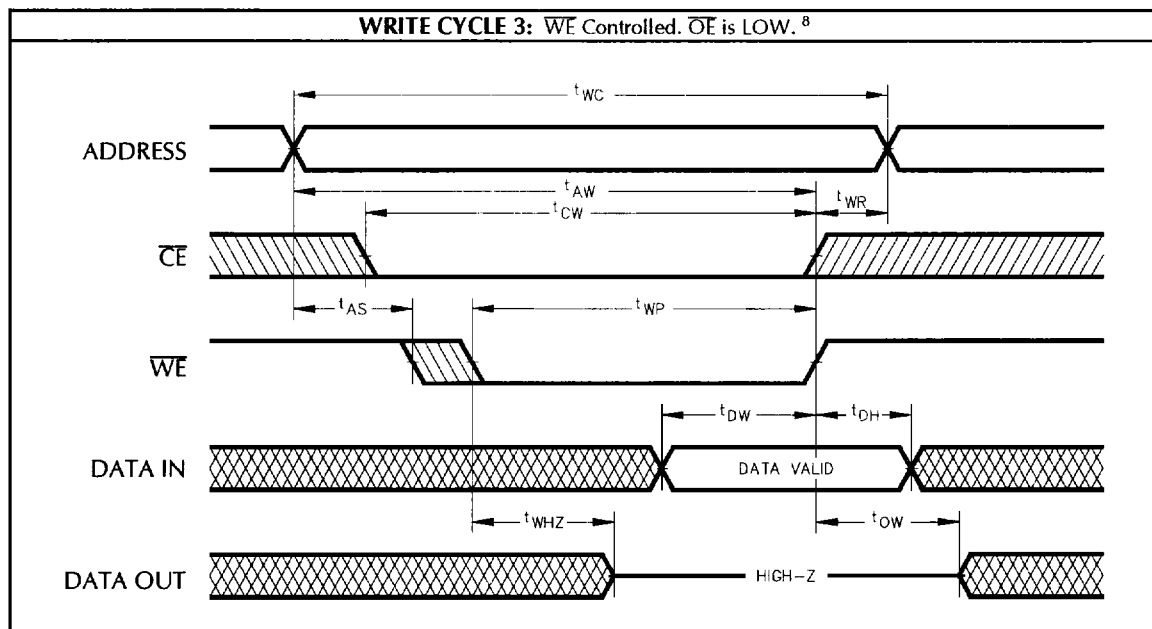
\*\*\* Valid for both Read and Write Cycles.

| DATA RETENTION CHARACTERISTICS |                                     |                                                                                                   |      |            |      |              |      |      |
|--------------------------------|-------------------------------------|---------------------------------------------------------------------------------------------------|------|------------|------|--------------|------|------|
| Symbol                         | Parameter                           | Test Condition                                                                                    | Typ. | Commercial |      | Industrial † |      | Unit |
|                                |                                     |                                                                                                   |      | Min.       | Max. | Min.         | Max. |      |
| V <sub>DR</sub>                | Data Retention Voltage              | CE ≥ V <sub>DR</sub> - 0.2V, V <sub>IN</sub> ≥ V <sub>DD</sub> - 0.2V or V <sub>IN</sub> ≤ + 0.2V |      | 2.0        | 5.5  | 2.0          | 5.5  | V    |
| I <sub>CCDR2</sub>             | Data Retention Supply Current       | V <sub>DR</sub> = 2.0V                                                                            | 0.14 |            | 1.0  |              | 1.6  | mA   |
| I <sub>CCDR3</sub>             | Data Retention Supply Current       | V <sub>DR</sub> = 3.0V                                                                            | 0.28 |            | 1.6  |              | 2.4  | mA   |
| t <sub>CDR</sub>               | Chip Disable to Data Retention Time |                                                                                                   |      | 0          |      | 0            |      | ns   |
| t <sub>R</sub>                 | Recovery Time                       | t <sub>RC</sub> = Read Cycle Timing                                                               |      | 5          |      | 5            |      | ms   |

† Not available in 20ns.



WRITE CYCLE 1:  $\overline{CE}$  Controlled.WRITE CYCLE 2:  $\overline{WE}$  Controlled.  $\overline{OE}$  is HIGH.<sup>8</sup>

**NOTES:**

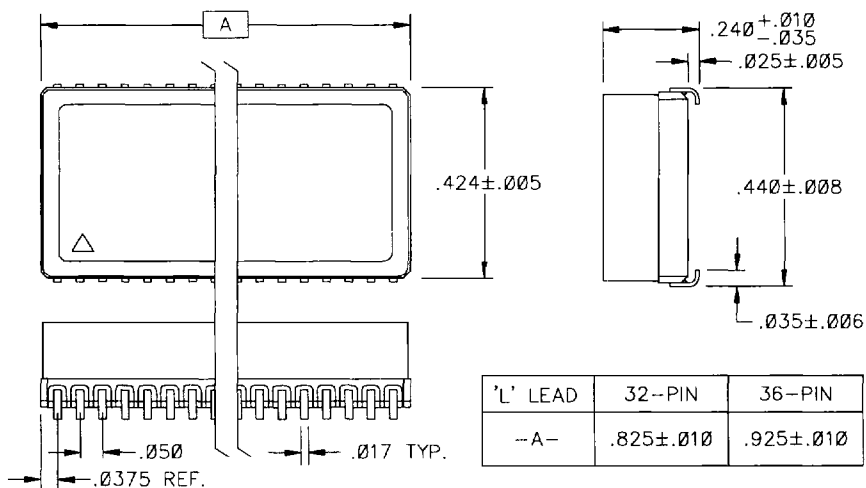
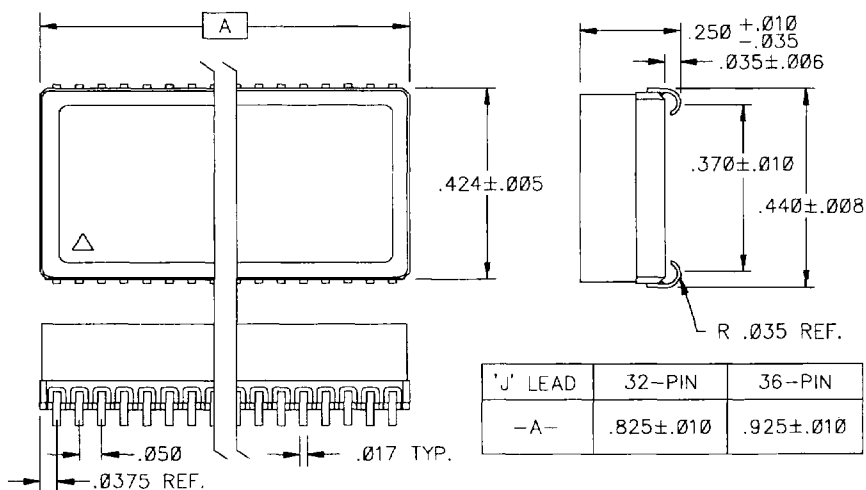
1. All voltages are with respect to  $V_{SS}$ .
2. -2.0V min. for pulse width less than 20ns ( $V_{IL}$  min. = -0.5V at DC level).
3. Stresses greater than those under **ABSOLUTE MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
4. This parameter is guaranteed and not 100% tested.
5. Transition is measured at the point of  $\pm 500\text{mV}$  from steady state voltage.
6. When  $\overline{OE}$  and  $\overline{CE}$  are LOW and  $\overline{WE}$  is HIGH, I/O pins are in the output state, and input signals of opposite phase to the outputs must not be applied.
7. The outputs are in a high impedance state when  $\overline{WE}$  is LOW.
8. Chip Enable and Write Enable can initiate and terminate WRITE Cycle.

**ORDERING INFORMATION**

DP S 512 S 8 X X4 - XX XX  
 PREFIX TYPE MEMORY DEPTH DESIG MEMORY WIDTH DESIG PACKAGE SPEED GRADE

|    |                                 |                   |
|----|---------------------------------|-------------------|
| CI | COMMERCIAL PROCESSED            | -40°C to +85°C    |
|    | at INDUSTRIAL TEMP.             |                   |
| C  | COMMERCIAL                      | 0°C to +70°C      |
| 20 | 20ns                            | (COMMERCIAL ONLY) |
| 25 | 25ns                            |                   |
| 30 | 30ns                            |                   |
| 35 | 35ns                            |                   |
| 45 | 45ns                            |                   |
| J4 | 'J' LEADED/2nd GENERATION STACK |                   |
| L4 | 'L' LEADED/2nd GENERATION STACK |                   |
| E  | 32-PIN EVOLUTIONARY PIN-OUT     |                   |
| R  | 36-PIN REVOLUTIONARY PIN-OUT    |                   |
| S  | MODULE WITH SUPPORT LOGIC       |                   |
|    | CMOS SRAM                       |                   |

## MECHANICAL DRAWING

**Dense-Pac Microsystems, Inc.**

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