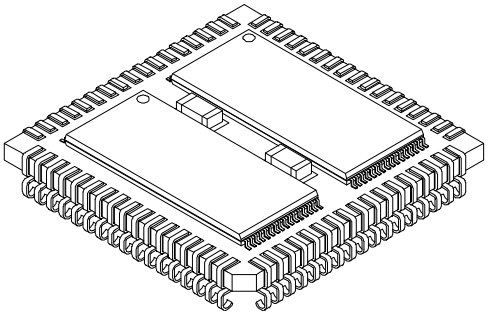
DENSE-PAC
MICROSYSTEMS

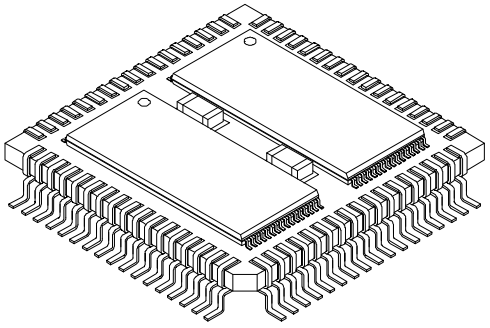
4 Megabit 5 Volt CMOS FLASH EEPROM
DPZ128X32XP/XHP

DESCRIPTION:

The DPZ128X32XP/XHP is a 4 megabit 5 Volt only CMOS Flash EEPROM (Electrically In-System Programmable and Erasable ROM memory) module. The module is built with four 128K x 8 FLASH memory devices. The DPZ128X32XP/XHP can be user configurable as 512K x 8, 256K x 16 or 128K x 32 bits.

The DPZ128X32XP/XHP is ideal for use in systems that require In-System periodic code updates, or for use as a high speed nonvolatile storage medium.



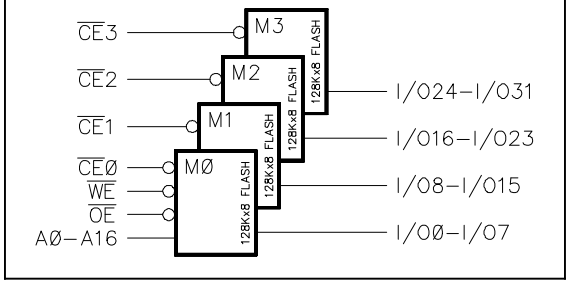


FEATURES:

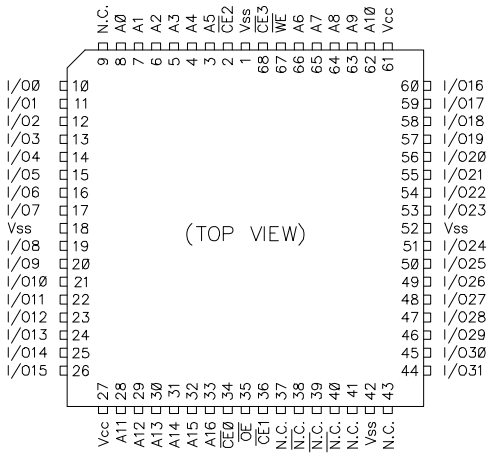
- User Definable Configuration:
  512K x 8, 256K x 16 or 128K x 32
- Fast Read Access Times: 70, 90, 120, 150ns
- Low Power: 120mA Maximum Active (32 bit Mode)
  400µA Maximum Standby (CMOS)
- 10,000 Erase/Program Cycles Minimum
- 5 Volt Only In-System Programming
- TTL-Compatible Inputs and Outputs
- Packages Available:
  68- "J" Leaded Plastic Surface Mount Module
  68- Gull - Leaded Plastic Surface Mount Module

PIN NAMES	
A0 - A16	Address Inputs
I/O0 - I/O31	Data Input/Output
$\overline{CE}$0 - $\overline{CE}$3	Low Chip Enables
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{DD}	Power (+5V)
V_{SS}	Ground
N.C.	No Connect

FUNCTIONAL BLOCK DIAGRAM



PIN-OUT DIAGRAM



DEVICE OPERATION

DATA BUS WIDTH:

The DPZ128X32XP/XHP is configured with separate $\overline{CE}$'s and data I/O's to allow the module to be used in an 8 bit, 16 bit or 32 bit environment. When either the software data protect or the chip erase feature is used, the specific data shown in the algorithms must be written to each device that the operation is being perfomed on. An example would be if the module is used in a 32 bit system, the data called out in the third data load for the software data protect alogrithm is A0H. The data of A0A0A0A0H should be written to the DPZ128X32XP/XHP.

READ:

The DPZ128X32XP/XHP is accessed like a Static Ram. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers flexibility in preventing bus contention.

BYTE LOAD:

A byte is loaded into the device by applying a low pulse to $\overline{WE}$ or $\overline{CE}$ with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high. On the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last, the address is latched. On the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs first, the data is latched. This operation is used to load data into the 128 byte page for programming or to load software codes for data protection or 5 volt chip erase.

PROGRAM:

This DPZ128X32XP/XHP is programmed in a page mode only. A7 to A16 are used to specify the page address and they must be valid during each high to low transition of $\overline{WE}$ or $\overline{CE}$. A0 to A6 are used to specify the address of the byte within the 128 byte page. The data can be loaded into the page in any order. All of the bytes within the page must be written, otherwise any unwritten bytes will be erased to read FFH. The locations to be reprogrammed need not be erased prior to programming as with other FLASH technologies. Each new byte to be loaded must have its high to low transition of $\overline{WE}$ or $\overline{CE}$ within 150µs of the preceding bytes high to low transition. If a high to low transition is not detected within 150µs of the last high to low transition, the internal programming period will begin.

DATA POLLING:

The DPZ128X32XP/XHP features DATA Polling to indicate the end of a program cycle. During a program cycle an attempted read of the last byte loaded will result in the complement of the loaded data on the MSB (most significant bit, I/O7,I/O15,I/O23 and I/O31) of the device or devices being programmed at that time. When the programming cycle is complete, the data will be true on all outputs and the next programming cycle can begin. Data Polling can begin at any time during the programming period.

TOGGLE BIT:

The DPZ128X32XP/XHP has an additional method for determining if the program period or erase cycle is completed. During a program or erase operation, successive attempts to read data from the device will result in I/O6, I/O14, I/O22 or I/O30 (depending on the device or devices the operation is being performed on) toggling between one and zero. Once the program or erase period has completed, the I/O pin will stop toggling and valid data can be read. Examining the toggle bit can begin at any time during the program or erase period.

HARDWARE DATA PROTECTION:

The devices used on the DPZ128X32XP/XHP incorporate several hardware features for data protection. If V_{DD} falls below 3.8V (typ.), the program function is inhibited. During power up, programming will be inhibited 5ms (typ.) after V_{DD} has reached the V_{DD} sense level. Another hardware feature is a noise filter on $\overline{CE}$ or $\overline{WE}$. Any pulse less than 15ns (typ.) will not initiate a program cycle. Finally, programming is inhibited by holding any one of: $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high.

SOFTWARE DATA PROTECTION:

The DPZ128X32XP/XHP features software data protection that can be enabled and disabled by the end user. The software protection is enabled by writing a series of three commands to specific addresses with specific data using the page program timing specifications. Once the software protection is enabled, the same three commands must precede a program cycle. The software protection will remain active until the disable command algorithm is issued. Power transitions will not reset the software protection. The data will be protected against inadvertent programming during power transitions. The DPZ128X23VT/VTP is shipped with the software data protection disabled.

5 VOLT CHIP ERASE:

Each device on the DPZ128X32XP/XHP can be erased at one time by using a six byte software code. The erase code consists of six byte load commands to specific address locations with specific data patterns. After the command is entered, every location in the device being erased will be set to a high state (FFH).

RECOMMENDED OPERATING RANGE [1]					
Symbol	Characteristic	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input HIGH Voltage	2.0			V
V_{IL}	Input LOW Voltage			0.8	V

ABSOLUTE MAXIMUM RATING [3]			
Symbol	Parameter	Value	Unit
T_{STC}	Storage Temperature	-65 to + 150	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
V_{DD}	Supply Voltage [1]	-0.6 to + 6.25	V
$V_{I/O}$	Input/Output Voltage [1]	-0.6 to V_{DD}+0.6	V
V_{OE}	$\overline{OE}$ Input Voltage [1]	-0.6 to +13.5	V

AC TEST CONDITIONS	
Input Pulse Level	0V to 3.0V
Input Pulse Rise and Fall Times	5ns*
Input and Output Timing Reference Levels	1.5 V

* Transition between 0.8 and 2.2V.

OUTPUT LOAD		
Float	C_L	Parameters Measured
1	100pF	except t_{DF}
2	5pF	t_{DF}

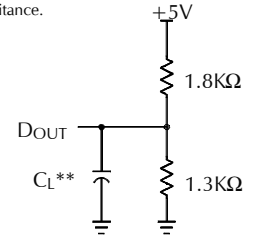
TRUTH TABLE				
Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O PIN
Standby	H	X	X	HIGH-Z
Read	L	L	H	D_{OUT}
Write	L	H	L	D_{IN}
Write Inhibit	X	L	X	HIGH-Z
Write Inhibit	X	X	H	HIGH-Z
5.0V Chip Erase	L	H	L	-
Output Disable	X	H	X	HIGH-Z

L = LOW H = HIGH X = Don't Care

CAPACITANCE [4]: T_A = 25°C, F = 1.0MHz				
Symbol	Parameter	Max.	Unit	Condition
C_{CE}	Chip Enable	15	pF	V_{IN} = 0V
C_{ADR}	Address Input	35		
C_{WE}	Write Enable	35		
C_{OE}	Output Enable	35		
$C_{I/O}$	Data Input/Output	20		

FIGURE 1: Output Load

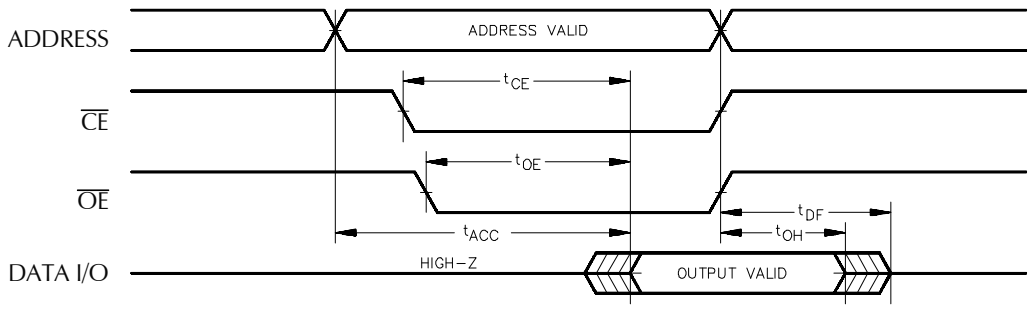
** Including Probe and Jig Capacitance.



DC OPERATING CHARACTERISTICS: Over the operating ranges.									
Symbol	Characteristics	Test Conditions	X 32		X 16		X8		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
I_{CC}	Operating Supply Current	$\overline{CE}$ = $\overline{OE}$ = V_{IL} all I/O = 0mA F = 5MHz		200		105		60	mA
I_{SB1}	V_{DD} Current Standby (TTL)	$\overline{CE}$ = V_{IH}		12		12		12	mA
I_{SB2}	V_{DD} Current Standby (CMOS)	$\overline{CE}$ = V_{DD} -0.3Vdc		1.2		1.2		1.2	mA
I_{IL}	Input Leakage Current	V_{IN} - V_{DD} Max.	-40	+40	-40	+40	-40	+40	µA
I_{OL}	Output Leakage Current	V_{OUT} - V_{DD} Max.	-10	+10	-20	+20	-40	+40	µA
V_{IL}	Input Voltage Low			0.8		0.8		0.8	V
V_{IH}	Input Voltage High		2.0		2.0		2.0		V
V_{OL}	Output Voltage Low	I_{OUT} = 2.1mA		0.45		0.45		0.45	V
V_{OH}	Output Voltage High	I_{OUT} = -400µA	2.4		2.4		2.4		V

A.C. OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges											
No.	Symbol	Parameter	70ns		90ns		120ns		150ns		Unit
			Min.	Max.	Min.	Max.	Mn.	Max.	Min.	Max.	
1	t_{ACC}	Address to Output Valid		70		90		120		150	ns
2	t_{CE}	Chip Enable to Output Valid		70		90		120		150	ns
3	t_{OE}	Output Enable to Output Valid	0	35	0	40	0	50	0	70	ns
4	t_{DF}	Chip Enable or Output Enable to Float [4]	0	25	0	25	0	30	0	40	ns
5	t_{OH}	Output Hold from Chip Enable, Output Enable, or Address, Whichever Occurs First	0		0		0		0		ns

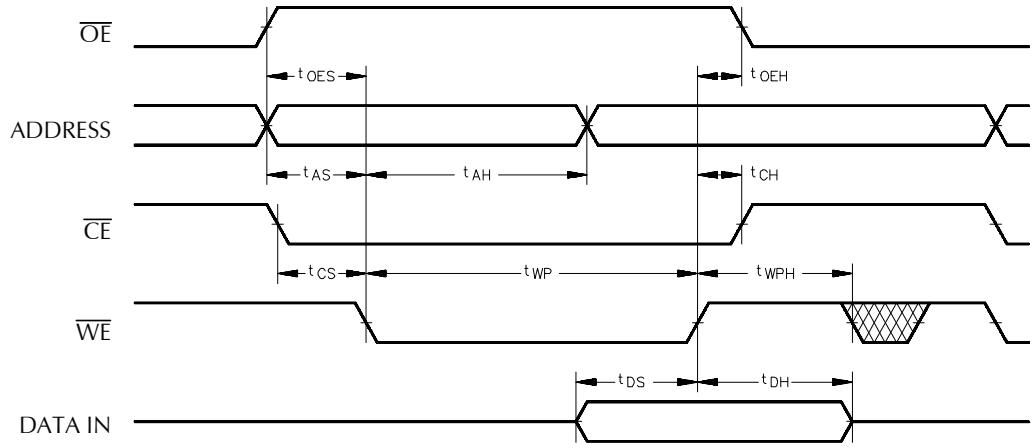
READ CYCLE



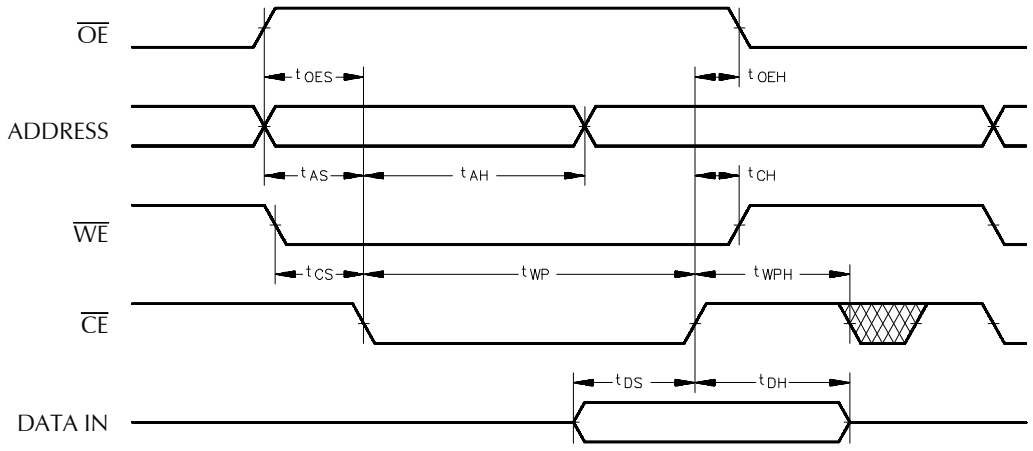
A.C. BYTE LOAD CHARACTERISTICS					
No.	Symbol	Parameter	Min.	Max.	Unit
6	t_{AS}	Address Setup Time	0		ns
7	t_{OES}	Output Enable Setup Time	0		ns
8	t_{AH}	Address Hold Time	50		ns
9	t_{CS}	Chip Select Setup Time	0		ns
10	t_{CH}	Chip Select Hold Time	0		ns
11	t_{WP}	Write Pulse Width (Write Enable or Chip Enable)	90		ns
12	t_{DS}	Data Setup Time	35		ns
13	t_{DH}	Data Hold Time	0		ns
14	t_{OEH}	Output Enable Hold Time	0		ns
15	t_{WPH}	Write Page Width High	100		ns

NOTES:
1. All voltages are with respect to V_{SS}.
2. -1.0V min. for pulse width less than 20ns (V_{IL} min. = -0.3V at DC level).
3. Stresses greater than those under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
4. This parameter is guaranteed and not 100% tested.
5. A7 through A16 specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.
6. $\overline{OE}$ must be high when $\overline{WE}$ and $\overline{CE}$ are both low.
7. All bytes that are not loaded within the page being programmed will be erased to FF.
8. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
9. Beginning and ending state of I/O6 will vary.
10. Any address location may be used but the address should not vary.

A.C. BYTE LOAD WAVEFORMS: $\overline{WE}$ Controlled.



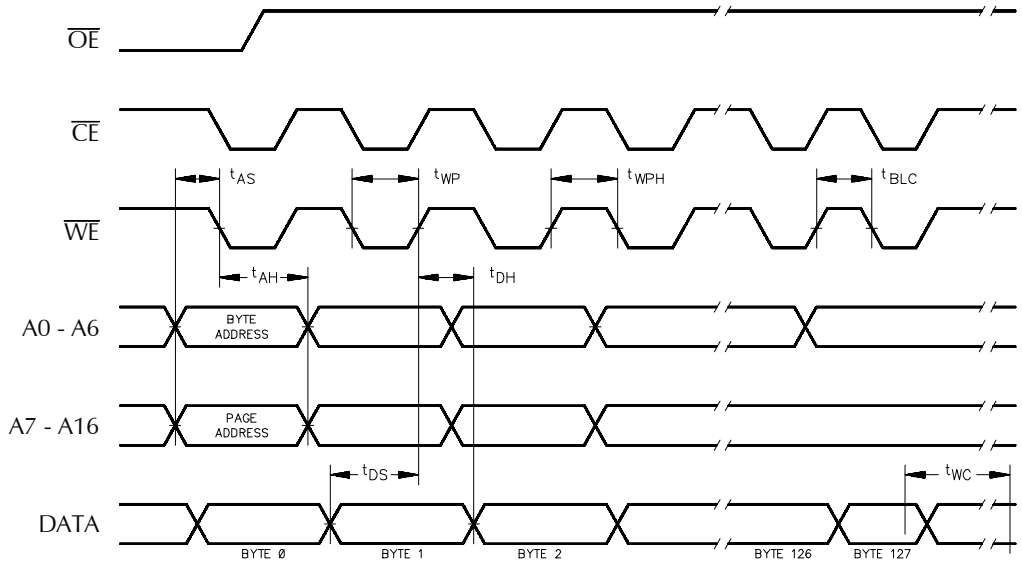
A.C. BYTE LOAD WAVEFORMS: $\overline{CE}$ Controlled.



WAVEFORM KEY

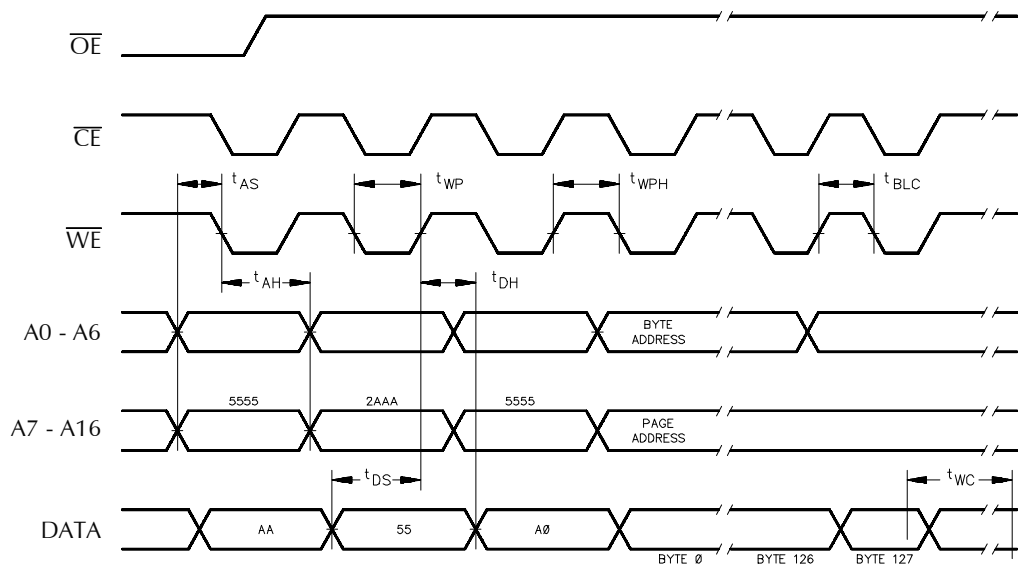
PROGRAM CYCLE CHARACTERISTICS					
No.	Symbol	Parameter	Min.	Max.	Unit
16	t_{WC}	Write Cycle Time		10	ms
17	t_{AS}	Address Setup Time	0		ns
18	t_{AH}	Address Hold Time	50		ns
19	t_{DS}	Data Setup Time	35		ns
20	t_{DH}	Data Hold Time	0		ns
21	t_{WP}	Write Pulse Width	90		ns
22	t_{BLC}	Byte Load Cycle Time		150	µs
23	t_{WPH}	Write Pulse Width Time	100		ns

PROGRAM CYCLE WAVEFORMS [5, 6, 7]



SOFTWARE DATA PROTECT ENABLE ALGORITHM				
Step	Mode	Address (A0 - A14)	Data (I/O0 - I/O7)	Comment
1	Write	5555 Hex	AA Hex	Dummy Write.
2	Write	2AAA Hex	55 Hex	Dummy Write.
3	Write	5555Hex	A0 Hex	Writes Enabled Data Protect state will be activated at end of program cycle.
4	Write	Address	Data	128 bytes of data are entered. Enter Data Protect stated.

SOFTWARE PROTECT PROGRAM CYCLE WAVEFORMS [5, 6, 7]

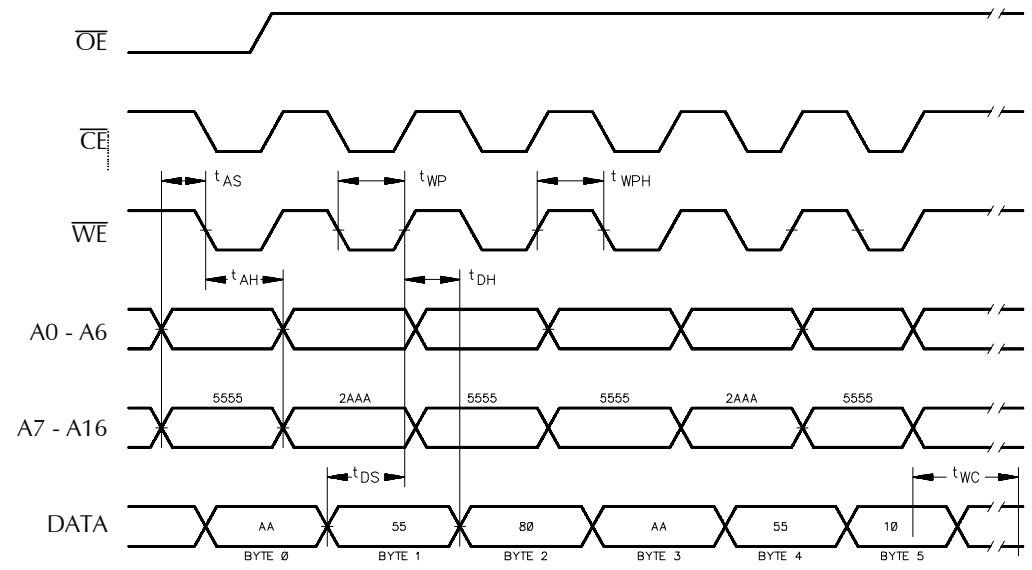


SOFTWARE DATA PROTECT DISABLE ALGORITHM				
Step	Mode	Address (A0 - A14)	Data (I/O0 - I/O7)	Comment
1	Write	5555 Hex	AA Hex	Dummy Write.
2	Write	2AAA Hex	55 Hex	Dummy Write.
3	Write	5555 Hex	80 Hex	Dummy Write.
4	Write	5555 Hex	AA Hex	Dummy Write.
5	Write	2AAA Hex	55 Hex	Dummy Write.
6	Write	5555Hex	20 Hex	Exit Data Protect state. Data Protect state will be deactivated at end of program period.
7	Write	Address	Data	128 bytes of data are entered.

CHIP ERASE CYCLE CHARACTERISTICS					
No.	Symbol	Parameter	Min.	Max.	Unit
24	t_{WC}	Write Cycle Time		20	ms
25	t_{AS}	Address Setup Time	0		ns
26	t_{AH}	Address Hold Time	50		ns
27	t_{DS}	Data Setup Time	35		ns
28	t_{DH}	Data Hold Time	0		ns
29	t_{WP}	Write Pulse Width	90		ns
30	t_{BLC}	Byte Load Cycle Time		150	µs
31	t_{WPH}	Write Pulse Width High	100		ns

SOFTWARE CHIP ERASE ALGORITHM				
Step	Mode	Address (A0 - A14)	Data (I/O0 - I/O7)	Comment
1	Write	5555 Hex	AA Hex	Dummy Write.
2	Write	2AAA Hex	55 Hex	Dummy Write.
3	Write	5555 Hex	80 Hex	Dummy Write.
4	Write	5555 Hex	AA Hex	Dummy Write.
5	Write	2AAA Hex	55 Hex	Dummy Write.
6	Write	5555Hex	10 Hex	$\overline{\text{DATA}}$ Polling may be used to determine the end of the erase cycle by checking any address for data equal to FF. After loading the six byte code, no byte loads are allowed until the completion of the erase cycle. The erase cycle will time itself to completion within t_{WC}.

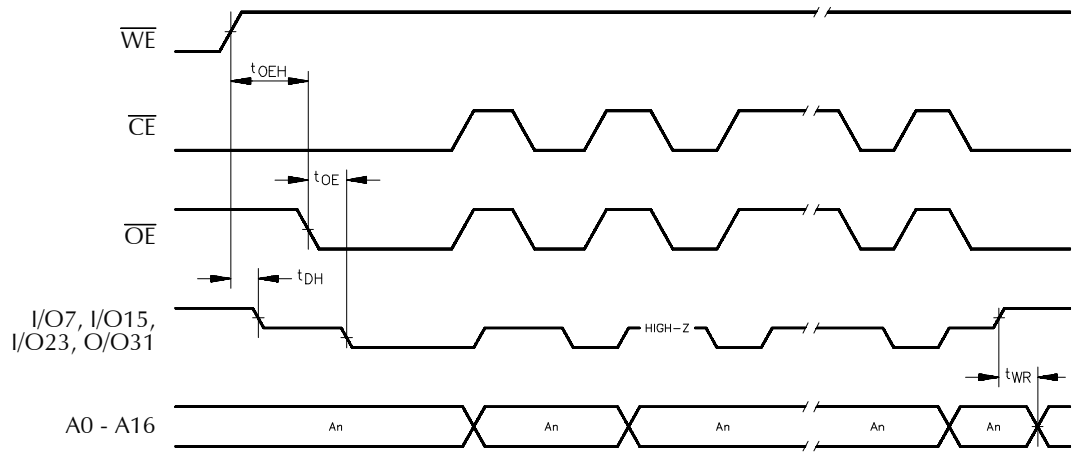
CHIP ERASE CYCLE WAVEFORMS [6]



$\overline{\text{DATA}}$ POLLING CHARACTERISTICS [4]					
No.	Symbol	Parameter	Min.	Max.	Unit
32	t_{DH}	Data Hold Time	10		ns
33	t_{OEH}	Output Enable Hold Time	10		ns
34	t_{OE}	Output Enable to Output Delay *			ns
35	t_{WR}	Write Recovery Time	0		ns

* See t_{OE} spec in AC Read Characteristic.

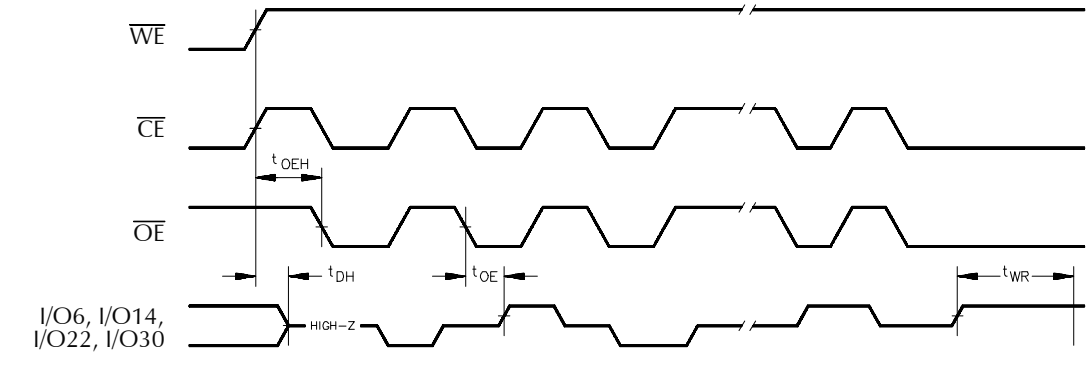
DATA POLLING WAVEFORMS [6]



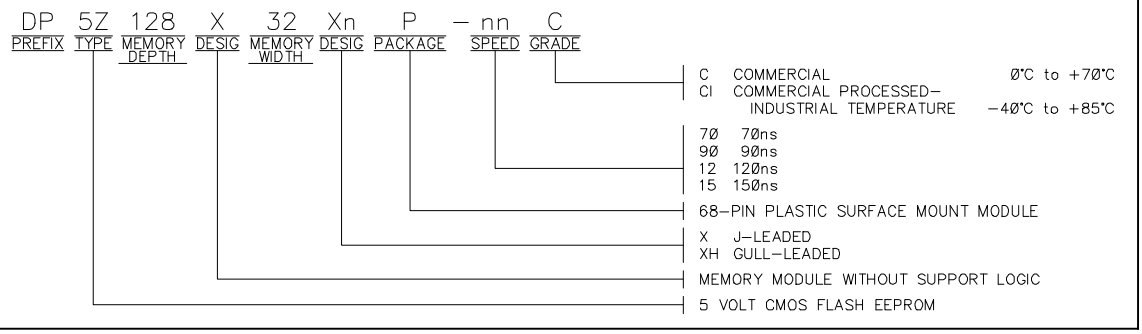
TOGGLE BIT CHARACTERISTICS [4]					
No.	Symbol	Parameter	Min.	Max.	Unit
36	t_{DH}	Data Hold Time	10		ns
37	t_{OEH}	Output Enable Hold Time	10		ns
38	t_{OE}	Output Enable to Output Delay*			ns
39	t_{OEHP}	Output Enable High Pulse	150		ns
40	t_{WR}	Write Recovery Time	0		ns

* See t_{OE} spec in AC Read Characteristic.

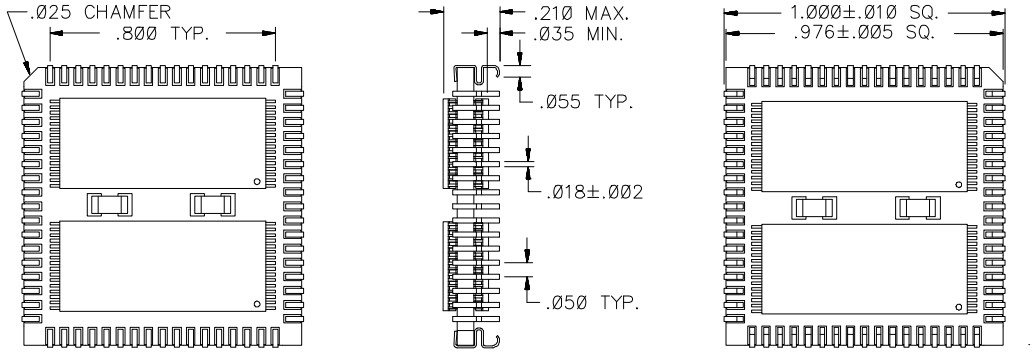
TOGGLE BIT WAVEFORMS [8, 9, 10]



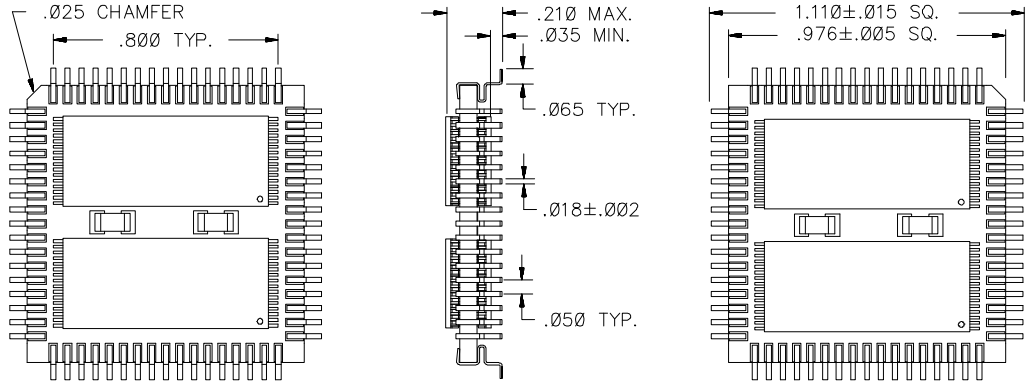
ORDERING INFORMATION



"J" LEADED MECHANICAL DRAWING



GULL-LEADED MECHANICAL DRAWING



Dense-Pac Microsystems, Inc.
7321 Lincoln Way ◆ Garden Grove , California 92841-1431
(714) 898-0007 (800) 642-4477 (Outside CA) ◆ FAX: (714) 897-1772 ◆ http://www.dense-pac.com