Recommended System Management Alternative: X4043

2K **X24C02** **256 x 8 Bit**

Serial EEPROM

FEATURES

- **2.7V to 5.5V power supply versions**
- **Low power CMOS**
  - **—Active read current less than 1 mA**
  - **—Active write current less than 1.5 mA**
- **Internally organized 256 x 8**
- **2-wire serial interface**
  - **—Bidirectional data transfer protocol**
  - **—Schmitt trigger input noise suppression 400kHz across V_{CC} range**
- **Sixteen byte page write mode**
  - **—Minimizes total write time per byte**
- **Self-timed write cycle**
  - **—Typical write cycle time of 5 ms**
- **High reliability**
  - **—Endurance: 1,000,000 cycles**
  - **—Data retention: 100 years**
- **8-pin SOIC**

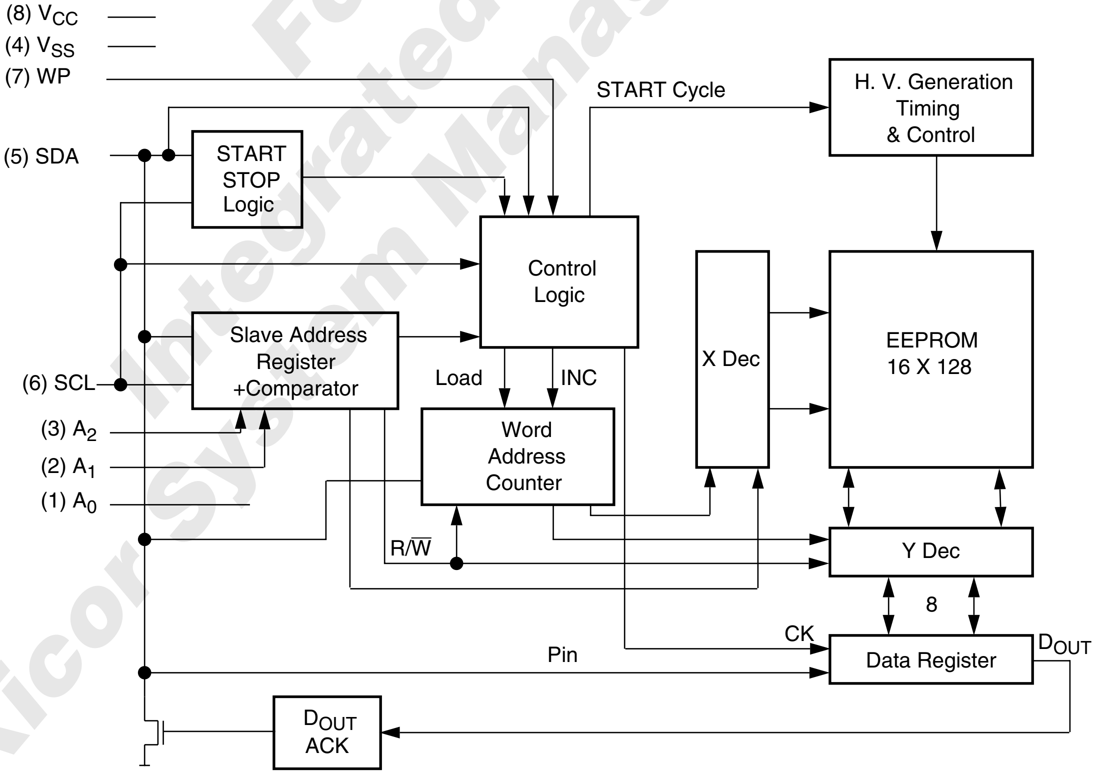
DESCRIPTION

The X24C02 is a CMOS 2048 bit serial EEPROM, internally organized 256 x 8. The X24C02 features a serial interface and software protocol allowing operation on a simple two wire bus.

The X24C02 is fabricated with Xicor's advanced CMOS Textured Poly Floating Gate Technology.

The X24C02 utilizes Xicor's proprietary DirectWrite™ cell, providing a minimum endurance of 1,000,000 cycles and a minimum data retention of 100 years.

BLOCK DIAGRAM



PIN DESCRIPTIONS

Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device.

Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs.

An open drain output requires the use of a pull-up resistor. For selecting typical values, refer to the Pull-Up Resistor selection graph at the end of this data sheet.

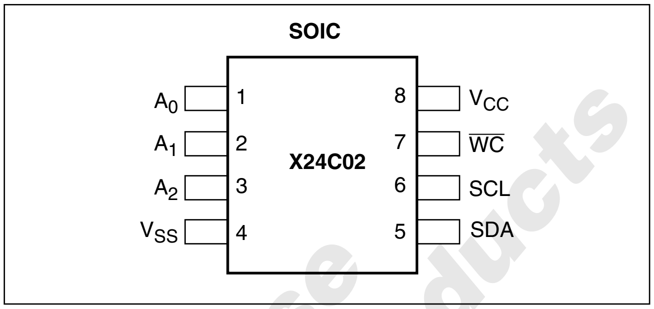
Address (A_0, A_1, A_2)

The Address inputs (A_0, A_1, A_2) are used to set the appropriate bits of the seven bit slave address. These inputs can be used static or actively driven. If used statically they must be tied to V_{SS} or V_{CC} as appropriate. If driven they must be driven to V_{SS} or to V_{CC}.

PIN NAMES

Symbol	Description
A_0–A_2	Address Inputs
SDA	Serial Data
SCL	Serial Clock
$\overline{WC}$	Write Control
V_{SS}	Ground
V_{CC}	Supply Voltage

PIN CONFIGURATION



DEVICE OPERATION

The X24C02 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers, and provide the clock for both transmit and receive operations. Therefore, the X24C02 will be considered a slave in all applications.

Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to Figures 1 and 2.

Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The X24C02 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

Stop Condition

All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used by the X24C02 to place the device in the standby power mode after a read sequence. A stop condition can only be issued after the transmitting device has released the bus.

Figure 1. Data Validity

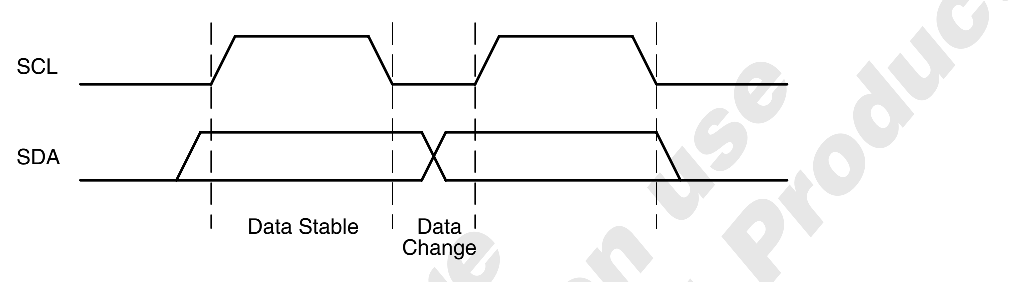
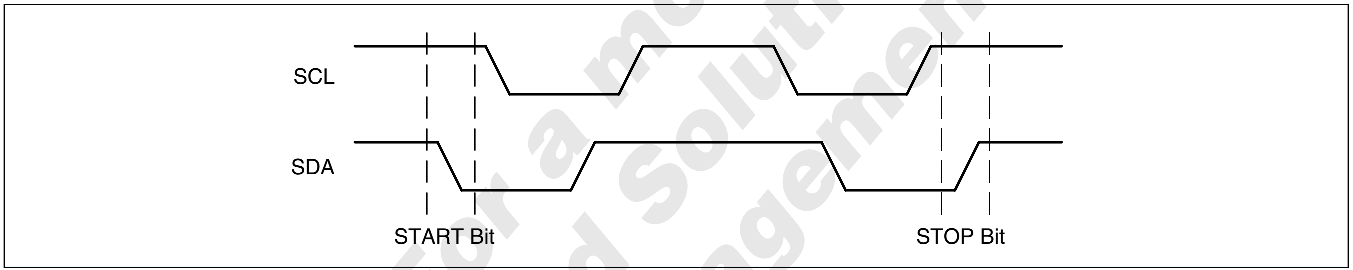


Figure 2. Definition of Start and Stop



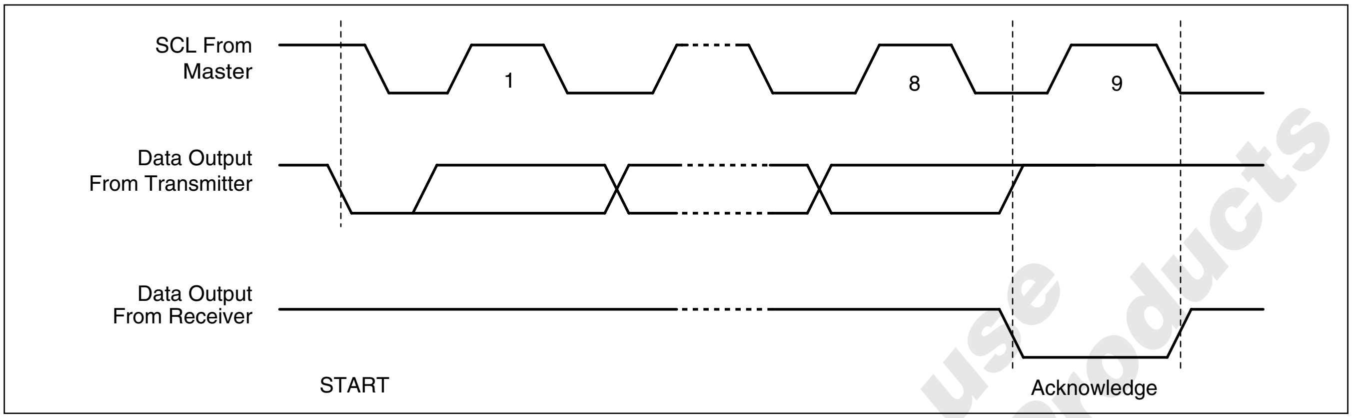
Acknowledge

Acknowledge is a software convention used to indicate successful data transfer. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to Figure 3.

The X24C02 will respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the X24C02 will respond with an acknowledge after the receipt of each subsequent eight bit word.

In the read mode the X24C02 will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the X24C02 will continue to transmit data. If an acknowledge is not detected, the X24C02 will terminate further data transmissions. The master must then issue a stop condition to return the X24C02 to the standby power mode and place the device into a known state.

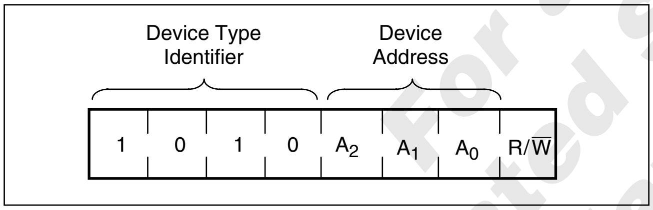
Figure 3. Acknowledge Response From Receiver



DEVICE ADDRESSING

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave are the device type identifier (see Figure 4). For the X24C02 this is fixed as 1010[B].

Figure 4. Slave Addressing



The next three significant bits address a particular device. A system could have up to eight X24C02 devices on the bus (see Figure 10). The eight addresses are defined by the state of the A_0, A_1 and A_2 inputs.

The last bit of the slave address defines the operation to be performed. When set to one a read operation is selected, when set to zero a write operation is selected.

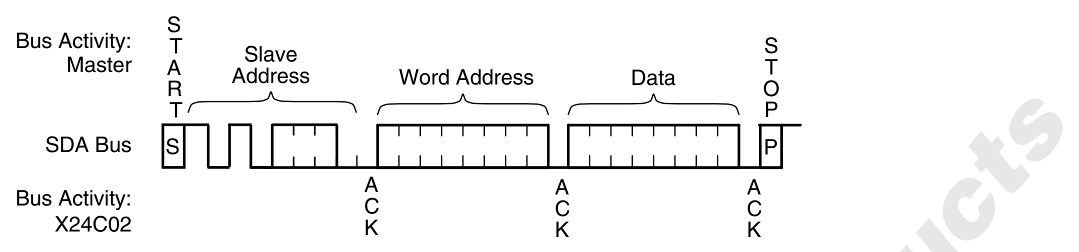
Following the start condition, the X24C02 monitors the SDA bus comparing the slave address being transmitted with its slave address (device type and state of A_0, A_1 and A_2 inputs). Upon a correct compare the X24C02 outputs an acknowledge on the SDA line. Depending on the state of the R/W bit, the X24C02 will execute a read or write operation.

WRITE OPERATIONS

Byte Write

For a write operation, the X24C02 requires a second address field. This address field is the word address, comprised of eight bits, providing access to any one of the 256 words of memory. Upon receipt of the word address the X24C02 responds with an acknowledge, and awaits the next eight bits of data, again responding with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the X24C02 begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress the X24C02 inputs are disabled, and the device will not respond to any requests from the master. Refer to Figure 5 for the address, acknowledge and data transfer sequence.

Figure 5. Byte Write

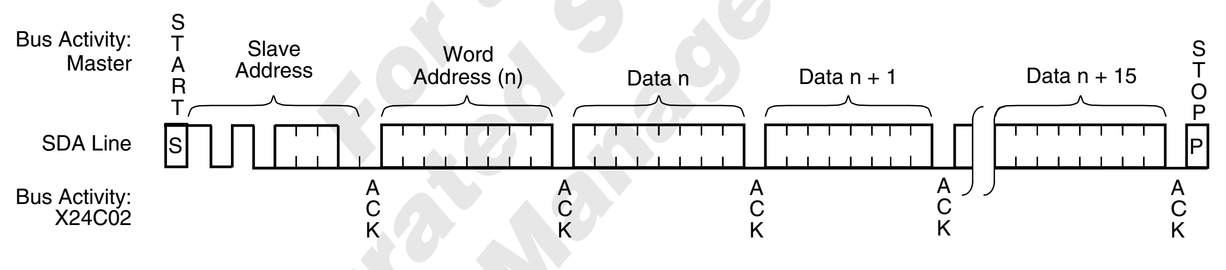


Page Write

The X24C02 is capable of a sixteen byte page write operation. It is initiated in the same manner as the byte write operation, but instead of terminating the write cycle after the first data word is transferred, the master can transmit up to fifteen more words. After the receipt of each word, the X24C02 will respond with an acknowledge.

After the receipt of each word, the four low order address bits are internally incremented by one. The high order five bits of the address remain constant. If the master should transmit more than sixteen words prior to generating the stop condition, the address counter will "roll over" and the previously written data will be overwritten. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer to Figure 6 for the address, acknowledge and data transfer sequence.

Figure 6. Page Write

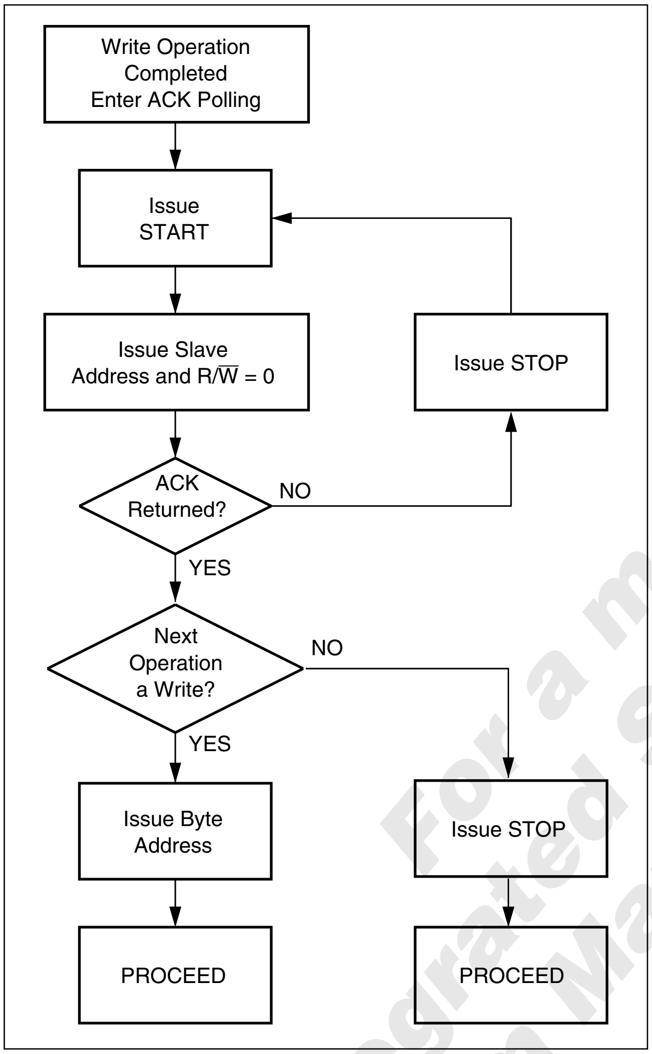


Note: In this example n = xxxx 000 (B); x = 1 or 0

Acknowledge Polling

The disabling of the inputs can be used to take advantage of the typical 5 ms write cycle time. Once the stop condition is issued to indicate the end of the host's write operation, the X24C02 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition, followed by the slave address for a write operation. If the X24C02 is still busy with the write operation no ACK will be returned. If the X24C02 has completed the write operation an ACK will be returned, and the host can then proceed with the next read or write operation. Refer to Flow 1.

Flow 1. ACK Polling Sequence



READ OPERATIONS

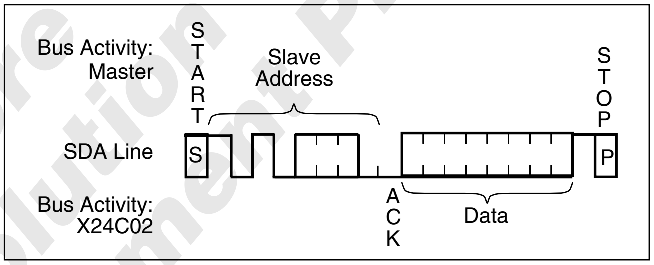
Read operations are initiated in the same manner as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to a one. There are three basic read operations: current address read, random read and sequential read.

It should be noted that the ninth clock cycle of the read operation is not a "don't care." To terminate a read operation, the master must either issue a stop condition during the ninth cycle, or hold SDA HIGH during the ninth clock cycle and then issue a stop condition.

Current Address Read

Internally the X24C02 contains an address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address n, the next read operation would access data from address n + 1. Upon receipt of the slave address with the R/$\overline{W}$ bit set to one, the X24C02 issues an acknowledge and transmits the eight bit word. The read operation is terminated by the master by not responding with an acknowledge, and issuing a stop condition. Refer to Figure 7 for the sequence of address, acknowledge and data transfer.

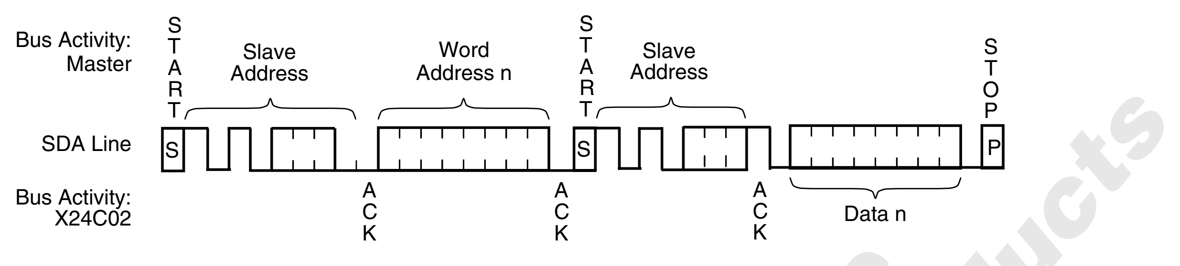
Figure 7. Current Address Read



Random Read

Random read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the R/$\overline{W}$ bit set to one, the master must first perform a "dummy" write operation. The master issues the start condition, and the slave address followed by the word address it is to read. After the word address acknowledge, the master immediately reissues the start condition and the slave address with the R/$\overline{W}$ bit set to one. This will be followed by an acknowledge from the X24C02 and then by the eight bit word. The read operation is terminated by the master by not responding with an acknowledge, and issuing a stop condition. Refer to Figure 8 for the address, acknowledge and data transfer sequence.

Figure 8. Random Read



Sequential Read

Sequential Read can be initiated as either a current address read or random access read. The first word is transmitted as with the other modes, however, the master now responds with an acknowledge, indicating it requires additional data. The X24C02 continues to output data for each acknowledge received. The read operation is terminated by the master; by not responding with an acknowledge and by issuing a stop condition.

The data output is sequential, with the data from address n followed by the data from n + 1. The address counter for read operations increments all address bits, allowing the entire memory contents to be serially read during one operation. At the end of the address space (address 255), the counter "rolls over" to address 0 and the X24C02 continues to output data for each acknowledge received. Refer to Figure 9 for the address, acknowledge and data transfer sequence.

Figure 9. Sequential Read

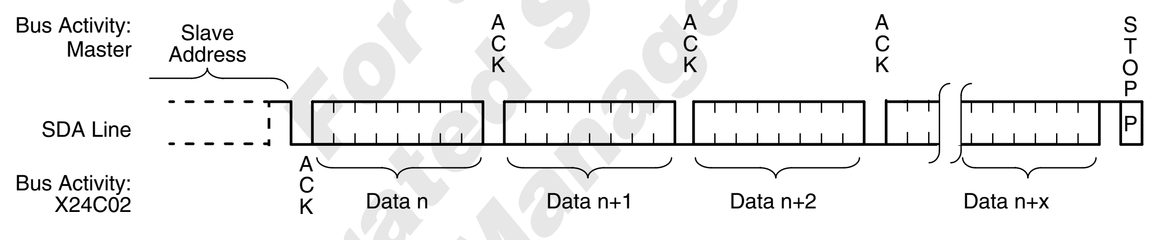
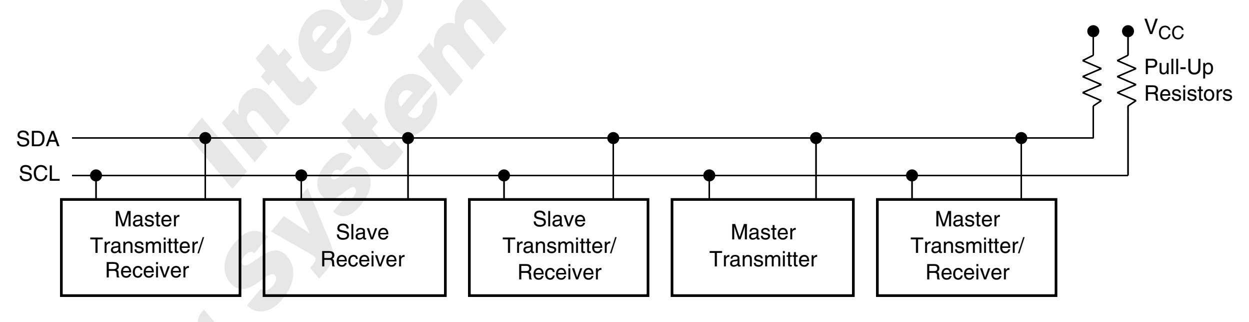


Figure 10. Typical System Configuration



ABSOLUTE MAXIMUM RATINGS

Temperature under bias ....–65 to +135°C
Storage temperature ....–65 to +150°C
Voltage on any pin with
respect to V_{SS} ....–1.0V to +7.0V
D.C. output current .... 5 mA
Lead temperature (soldering, 10 Seconds) ....300°C

COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only; functional operation of the device (at these or any other conditions above those indicated in the operational sections of this specification) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	70°C
Industrial	–40°C	+85°C

Supply Voltage	Limits
X24C02-2.7	2.7V to 5.5V

D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified)

Symbol	Parameter	Limits		Unit	Test Conditions
		Min.	Max.		
I_{CC1}	V_{CC} supply current (Read)		1	mA	SCL = V_{CC} x 0.1/Vd x 0.9 Levels @ 100 kHz, SDA = Open, All Other Inputs = GND or V_{CC} – 0.3V
I_{CC2}	V_{CC} supply current (Write)		1.5		
$I_{SB}1^{(1)}$	V_{CC} standby current		10	µA	SCL = SDA = V_{CC} – 0.3V, All Other Inputs = GND or V_{CC}, V_{CC} = 5.5V
I_{LI}	Input leakage current		10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output leakage current		10	µA	V_{OUT} = GND to V_{CC}
$V_{IL}^{(2)}$	Input low voltage	–1.0	V_{CC} x 0.3	V	
$V_{IH}^{(2)}$	Input high voltage	V_{CC} x 0.7	V_{CC} + 0.5	V	
V_{OL}	Output low voltage		0.4	V	I_{OL} = 3 mA, $V_{CC} \geq 2.7V$

CAPACITANCE $T_A = 25°C$, f = 1.0MHz, V_{CC} = 5V

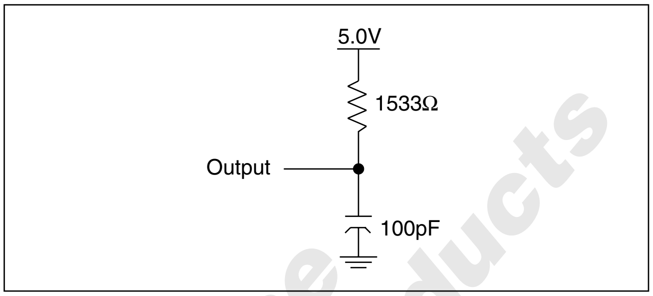
Symbol	Parameter	Max.	Unit	Test Conditions
$C_{I/O}^{(3)}$	Input/output capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
$C_{IN}^{(3)}$	Input capacitance (A_0, A_1, A_2, SCL)	6	pF	V_{IN} = 0V

Notes: (1) Must perform a stop command prior to measurement.
(2) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(3) This parameter is periodically sampled and not 100% tested.

A.C. CONDITIONS OF TEST

Input pulse levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input rise and fall times	10 ns
Input and output timing levels	V_{CC} x 0.5

EQUIVALENT A.C. LOAD CIRCUIT



A.C. CHARACTERISTICS (over recommended operating conditions unless otherwise specified)

Read & Write Cycle Limits

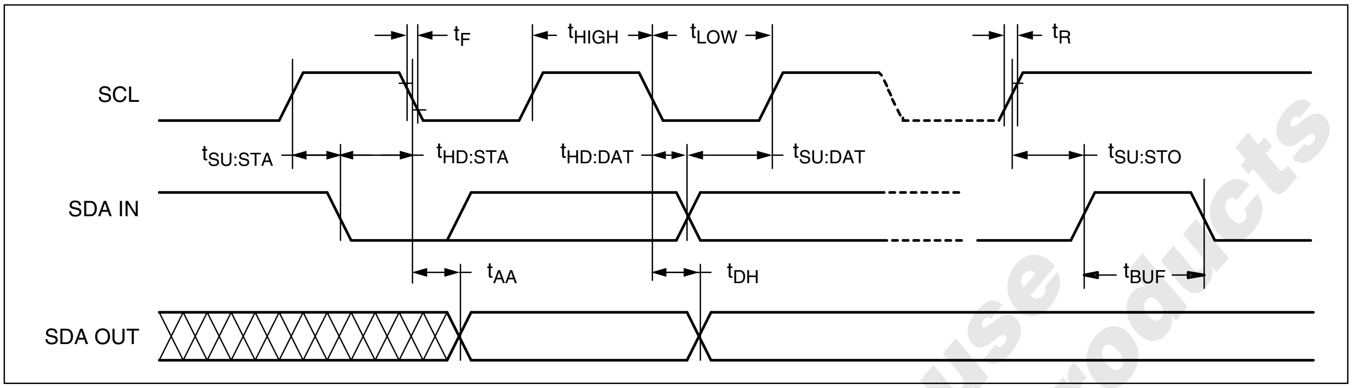
Symbol	Parameter	Min.	Max.	Unit
f_{SCL}	SCL clock frequency	0	400	kHz
T_I	Noise suppression time constant at SCL, SDA inputs	50		ns
td	SCL low to SDA data out valid	0.1	0.9	µs
t_{BUF}	Time the bus must be free before a new transmission can start	1.2		µs
$t_{HD:STA}$	Start condition hold time	0.6		µs
t_{LOW}	Clock low period	1.2		µs
t_{HIGH}	Clock high period	0.6		µs
$t_{SU:STA}$	Start condition setup time (for a repeated start condition)	0.6		µs
$t_{HD:DAT}$	Data In hold time	0		µs
$t_{SU:DAT}$	Data In setup time	100		ns
t_R	SDA and SCL rise time		300	µs
t_F	SDA and SCL fall time		300	ns
$t_{SU:STO}$	Stop condition setup time	0.6		µs
t_{DH}	Data out hold time	50	300	ns

POWER-UP TIMING

Symbol	Parameter	Max.	Unit
t_{PUR}(4)	Power-up to read operation	1	ms
t_{PUW}(4)	Power-up to write operation	5	ms

Note: (4) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.

Bus Timing



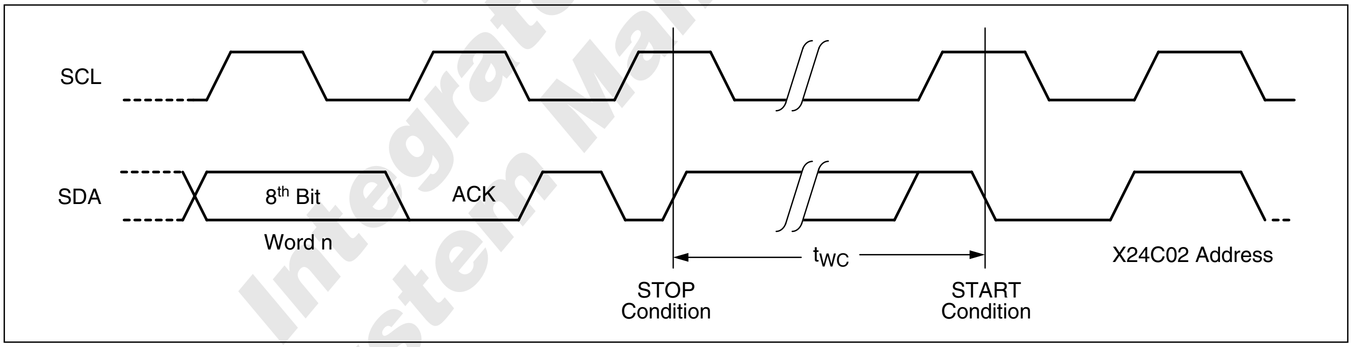
Write Cycle Limits

Symbol	Parameter	Min.	Typ.(5)	Max.	Unit
t_{WC}(6)	Write Cycle Time		5	10	ms

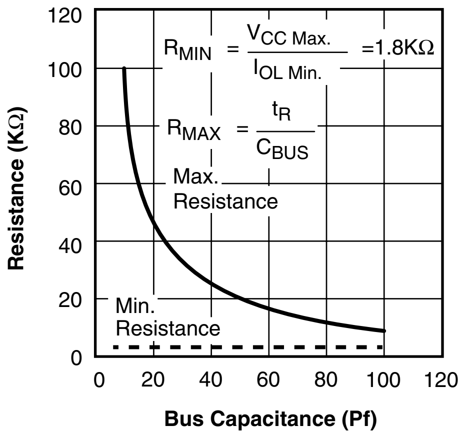
Notes: (5) Typical values are for T_A = 25°C and nominal supply voltage (5V).
(6) t_{WR} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.

The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal erase/write cycle. During the write cycle, the X24C02 bus interface circuits are disabled, SDA is allowed to remain HIGH, and the device does not respond to its slave address.

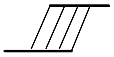
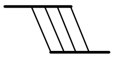
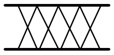
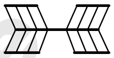
Write Cycle Timing



Guidelines for Calculating Typical Values of Bus Pull-Up Resistors

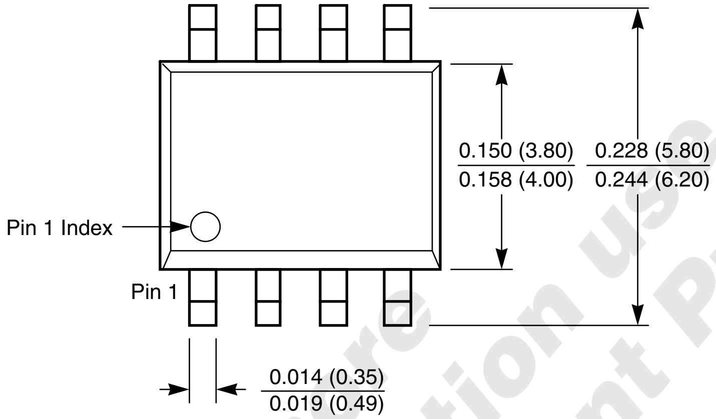


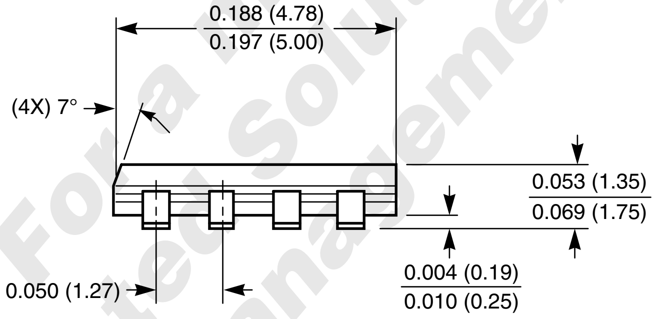
SYMBOL TABLE

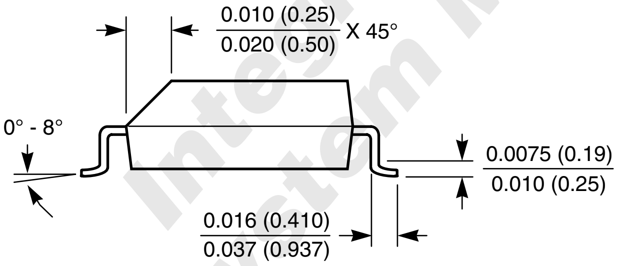
WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don’t Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

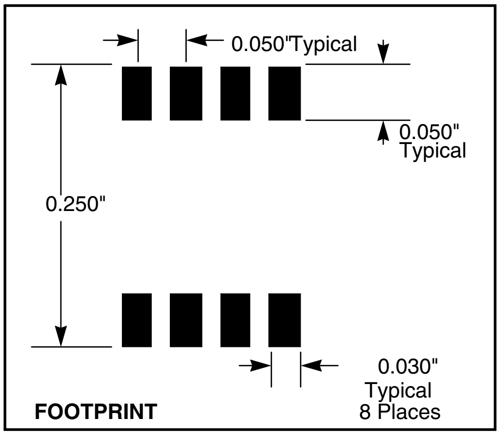
PACKAGING INFORMATION

8-Lead Plastic Small Outline Gull Wing Package Type S



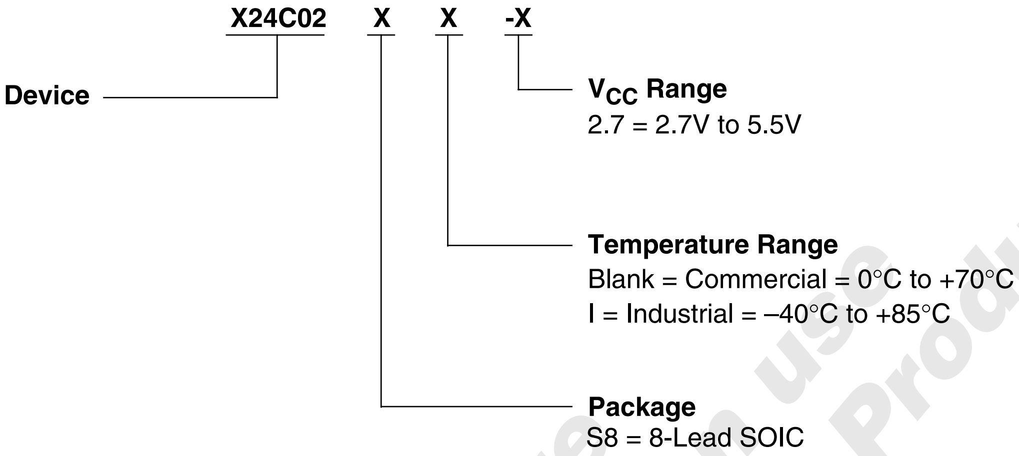




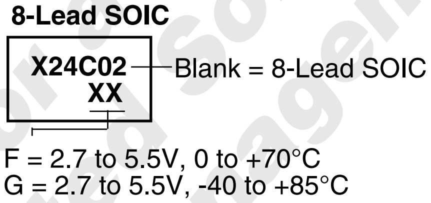


NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

Ordering Information



Part Mark Convention



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Xicor products are covered by one or more of the following U.S. Patents: 4,326,134; 4,393,481; 4,404,475; 4,450,402; 4,486,769; 4,488,060; 4,520,461; 4,533,846; 4,599,706; 4,617,652; 4,668,932; 4,752,912; 4,829,482; 4,874,967; 4,883,976; 4,980,859; 5,012,132; 5,003,197; 5,023,694; 5,084,667; 5,153,880; 5,153,691; 5,161,137; 5,219,774; 5,270,927; 5,324,676; 5,434,396; 5,544,103; 5,587,573; 5,835,409; 5,977,585. Foreign patents and additional patents pending.

LIFE RELATED POLICY

In situations where semiconductor component failure may endanger life, system designers using this product should design the system with appropriate error detection and correction, redundancy and back-up features to prevent such an occurrence.

Xicor's products are not authorized for use in critical components in life support devices or systems.

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

Product Change Notice : PCN February 4, 2000

February 4, 2000
Ref: PCN-00-01

Dear Xicor Customer,

At Xicor, we continuously strive to improve the performance and efficiency of our operations, and the quality of our products. Consistent with this effort, we are currently adding additional wafer fabrication capacity for various IIC and SPI serial products.

This added wafer fabrication capacity will complement current operations and will expand Xicor's capabilities to accommodate future growth.

In addition, several of the IIC and SPI serial products are undergoing a die revision change. The new die revision is functionally and pin to pin compatable with the existing die revision.

See the detailed product number list below for the implementation date and description of the change. Samples for qualification will be available approximately 4 weeks before the implementation date. Qualification data is available upon request.

If you have any further questions, please contact your regional Xicor sales office.

Sincerely,

Xicor Marketing Department

Xicor Part Number	**Implement Date**	**Description of Change**
IIC Serial Products		
X24164P	2/28/00	Foundry Change
X24164P-3	2/28/00	Foundry Change
X24164PI	2/28/00	Foundry Change
X24164PI-3	2/28/00	Foundry Change
X24164S	2/28/00	Foundry Change
X24164S-2.7	2/28/00	Foundry Change
X24164S-3	2/28/00	Foundry Change
X24164SI	2/28/00	Foundry Change
X24164SI-2.7	2/28/00	Foundry Change
X24C04P	5/31/00	Die Rev / Foundry Change
X24C04P-2.7	5/31/00	Die Rev / Foundry Change
X24C04P-3	5/31/00	Die Rev / Foundry Change
X24C04P-3.5	5/31/00	Die Rev / Foundry Change
X24C04PI	5/31/00	Die Rev / Foundry Change
X24C04PI-2.7	5/31/00	Die Rev / Foundry Change

X24C04PI-3	5/31/00	Die Rev / Foundry Change
X24C04PI-3.5	5/31/00	Die Rev / Foundry Change
X24C04PM	5/31/00	Die Rev / Foundry Change
X24C04PM-3	5/31/00	Die Rev / Foundry Change
X24C04PM-3.5	5/31/00	Die Rev / Foundry Change
X24C04S14	5/31/00	Die Rev / Foundry Change
X24C04S14-3	5/31/00	Die Rev / Foundry Change
X24C04S14-3.5	5/31/00	Die Rev / Foundry Change
X24C04S14I	5/31/00	Die Rev / Foundry Change
X24C04S14I-3	5/31/00	Die Rev / Foundry Change
X24C04S14I-3.5	5/31/00	Die Rev / Foundry Change
X24C04S14M	5/31/00	Die Rev / Foundry Change
X24C04S14M-3	5/31/00	Die Rev / Foundry Change
X24C04S14M-3.5	5/31/00	Die Rev / Foundry Change
X24C04S8	5/31/00	Die Rev / Foundry Change
X24C04S8-2.7	5/31/00	Die Rev / Foundry Change
X24C04S8-3	5/31/00	Die Rev / Foundry Change
X24C04S8-3.5	5/31/00	Die Rev / Foundry Change
X24C04S8I	5/31/00	Die Rev / Foundry Change
X24C04S8I-2.7	5/31/00	Die Rev / Foundry Change
X24C04S8I-3	5/31/00	Die Rev / Foundry Change
X24C04S8I-3.5	5/31/00	Die Rev / Foundry Change
X24C04S8M	5/31/00	Die Rev / Foundry Change
X24C04S8M-3	5/31/00	Die Rev / Foundry Change
X24C04S8M-3.5	5/31/00	Die Rev / Foundry Change
X24C08P	8/31/00	Die Rev / Foundry Change
X24C08P-2.7	8/31/00	Die Rev / Foundry Change
X24C08P-3	8/31/00	Die Rev / Foundry Change
X24C08P-3.5	8/31/00	Die Rev / Foundry Change
X24C08PI	8/31/00	Die Rev / Foundry Change
X24C08PI-2.7	8/31/00	Die Rev / Foundry Change
X24C08PI-3	8/31/00	Die Rev / Foundry Change
X24C08PI-3.5	8/31/00	Die Rev / Foundry Change
X24C08PM	8/31/00	Die Rev / Foundry Change
X24C08PM-3	8/31/00	Die Rev / Foundry Change
X24C08PM-3.5	8/31/00	Die Rev / Foundry Change
X24C08S	8/31/00	Die Rev / Foundry Change
X24C08S-3	8/31/00	Die Rev / Foundry Change
X24C08S-3.5	8/31/00	Die Rev / Foundry Change
X24C08S8	8/31/00	Die Rev / Foundry Change
X24C08S8-2.7	8/31/00	Die Rev / Foundry Change
X24C08S8-3	8/31/00	Die Rev / Foundry Change
X24C08S8I	8/31/00	Die Rev / Foundry Change
X24C08S8I-2.7	8/31/00	Die Rev / Foundry Change

X24C08S8I-3	8/31/00	Die Rev / Foundry Change
X24C08S8M	8/31/00	Die Rev / Foundry Change
X24C08SI	8/31/00	Die Rev / Foundry Change
X24C08SI-3	8/31/00	Die Rev / Foundry Change
X24C08SI-3.5	8/31/00	Die Rev / Foundry Change
X24C08SM	8/31/00	Die Rev / Foundry Change
X24C08SM-3	8/31/00	Die Rev / Foundry Change
X24C08SM-3.5	8/31/00	Die Rev / Foundry Change
SPI Serial Products		
X25020P	7/31/00	Die Rev / Foundry Change
X25020P-2.7	7/31/00	Die Rev / Foundry Change
X25020PI	7/31/00	Die Rev / Foundry Change
X25020PI-2.7	7/31/00	Die Rev / Foundry Change
X25020S	7/31/00	Die Rev / Foundry Change
X25020S-2.7	7/31/00	Die Rev / Foundry Change
X25020S-3	7/31/00	Die Rev / Foundry Change
X25020SI	7/31/00	Die Rev / Foundry Change
X25020SI-2.7	7/31/00	Die Rev / Foundry Change
X25020SI-3	7/31/00	Die Rev / Foundry Change
X25040P	7/31/00	Die Rev / Foundry Change
X25040P-2.7	7/31/00	Die Rev / Foundry Change
X25040PI	7/31/00	Die Rev / Foundry Change
X25040PI-2.7	7/31/00	Die Rev / Foundry Change
X25040S	7/31/00	Die Rev / Foundry Change
X25040S-2.7	7/31/00	Die Rev / Foundry Change
X25040SI	7/31/00	Die Rev / Foundry Change
X25040SI-2.7	7/31/00	Die Rev / Foundry Change
X25040SM	7/31/00	Die Rev / Foundry Change
X25160S	8/31/00	Foundry Change
X25160S-2.7	8/31/00	Foundry Change
X25160SI	8/31/00	Foundry Change
X25160SI-2.7	8/31/00	Foundry Change
X25320P	8/31/00	Foundry Change
X25320S	8/31/00	Foundry Change
X25320S-2.7	8/31/00	Foundry Change
X25320SI	8/31/00	Foundry Change
X25320SI-2.7	8/31/00	Foundry Change

February 4, 2000

Dear Xicor Customer,

At Xicor, we continuously strive to improve the performance and efficiency of our operations, and the quality of our products. Consistent with this effort, we are revising the tape and reel "T" codes to eliminate partial reel quantities.

See the detailed tape and reel "T" codes definitions list and definitions matrix below . The implementation date for the new tape and reel "T" codes is March 1, 2000. All existing orders with shipment dates on or after March 1, 2000 will be converted to the new tape and reel "T" codes. All new orders on or after March 1, 2000 must use the new tape and reel "T" codes.

If you have any further questions, please contact your regional Xicor sales office.

Sincerely,

Xicor Marketing Department

Tape and Reel "T" Code Definitions

CODE	**PACKAGE**	**QTY**	**REQUIREMENTS**	**REEL SIZE**
T1	SOIC (150 MIL SOIC) "S"	=2500	Tape and Reel	13"
T1	SOIC (300 MIL SOIC) "S"	=1000	Tape and Reel	13"
T1	EIAJ (WIDE SOIC) "A"	=2000	Tape and Reel	13"
T1	TSOP (THIN SOIC) "T"	=1000	Tape and Reel	13"
T1	PLCC "J"	=750	Tape and Reel	13"
T1	MSOP "M"	=2500	Tape and Reel	13"
T1	GULL WING "R"	=500	Tape and Reel	13"
T1	TSSOP "V"	=2500	Tape and Reel	13"
T1	XBGA "B" or "Z"	=10000	Tape and Reel	13"
T2	SOIC (150 MIL SOIC) "S"	=1000	Tape and Reel	7"
T2	SOIC (300 MIL SOIC) "S"	=500	Tape and Reel	13"
T2	EIAJ (WIDE SOIC) "A"	=1000	Tape and Reel	7"

T2	TSOP (THIN SOIC) "T"	=500	Tape and Reel	13"
T2	PLCC "J"	=500	Tape and Reel	13"
T2	MSOP "M"	=1000	Tape and Reel	7"
T2	GULL WING "R"	=250	Tape and Reel	13"
T2	TSSOP "V"	=1000	Tape and Reel	7"
T2	XBGA "B" or "Z"	=5000	Tape and Reel	13"
T3	SOIC (150 MIL SOIC) "S"	=2500	Tape and Reel & Dry Pack	13"
T3	SOIC (300 MIL SOIC) "S"	=1000	Tape and Reel & Dry Pack	13"
T3	EIAJ (WIDE SOIC) "A"	=2000	Tape and Reel & Dry Pack	13"
T3	TSOP (THIN SOIC) "T"	=1000	Tape and Reel & Dry Pack	13"
T3	PLCC "J"	=750	Tape and Reel & Dry Pack	13"
T3	MSOP "M"	=2500	Tape and Reel & Dry Pack	13"
T3	GULL WING "R"	=500	Tape and Reel & Dry Pack	13"
T3	TSSOP "V"	=2500	Tape and Reel & Dry Pack	13"
T3	XBGA "B" or "Z"	=10000	Tape and Reel & Dry Pack	13"
T4	SOIC (150 MIL SOIC) "S"	=1000	Tape and Reel & Dry Pack	7"
T4	SOIC (300 MIL SOIC) "S"	=500	Tape and Reel & Dry Pack	13"
T4	EIAJ (WIDE SOIC) "A"	=1000	Tape and Reel & Dry Pack	7"
T4	TSOP (THIN SOIC) "T"	=500	Tape and Reel & Dry Pack	13"
T4	PLCC "J"	=500	Tape and Reel & Dry Pack	13"
T4	MSOP "M"	=1000	Tape and Reel & Dry Pack	7"
T4	GULL WING "R"	=250	Tape and Reel & Dry Pack	13"
T4	TSSOP "V"	=1000	Tape and Reel & Dry Pack	7"
T4	XBGA "B" or "Z"	=5000	Tape and Reel & Dry Pack	13"
T5	MSOP "M"	=3500	Tape and Reel	13"
T5	TSSOP "V"	=3500	Tape and Reel	13"
T5	XBGA "B" or "Z"	=2500	Tape and Reel	13"
T6	MSOP "M"	=3500	Tape and Reel & Dry Pack	13"
T6	TSSOP "V"	=3500	Tape and Reel & Dry Pack	13"
T6	XBGA "B" or "Z"	=2500	Tape and Reel & Dry Pack	13"

T6	XBGA "B" or "Z"	=2500	Tape and Reel & Dry Pack	13
T7	ALL PACKAGES	ALL QTYS.	Dry Pack	N/A

Tape and Reel "T" Code Definition Matrix

150 MIL SOIC "S" (8L, 14L,16L)			
Code	2500	1000	Dry Pack
T1	x	x	x
T2	x	x	x
T3	x		x
T4	x	x	x
T7*	x	x	x

*NOTE: DRY PACK ONLY

TSOP THIN SOIC "T"			
Code	1000	500	Dry Pack
T1	x	x	x
T2	x	x	x
T3	x	x	x
T4	x	x	x
T7*	x	x	x

*NOTE: DRY PACK ONLY

GULL WING "R"			
Code	500	250	Dry Pack
T1	x	x	x
T2	x	x	x
T3	x	x	X
T4	x	x	X
T7*	x	x	x

*NOTE: DRY PACK ONLY

300 MIL SOIC "S" (20L, 24L, 28L)			
Code	1000	500	Dry Pack
T1	X	x	x
T2	x	X	x
T3	X	x	X
T4	x	X	X
T7*	x	x	X

*NOTE: DRY PACK ONLY

XBGA "B" or "Z"				
Code	10000	5000	2500	Dry Pack
T1	x	x	x	x
T2	x	x	x	x
T3	x	x	x	x
T4	x	x	x	x
T5	x	x	x	x
T6	x	x	x	x
T7*	x	x	x	x

*NOTE: DRY PACK ONLY

EIAJ "A"			
Code	2000	1000	Dry Pack
T1	x	x	x
T2	x	x	x
T3	x	x	x
T4	x	x	x
T7*	x	x	x

*NOTE: DRY PACK ONLY

PLCC "J"			
Code	750	500	Dry Pack
T1	x	x	x
T2	x	x	x
T3	x	x	X
T4	x	x	X
T7*	x	x	X

*NOTE: DRY PACK ONLY

TSSOP "V"				
Code	2500	1000	3500	Dry Pack
T1	x	x	x	x
T2	x	x	x	x
T3	x	x	x	x
T4	x	x	x	x
T5	x	x	x	x
T6	x	x	x	x
T7*	x	x	x	x

*NOTE: DRY PACK ONLY

MSOP "M"				
Code	2500	1000	3500	Dry Pack
T1	x	x	x	x
T2	x	x	x	x
T3	x	x	x	x
T4	x	x	x	x
T5	x	x	x	x
T6	x	x	x	x

T7*	x	x	x	x

*NOTE: DRY PACK ONLY

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