DRAM

8 MEG x 8

3.3V, BURST EDO

FEATURES

- Burst order, interleave or linear, programmed by executing WCBR cycle after initialization
- Single +3.3V ±5% power supply
- Industry-standard x16 pinout and package
- 13 row-addresses, 10 column-addresses (W4) or 12 row-addresses, 11 column-addresses (W5)
- High-performance CMOS silicon-gate process
- All inputs and outputs are LVTTL-compatible
- 4,096-cycle $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) REFRESH distributed across 64ms
- Four-cycle Extended Data-Out (EDO) burst accesses

OPTIONS — MARKING

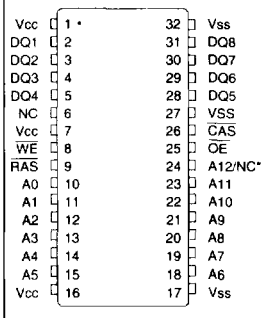
- Timing
  - 52ns access; 15ns cycle — -52
  - 60ns access; 16.6ns cycle — -60
- Packages
  - Plastic SOJ (400 mil) — DJ
  - Plastic TSOP (400 mil) — TG*
- Part Number Example: MT4LC8M8W4DJ-52

KEY TIMING PARAMETERS

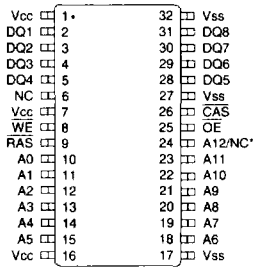
SPEED	^tRAC	^tPC	^tCAC	^tCOH	^tDS	^tDH
-52	52ns	15ns	10ns	3ns	0ns	5ns
-60	60ns	16.6ns	11ns	3ns	0ns	5ns

PIN ASSIGNMENT (Top View)

32-Pin SOJ (DA-5)



32-Pin TSOP (DB-4)**



*A12 = W4 version, NC = W5 version
**Consult factory for availability

GENERAL DESCRIPTION

The MT4LC8M8W4 and MT4LC8M8W5 are high-speed CMOS dynamic random access memory devices containing 67,108,864 bits, and designed to operate at 3.3V ±5%. The MT4LC8M8W4 and MT4LC8M8W5 are functionally organized as 8,388,608 locations containing 8 bits each. The 8,388,608 memory locations are arranged in 8,192 rows by 1,024 columns for the MT4LC8M8W4 or 4,096 rows by 2,048 columns for the MT4LC8M8W5. During READ or WRITE cycles, each location is uniquely addressed via the address bits.

The MT4LC8M8W4 and MT4LC8M8W5 are burst access DRAMs in which all READ and WRITE access cycles occur in bursts of four. The bursts wrap around on a 4-byte boundary. This means that the two least significant bits of the $\overline{CAS}$ address are modified internally to produce each address of the burst sequence. The burst type, interleave or linear, is determined by executing a WCBR cycle (CBR cycle with $\overline{WE}$ LOW) with address A0 set to either HIGH or LOW. A0 LOW will program the device to execute linear bursts, A0 HIGH will program the bursts to be interleave. For future compatability it is strongly recommended that the information (0010 000x) where x=A0 is supplied on addresses A7-A0 during the WCBR cycle. The WCBR cycle must be followed by a $\overline{RAS}$-ONLY or CBR REFRESH cycle to exit this programming mode. $\overline{RAS}$ HIGH and $\overline{CAS}$ HIGH terminates burst operations in the selected row, resets the burst counter, closes that row and decreases chip current to a reduced standby level. The chip is precharged for the next access during the $\overline{RAS}$ HIGH time.

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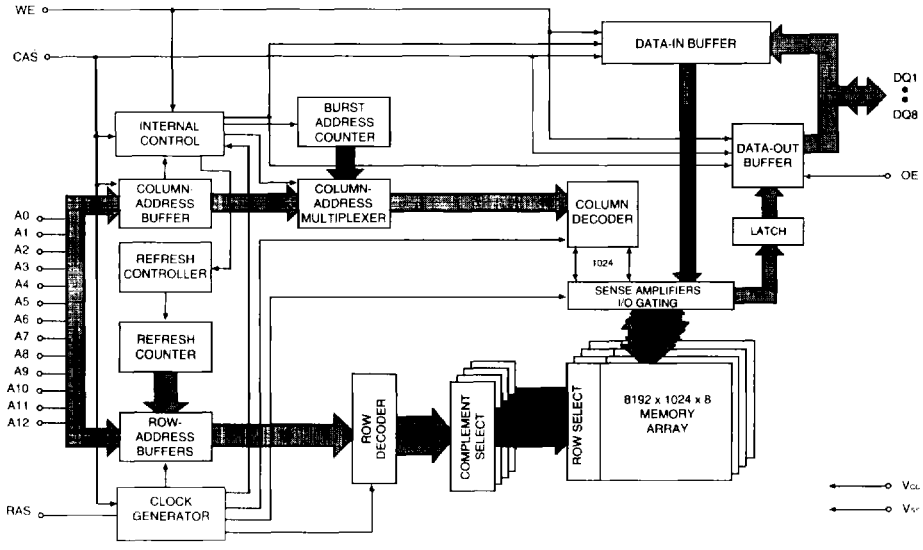
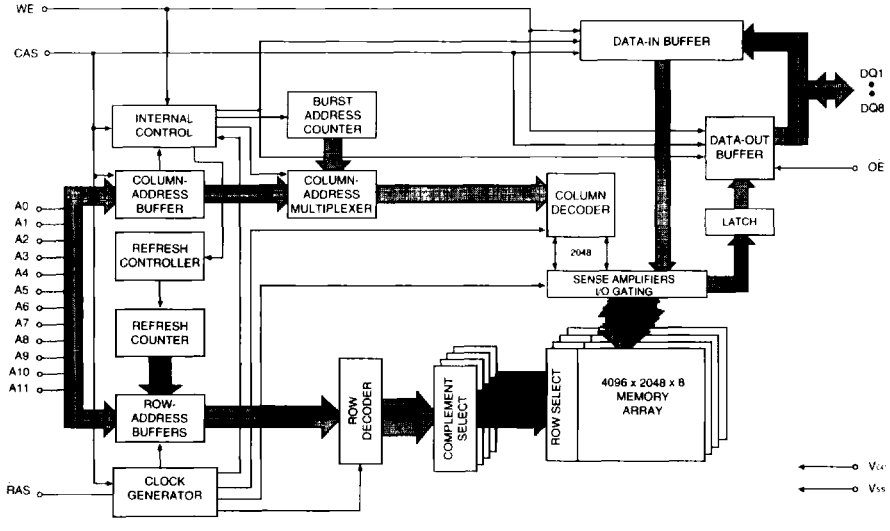
FUNCTIONAL BLOCK DIAGRAM
MT4LC8M8W4 (13 row-addresses)



FUNCTIONAL BLOCK DIAGRAM



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