DDR2 SDRAM REGISTERED DIMM

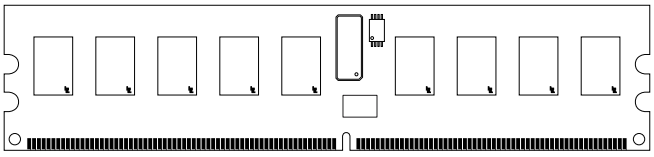
MT18HTF6472D – 512MB
MT18HTF12872D – 1GB (ADVANCE‡)
MT18HTF25672D – 2GB(ADVANCE‡)

For the latest data sheet, please refer to the Micron® Web site: www.micron.com/moduleds

Features

- 240-pin, dual in-line memory module (DIMM)
- Fast data transfer rates: PC2-3200 or PC2-4300
- Utilizes 400 MT/s and 533 MT/s DDR SDRAM components
- 512MB (64 Meg x 72), 1GB (128 Meg x 72) 2GB (256 Meg x 72)
- V_{DD} = +1.8V ±0.1V, $V_{DD}Q$ = +1.8V ±0.1V
- V_{DDSPD} = +1.7V to +3.6V
- JEDEC standard 1.8V I/O (SSTL_18-compatible)
- Differential data strobe (DQS, DQS#) option
- Four-bit prefetch architecture
- Differential clock inputs (CK, CK#)
- Commands entered on each rising CK edge
- DQS edge-aligned with data for READs
- DQS center-aligned with data for WRITEs
- DLL to align DQ and DQS transitions with CK
- Four or eight internal device banks for concurrent operation
- Data mask (DM) for masking write data
- Programmable CAS# latency (CL): 3 and 4
- Posted CAS# additive latency (AL): 0, 1, 2, 3, and 4
- WRITE latency = READ latency - 1 ^{t}CK
- Programmable burst lengths: 4 or 8
- READ burst interrupt supported by another READ
- WRITE burst interrupt supported by another WRITE
- Adjustable data-output drive strength
- Concurrent auto precharge option is supported
- Auto Refresh (CBR) and Self Refresh Mode
- 7.8125µs maximum average periodic refresh interval
- 64ms, 8,192-cycle refresh

Figure 1: 240-Pin DIMM (MO-206 R/C "B")



- Off-chip driver (OCD) impedance calibration
- On-die termination (ODT)
- Serial Presence Detect (SPD) with EEPROM
- Gold edge contacts

OPTIONS	MARKING
• Package	
240-pin DIMM (standard)	G
240-pin DIMM (lead-free)[1]	Y
• Frequency/CAS Latency[2]	
3.75ns @ CL = 4 (DDR2-533)	-53E
5.0ns @ CL = 3 (DDR2-400)	-40E

NOTE: 1. Consult factory for availability of lead-free products.
2. CL = CAS (READ) Latency.

Table 1: Address Table

	512MB	1GB	2GB
Refresh Count	8K	8K	8K
Row Addressing	8K (A0–A12)	16K (A0–A13)	16K (A0–A13)
Device Bank Addressing	4 (BA0, BA1)	4 (BA0, BA1)	8 (BA0, BA1, BA2)
Device Configuration	256Mb (32 Meg x 8)	512Mb (64 Meg x 8)	1Gb (128 Meg x 8)
Column Addressing	1K (A0–A9)	1K (A0–A9)	1K (A0–A9)
Module Rank Addressing	2 (S0#, S1#)	2 (S0#, S1#)	2 (S0#, S1#)

Table 1: Key Timing Parameters

SPEED GRADE	DATA RATE (MHz)		^{t}RCD (ns)	^{t}RP (ns)	^{t}RC (ns)
	CL = 3	CL = 4			
-53E	400	533	15	15	60
-40E	400	400	15	15	60

Table 2: Part Numbers and Timing Parameters

PART NUMBER[1]	MODULE DENSITY	CONFIGURATION	MODULE BANDWIDTH	MEMORY CLOCK/ DATA RATE	LATENCY (CL - ^{t}RCD - ^{t}RP)
MT18HTF6472DG-40E__	512MB	64 Meg x 72	3.2 GB/s	5.0ns/400 MT/s	3-3-3
MT18HTF6472DY-40E__	512MB	64 Meg x 72	3.2 GB/s	5.0ns/400 MT/s	3-3-3
MT18HTF6472DG-53E__	512MB	64 Meg x 72	4.3 GB/s	3.75ns/533 MT/s	4-4-4
MT18HTF6472DY-53E__	512MB	64 Meg x 72	4.3 GB/s	3.75ns/533 MT/s	4-4-4
MT18HTF12872DG-40E__[2]	1GB	128 Meg x 72	3.2 GB/s	5.0ns/400 MT/s	3-3-3
MT18HTF12872DY-40E__[2]	1GB	128 Meg x 72	3.2 GB/s	5.0ns/400 MT/s	3-3-3
MT18HTF12872DG-53E__[2]	1GB	128 Meg x 72	4.3 GB/s	3.75ns/533 MT/s	4-4-4
MT18HTF12872DY-53E__[2]	1GB	128 Meg x 72	4.3 GB/s	3.75ns/533 MT/s	4-4-4
MT18HTF25672DG-40E__[2]	2GB	256 Meg x 72	3.2 GB/s	5.0ns/400 MT/s	3-3-3
MT18HTF25672DY-40E__[2]	2GB	256 Meg x 72	3.2 GB/s	5.0ns/400 MT/s	3-3-3
MT18HTF25672DG-53E__[2]	2GB	256 Meg x 72	4.3 GB/s	3.75ns/533 MT/s	4-4-4
MT18HTF25672DY-53E__[2]	2GB	256 Meg x 72	4.3 GB/s	3.75ns/533 MT/s	4-4-4

NOTE:

1. All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT18HTF12872DG-40EC2.
2. Contact Micron for product availability.

Table 3: Pin Assignment (240-pin DIMM Front)

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	VREF	31	DQ19	61	A4	91	VSS
2	VSS	32	VSS	62	VDDQ	92	DQS5#
3	DQ0	33	DQ24	63	A2	93	DQS5
4	DQ1	34	DQ25	64	VDD	94	VSS
5	VSS	35	VSS	65	VSS	95	DQ42
6	DQS0#	36	DQS3#	66	VSS	96	DQ43
7	DQS0	37	DQS3	67	VDD	97	VSS
8	VSS	38	VSS	68	NC	98	DQ48
9	DQ2	39	DQ26	69	VDD	99	DQ49
10	DQ3	40	DQ27	70	A10/AP	100	VSS
11	VSS	41	VSS	71	BA0	101	SA2
12	DQ8	42	CB0	72	VDDQ	102	NC
13	DQ9	43	CB1	73	WE#	103	VSS
14	VSS	44	VSS	74	CAS#	104	DQS6#
15	DQS1#	45	DQS8#	75	VDDQ	105	DQS6
16	DQS1	46	DQS8	76	S1#	106	VSS
17	VSS	47	VSS	77	0DT1	107	DQ50
18	RESET#	48	CB2	78	VDDQ	108	DQ51
19	NC	49	CB3	79	VSS	109	VSS
20	VSS	50	VSS	80	DQ32	110	DQ56
21	DQ10	51	VDDQ	81	DQ33	111	DQ57
22	DQ11	52	CKE0	82	VSS	112	VSS
23	VSS	53	VDD	83	DQS4#	113	DQS7#
24	DQ16	54	BA2	84	DQS4	114	DQS7
25	DQ17	55	NC	85	VSS	115	VSS
26	VSS	56	VDDQ	86	DQ34	116	DQ58
27	DQS2#	57	A11	87	DQ35	117	DQ59
28	DQS2	58	A7	88	VSS	118	VSS
29	VSS	59	VDD	89	DQ40	119	SDA
30	DQ18	60	A5	90	DQ41	120	SCL

Table 4: Pin Assignment (240-pin DIMM Back)

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
121	VSS	151	VSS	181	VDDQ	211	DM5/DQS14
122	DQ4	152	DQ28	182	A3	212	NC/DQS14#
123	DQ5	153	DQ29	183	A1	213	VSS
124	VSS	154	VSS	184	VDD	214	DQ46
125	DM0/DQS9	155	DM3/DQS12	185	CK0	215	DQ47
126	NC/DQS9#	156	NC/DQS12#	186	CK0#	216	VSS
127	VSS	157	VSS	187	VDD	217	DQ52
128	DQ6	158	DQ30	188	A0	218	DQ53
129	DQ7	159	DQ31	189	VDD	219	VSS
130	VSS	160	VSS	190	BA1	220	RFU
131	DQ12	161	CB4	191	VDDQ	221	RFU
132	DQ13	162	CB5	192	RAS#	222	VSS
133	VSS	163	VSS	193	S0#	223	DM6/DQS15
134	DM1/DQS10	164	DM8/DQS17	194	VDDQ	224	NC/DQS15#
135	NC/DQS10#	165	NC/DQS17#	195	ODT0	225	VSS
136	VSS	166	VSS	196	NC/A13	226	DQ54
137	RFU	167	CB6	197	VDD	227	DQ55
138	RFU	168	CB7	198	VSS	228	VSS
139	VSS	169	VSS	199	DQ36	229	DQ60
140	DQ14	170	VDDQ	200	DQ37	230	DQ61
141	DQ15	171	CKE1	201	VSS	231	VSS
142	VSS	172	VDD	202	DM4/DQS13	232	DM7/DQS16
143	DQ20	173	NC	203	NC/DQS13#	233	NC/DQS16#
144	DQ21	174	NC	204	VSS	234	VSS
145	VSS	175	VDDQ	205	DQ38	235	DQ62
146	DM2/DQS11	176	A12	206	DQ39	236	DQ63
147	NC/DQS11#	177	A9	207	VSS	237	VSS
148	VSS	178	VDD	208	DQ44	238	VDDSPD
149	DQ22	179	A8	209	DQ45	239	SA0
150	DQ23	180	A6	210	VSS	240	SA1

NOTE:

Pin 196 is NC for 512MB, or A13 for 1GB and 2GB; pin 54 is NC for 512MB and 1GB, or BA2 for 2GB.

Figure 2: Pin Locations

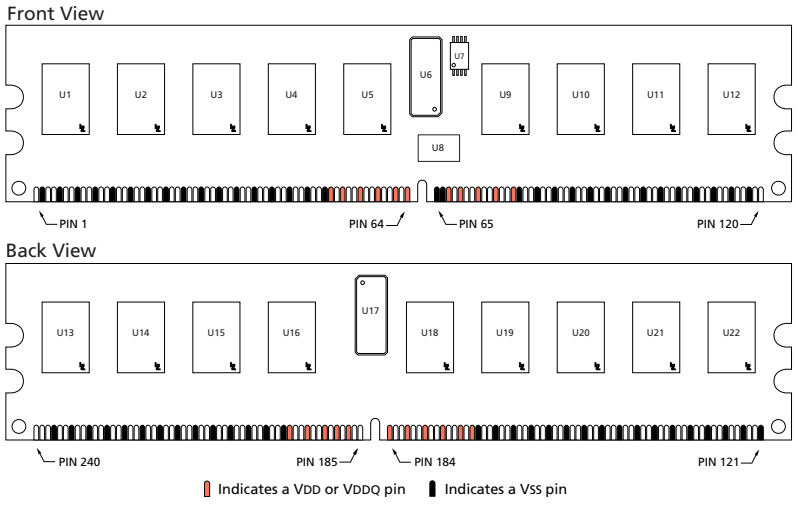


Table 5: Pin Descriptions

Pin numbers may not correlate with symbols. Refer to Pin Assignment tables on page 3 for more information

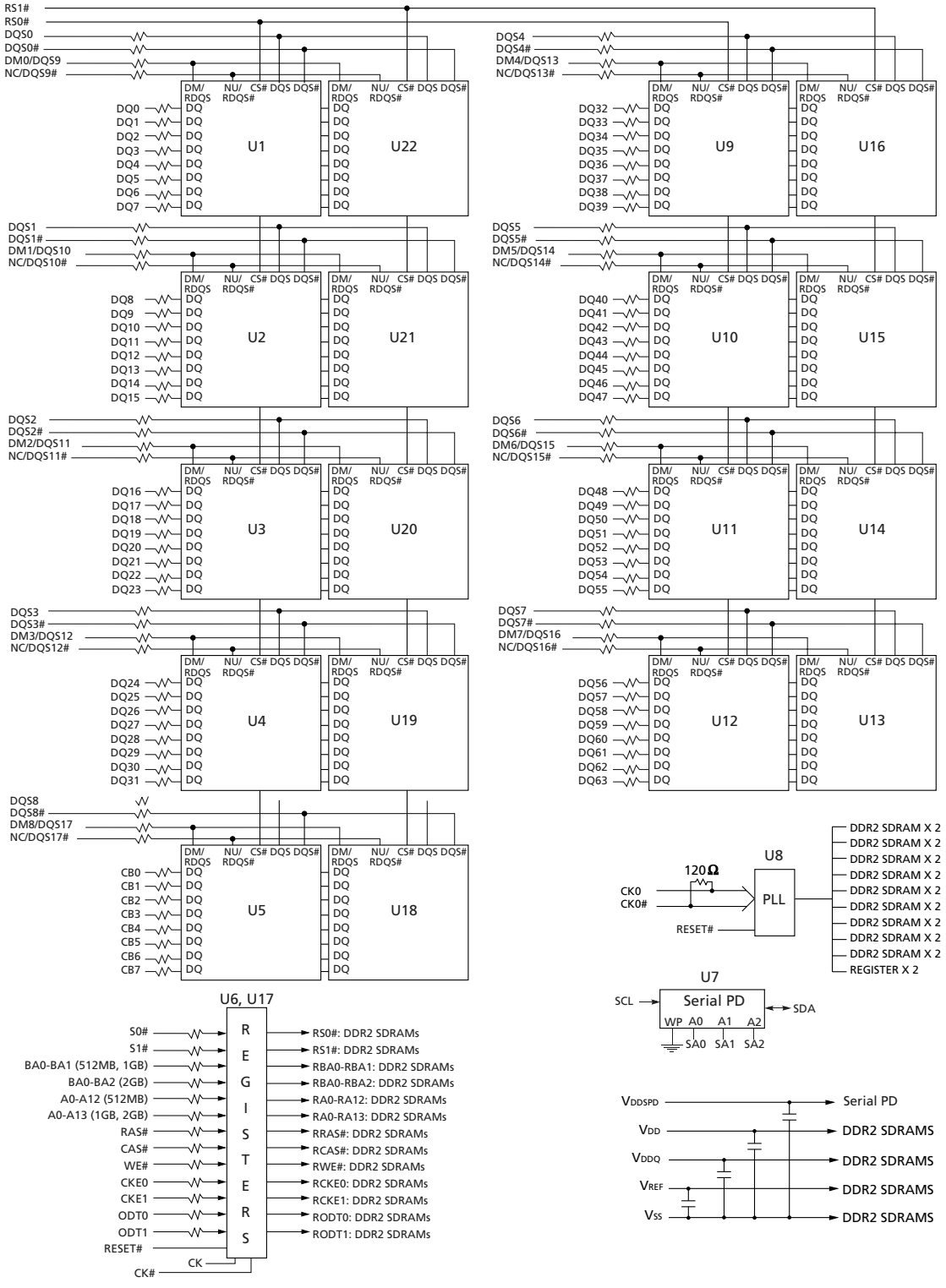
PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
77, 195	ODT0M ODT1	Input	On-Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to each of the following pins: DQ, DQS, DQS#, and DM. The ODT input will be ignored if disabled via the LOAD MODE command.
185, 186	CK0, CK0#	Input	Clock: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Output data (DQs and DQS/DQS#) is referenced to the crossings of CK and CK#.
52, 171	CKE0, CKE1	Input	Clock Enable: CKE (registered HIGH) activates and CKE (registered LOW) deactivates clocking circuitry on the DDR2 SDRAM. The specific circuitry that is enabled/disabled is dependent on the DDR2 SDRAM configuration and operating mode. CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all device banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any device bank). CKE is synchronous for POWER-DOWN entry, POWER-DOWN exit, output disable, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit. Input buffers (excluding CK, CK#, CKE, and ODT) are disabled during POWER-DOWN. Input buffers (excluding CKE) are disabled during SELF REFRESH. CKE is an SSTL_18 input but will detect a LVCMOS LOW level once V_{DD} is applied during first power-up. After Vref has become stable during the power on and initialization sequence, it must be maintained for proper operation of the CKE receiver. For proper self-refresh operation V_{REF} must be maintained to this input.
76, 193	S0#, S1#	Input	Chip Select: S# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when S# is registered HIGH. S# provides for external rank selection on systems with multiple ranks. S# is considered part of the command code.
73, 74, 192	RAS#, CAS#, WE#	Input	Command Inputs: RAS#, CAS#, and WE# (along with S#) define the command being entered.
54 (2GB), 71, 190	BA0, BA1, BA2 (2GB)	Input	Bank Address Inputs: define to which device bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA0–BA2 define which mode register including MR, EMR, EMR(2), and EMR(3) is loaded during the LOAD MODE command.
57, 58, 60, 61, 63, 70, 176, 177, 179, 180, 182, 183, 188, 196 (2GB)	A0–A12 (512MB) A0-A13 (1GB, 2GB)	Input	Address Inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for Read/Write commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA0–BA2) or all device banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command.
125, 134, 146, 155, 164, 202, 211, 223, 232	DM0–DM8	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading is designed to match that of DQ and DQS pins.

Table 5: Pin Descriptions

Pin numbers may not correlate with symbols. Refer to Pin Assignment tables on page 3 for more information

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
3, 4, 9, 10, 12, 13, 21, 22, 24, 25, 30, 31, 33, 34, 39, 40, 80, 81, 86, 87, 89, 90, 95, 96, 98, 99, 107, 108, 110, 111, 116, 117, 122, 123, 128, 129, 131, 132, 140, 141, 143, 144, 149, 150, 152, 153, 158, 159, 199, 200, 205, 206, 208, 209, 214, 215, 217, 218, 226, 227, 229, 230, 235, 236	DQ0–DQ63	I/O	Data Input/Output: Bidirectional data bus.
6, 7, 15, 16, 27, 28, 36, 37, 45, 46, 83, 84, 92, 93, 104, 105, 113, 114, 125, 126, 134, 135, 146, 147, 155, 156, 164, 165, 202, 203, 211, 212, 223, 224, 232, 233	DQS0–DQS17, DQS0#–DQS17#	I/O	Data Strobe: Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center aligned with write data. DQS# is only used when differential data strobe mode is enabled via the LOAD MODE command. If RDQS is disabled, DQS0–DQS17 become DM0–DM8 and DQS9#–DQS17# are not used.
42, 43, 48, 49, 161, 162, 167, 168	CB0–CB7	I/O	Check Bits: ECC, 1-bit error detection and correction.
120	SCL	Input	Serial Clock for Presence-Detect: SCL is used to synchronize the presence-detect data transfer to and from the module.
101, 239, 240	SA0–SA2	Input	Presence-Detect Address Inputs: These pins are used to configure the presence-detect device.
119	SDA	Input/ Output	Serial Presence-Detect Data: SDA is a bidirectional pin used to transfer addresses and data into and out of the presence-detect portion of the module.
18	RESET#	Input	Asynchronously forces all registered outputs LOW when RESET# is LOW. This signal can be used during power up to ensure that CKE is LOW and DQs are High-Z.
53, 59, 64, 67, 69, 172, 178, 184, 187, 189, 197,	V_{DD}	Supply	Power Supply: +1.8V ±0.1V.
51, 56, 62, 72, 75, 78, 170, 175, 181, 191, 194,	V_{DDQ}	Supply	DQ Power Supply: +1.8V ±0.1V. Isolated on the device for improved noise immunity.
1	V_{REF}	Supply	SSTL_18 reference voltage.
2, 5, 8, 11, 14, 17, 20, 23, 26, 29, 32, 35, 38, 41, 44, 47, 50, 65, 66, 79, 82, 85, 88, 91, 94, 97,100, 103, 106, 109,112, 115, 118, 121, 124, 127, 130, 133, 136, 139, 142, 145, 148, 151, 154, 157, 160, 163, 166, 169, 198, 201, 204, 207, 210, 213, 216, 219, 222, 225, 228, 231, 234, 237	V_{SS}	Supply	Ground.
238	V_{DDSPD}	Supply	Serial EEPROM positive power supply: +1.7V to +3.6V.
19, 42, 43, 48, 49, 54 (512MB, 1GB), 55, 68, 102, 161, 162, 167, 168, 196 (512MB), 173, 174,	NC	—	No Connect: These pins should be left unconnected.
137, 138, 220, 221	RFU	—	Reserved for Future Use

Figure 3: Functional Block Diagram



NOTE:

1. Unless otherwise noted, resistor values are 22Ω.
2. Micron module part numbers are explained in the Module Part Numbering Guide at www.micron.com/numberguide.

MT47H32M8FP = DDR2 SDRAM used in 512MB Module
MT47H64M8FP = DDR2 SDRAM used in 1GB Module
MT47H128M8FP = DDR2 SDRAM used in 2GB Module

General Description

The MT18HTF6472D, MT18HTF12872D, and MT18HTF25672D DDR2 SDRAM modules are high-speed, CMOS, dynamic random-access 512MB, 1GB, and 2GB memory modules organized in x72 (ECC) configuration. DDR2 SDRAM modules use internally configured quad-bank (512MB, 1GB) or eight-bank (2GB) DDR2 SDRAM devices.

DDR2 SDRAM modules use double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 4*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR2 SDRAM module effectively consists of a single 4*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and four corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR2 SDRAM device during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

DDR2 SDRAM modules operate from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Read and write accesses to DDR2 SDRAM modules are burst-oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the device bank and row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the device bank and the starting column location for the burst access.

DDR2 SDRAM modules provide for programmable read or write burst lengths of four or eight locations. DDR2 SDRAM supports interrupting a burst read of eight with another read, or a burst write of eight with another write. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

The pipelined, multibank architecture of DDR2 SDRAMs allows for concurrent operation, thereby providing high, effective bandwidth by hiding row precharge and activation time.

A self refresh mode is provided, along with a power-saving power-down mode.

All inputs are compatible with the JEDEC standard for SSTL_18. All full drive-strength outputs are SSTL_18-compatible.

PLL and Register Operation

DDR2 SDRAM modules operate in registered mode, where the command/address input signals are latched in the registers on the rising clock edge and sent to the DDR2 SDRAM devices on the following rising clock edge (data access is delayed by one clock cycle). A phase-lock loop (PLL) on the module receives and redrives the differential clock signals (CK, CK#) to the DDR2 SDRAM devices. The registers and PLL minimize system and clock loading. Registered mode will add one clock cycle to CL.

Serial Presence-Detect Operation

DDR2 SDRAM modules incorporate serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard I^2C bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA (2:0), which provide eight unique DIMM/EEPROM addresses. Write protect (WP) is tied to ground on the module, permanently disabling hardware write protect.

Functional Description

DDR2 SDRAM modules use double data rate architecture to achieve high-speed operation. The DDR2 architecture is essentially a 4*n*-prefetch architecture, with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR2 SDRAM module consists of a single 4*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and four corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

Prior to normal operation, DDR2 SDRAM modules must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions, and device operation.

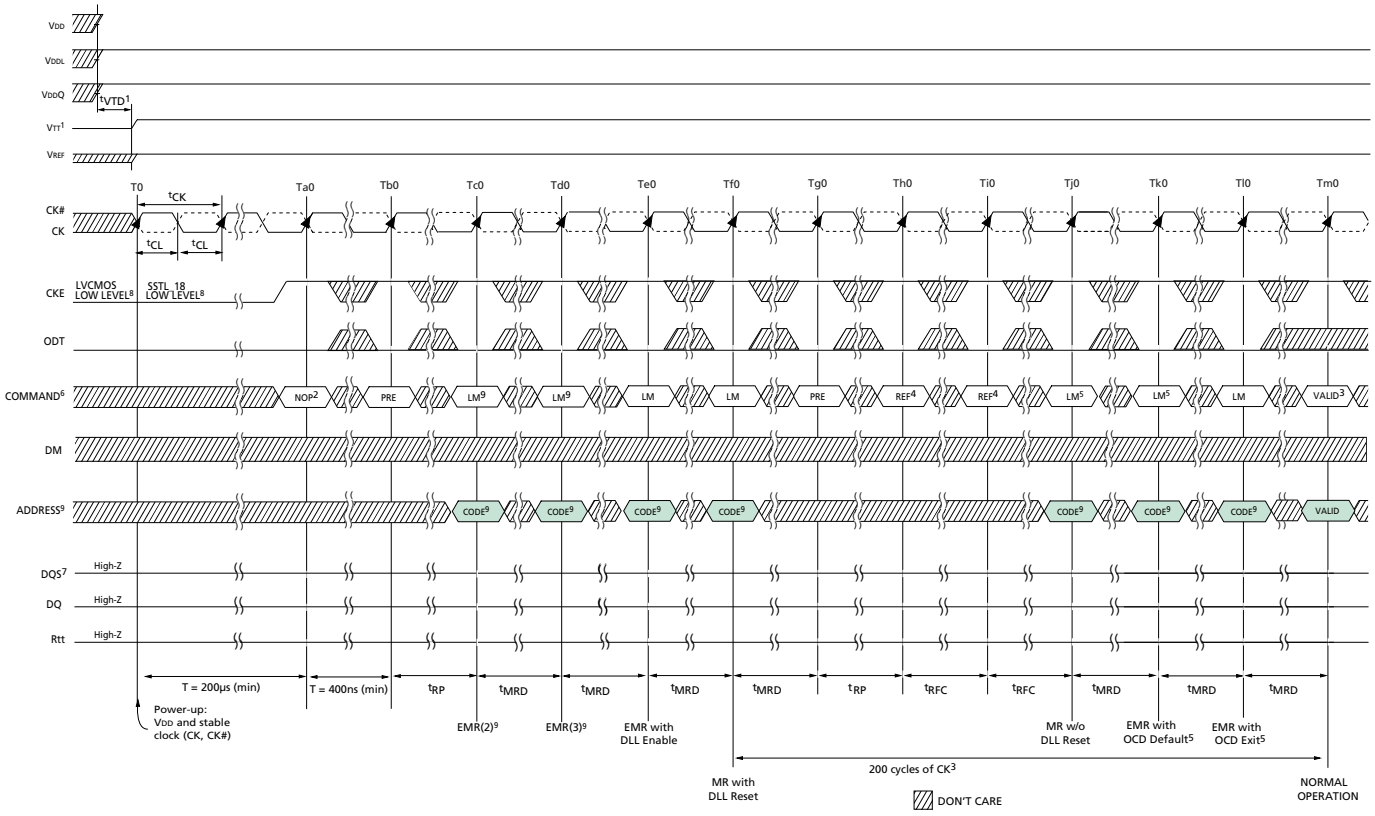
Initialization

The following sequence is required for power-up and initialization and is shown in Figure 4. The following sections provide detailed information covering device initialization, register definition, command descriptions, and device operation.

1. Apply power; if CKE is maintained below 20 percent of VDDQ, outputs remain disabled. To guarantee ODT is off, VREF must be valid and a low level must be applied to the ODT pin (all other inputs may be undefined). At least one of the following two sets of conditions (A or B) must be met:
   A. CONDITION SET A
      - VDD, VDDL and VDDQ are driven from a single power converter output
      - VTT is limited to 0.95V MAX
      - VREF tracks VDDQ/2.

   B. CONDITION SET B
      - Apply VDD before or at the same time as VDDL.
      - Apply VDDL before or at the same time as VDDQ.
      - Apply VDDQ before or at the same time as VTT and VREF.
2. For a minimum of 200µs after stable power and clock (CK, CK#), apply NOP or DESELECT commands and take CKE HIGH.
3. Wait a minimum of 400ns, then issue a PRECHARGE ALL command.
4. Issue an EMR(2) command. (To issue an EMR(2) command, provide LOW to BA0, and HIGH to BA1.)
5. Issue an EMR(3) command. (To issue an EMR(3) command, provide HIGH to BA0 and BA1.)
6. Issue an EMR to enable DLL. (To issue a DLL ENABLE command, provide LOW to BA1, A0 and provide HIGH to BA0.)
7. Issue a MODE REGISTER SET command for DLL RESET. 200 cycles of clock input is required to lock the DLL. (To issue a DLL RESET command, provide HIGH to A8 and provide LOW to BA0 and BA1.)
8. Issue PRECHARGE ALL command.
9. Issue two or more REFRESH commands.
10. Issue a MODE REGISTER SET command with LOW to A8 to initialize device operation (i.e., to program operating parameters without resetting the DLL).
11. At least 200 clocks after step 7, execute EMR OCD adjust mode if desired. If OCD adjust mode is not desired, then EMR OCD Default command is required followed by EMR OCD Exit command.

Figure 4: DDR2 Power-Up and Initialization



NOTE:

1. VTT is not applied directly to the device; however, tVTD should be greater than or equal to zero to avoid device latch-up. One of the following two conditions (a or b) MUST be met:
   a) VDD, VDDL, and VDDQ are driven from a single power converter output.
   VTT may be 0.95V maximum during power up.
   VREF tracks VDDQ/2.
   b) Apply VDD before or at the same time as VDDL.
   Apply VDDL before or at the same time as VDDQ.
   Apply VDDQ before or at the same time as VTT and VREF.
2. Either a NOP or DESELECT command may be applied.
3. 200 cycles of clock (CK, CK#) are required before a READ command can be issued.
4. Two or more REFRESH commands are required.
5. EMR OCD Default command is required unless OCD adjust mode is used by the system; either command must be followed by an EMR OCD Exit command.
6. PRE = PRECHARGE command, LM = LOAD MODE command, REF = REFRESH command, ACT = ACTIVE command, RA = Row Address, BA = Device Bank Address.
7. DQS represents DQS, DQS#, RDQS, RDQS#.
8. CKE pin uses LVCMOS input levels prior to state T0. After state T0, CKE pin uses SSTL_18 input levels.
9. The LM command for EMR(2) and EMR(3) may be before or after LM command for MR (Tf0) and EMR (Te0). ADDRESS represents A0–A12, BA0–BA1 (512MB); A0–A13, BA0–BA1 (1GB); or A0–A13, BA0–BA2 (2GB). A10 should be HIGH at states Tb0 and Tg0 to ensure a PRECHARGE (all device banks) command is issued.

Mode Register

The mode register is used to define the specific mode of operation of the DDR2 SDRAM. This definition includes the selection of a burst length, burst type, CAS latency, operating mode, DLL reset, write recovery, and power-down mode as shown in Figure 5. Contents of the mode register can be altered by re-executing the LOAD MODE (LM) command. If the user chooses to modify only a subset of the MR variables, all variables (M0–M14) must be programmed when the LOAD MODE command is issued.

The mode register is programmed via the ML command (bits M14, M13 = 0, 0) and will retain the stored information until it is programmed again or the device loses power (except for bit M8, which is self-clearing). Reprogramming the mode register will not alter the contents of the memory array, provided it is performed correctly.

The LOAD MODE command can only be issued (or reissued) when all device banks are in the precharged state. The controller must wait the specified time ^{t}MRD before initiating any subsequent operations such as an ACTIVE command. Violating either of these requirements will result in unspecified operation.

Burst Length

Burst length is defined by bits M0–M3 as shown in Figure 5. Read and write accesses to the DDR2 SDRAM are burst-oriented, with the burst length being programmable to either four or eight. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A2–A9 when the burst length is set to four and by A3–A9 when the burst length is set to eight. The remaining (least significant) address bits are used to select the starting location within the block. The programmed burst length applies to both READ and WRITE bursts.

Burst Type

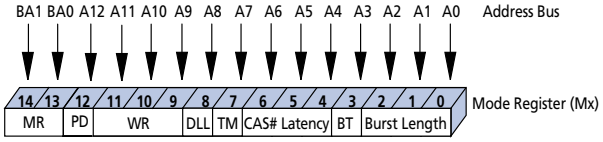
Accesses within a given burst may be programmed to be either sequential or interleaved. The burst type is selected via bit M3 as shown in Figure 5. The ordering of accesses within a burst is determined by the burst length, the burst type, and the starting column address as shown in Table 6. DDR2 SDRAM supports 4-bit burst and 8-bit burst modes only. For 8-bit burst mode, full interleave address ordering is supported; however, sequential address ordering is nibble-based.

Operating Mode

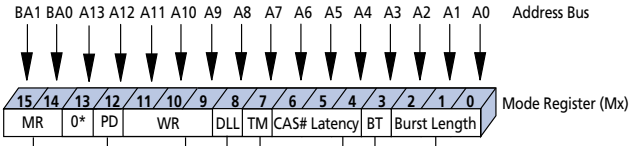
The normal operating mode is selected by issuing a LOAD MODE command with bit M7 set to zero, and all other bits set to the desired values as shown in Figure 5. When bit M7 is '1,' no other bits of the mode register are programmed. Programming bit M7 to '1' places the DDR2 SDRAM into a test mode that is only used by the Manufacturer and should NOT be used. No operation or functionality is guaranteed if M7 bit is '1.'

Figure 5: Mode Register (MR) Definition

512MB Address Bus



1GB Address Bus



M12	PD mode
0	Fast Exit (Normal)
1	Slow Exit (Low Power)

M7	Mode
0	Normal
1	Test

M8	DLL Reset
0	No
1	Yes

M2	M1	M0	Burst Length
0	0	0	Reserved
0	0	1	Reserved
0	1	0	4
0	1	1	8
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

M11	M10	M9	WRITE RECOVERY
0	0	0	Reserved
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	Reserved
1	1	1	Reserved

M3	Burst Type
0	Sequential
1	Interleaved

M6	M5	M4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	Reserved
1	1	1	Reserved

M15	M14	Mode Register Definition
0	0	Mode Register (MR)
0	1	Extended Mode Register (EMR)
1	0	Extended Mode Register (EMR2)
1	1	Extended Mode Register (EMR3)

*M13 (A13) is reserved for future use and must be programmed to '0'.

NOTE:

2GB mode registers TBD.

Table 6: Burst Definition

BURST LENGTH	STARTING COLUMN ADDRESS (A2, A1, A0)	ORDER OF ACCESSES WITHIN A BURST	
		BURST TYPE = SEQUENTIAL	BURST TYPE = INTERLEAVED
4	0 0 0	0,1,2,3	0,1,2,3
	0 0 1	1,2,3,0	1,0,3,2
	0 1 0	2,3,0,1	2,3,0,1
	0 1 1	3,0,1,2	3,2,1,0
8	0 0 0	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7
	0 0 1	1,2,3,0,5,6,7,4	1,0,3,2,5,4,7,6
	0 1 0	2,3,0,1,6,7,4,5	2,3,0,1,6,7,4,5
	0 1 1	3,0,1,2,7,4,5,6	3,2,1,0,7,6,5,4
	1 0 0	4,5,6,7,0,1,2,3	4,5,6,7,0,1,2,3
	1 0 1	5,6,7,4,1,2,3,0	5,4,7,6,1,0,3,2
	1 1 0	6,7,4,5,2,3,0,1	6,7,4,5,2,3,0,1
	1 1 1	7,4,5,6,3,0,1,2	7,6,5,4,3,2,1,0

DLL Reset

DLL reset is defined by bit M8 as shown in Figure 5. Programming bit M8 to '1' will activate the DLL RESET function. Bit M8 is self-clearing, meaning it returns back to a value of '0' after the DLL RESET function has been issued.

Anytime the DLL RESET function is used, 200 clock cycles must occur before a READ command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the ^{t}AC or ^{t}DQSCK parameters.

Write Recovery

Write recovery time is defined by bits M9–M11 as shown in Figure 5. Write recovery values of 2, 3, 4, 5, or 6 may be used for programming bits M9–M11. The user is required to program the value of write recovery, which is calculated by dividing ^{t}WR (in ns) by ^{t}CK (in ns) and rounding up a non-integer value to the next integer; WR [cycles] = ^{t}WR [ns] / ^{t}CK [ns]. Reserved states should not be used as unknown operation or incompatibility with future versions may result.

Power-Down Mode

Active power-down (PD) mode is defined by bit M12 as shown in Figure 5. PD mode allows the user to determine the active power-down mode, which determines performance vs. power savings. PD mode bit M12 does not apply to precharge power-down mode.

When bit M12 = 0, standard Active Power-down mode or 'fast-exit' active power-down mode is enabled. The ^{t}XARD parameter is used for 'fast-exit' active power-down exit timing. The DLL is expected to be enabled and running during this mode.

When bit M12 = 1, a lower power active power-down mode or 'slow-exit' active power-down mode is enabled. The ^{t}XARDS parameter is used for 'slow-exit' active power-down exit timing. The DLL can be enabled, but 'frozen' during active power-down mode since the exit-to-READ command timing is relaxed. The power difference expected between PD 'normal' and PD 'low-power' mode is defined in the IDD table.

CAS Latency (CL)

The CAS Latency (CL) is defined by bits M4–M6 as shown in Figure 5. CAS Latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first bit of output data. The CAS Latency can be set to 2, 3, 4, or 5 clocks. DDR2 SDRAM does not support any half clock latencies. Reserved states should not be used as unknown operation or incompatibility with future versions may result.

DDR2 SDRAM also supports a feature called Posted CAS additive latency (AL). This feature allows the READ command to be issued prior to ^{t}RCD(MIN) by delaying the internal command to the DDR2 SDRAM by AL clocks. The AL feature is described in more detail in the Extended Mode Register (EMR) and Operational sections.

Examples of CL = 3 and CL = 4 are shown in Figure 6; both assume AL = 0. If a READ command is registered at clock edge *n*, and the CAS Latency is *m* clocks, the data will be available nominally coincident with clock edge *n* + *m* (this assumes AL = 0).

Extended Mode Register

The extended mode register controls functions beyond those controlled by the mode register; these additional functions are DLL enable/disable, output drive strength, ODT (RTT), Posted CAS additive latency (AL), off-chip driver impedance calibration (OCD), DQS# enable/disable, RDQS/RDQS# enable/disable, and OUTPUT disable/enable. These functions are controlled via the bits shown in Figure 7. The extended mode register is programmed via the LOAD MODE (LM) command and will retain the stored information until it is programmed again or the device loses power. Reprogramming the extended mode register will not alter the contents of the memory array, provided it is performed correctly.

The extended mode register must be loaded when all device banks are idle and no bursts are in progress, and the controller must wait the specified time ^{t}MRD

before initiating any subsequent operation. Violating either of these requirements could result in unspecified operation.

DLL Enable/Disable

The DLL may be enabled or disabled by programming bit E0 during the LOAD MODE command as shown in Figure 7. The DLL must be enabled for normal operation. DLL enable is required during power-up initialization and upon returning to normal operation after having disabled the DLL for the purpose of debugging or evaluation. Enabling the DLL should always be followed by resetting the DLL using a LOAD MODE command.

The DLL is automatically disabled when entering self refresh operation and is automatically re-enabled and reset upon exit of self refresh operation.

Any time the DLL is enabled (and subsequently reset), 200 clock cycles must occur before a READ command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the ^{t}AC or ^{t}DQSCK parameters.

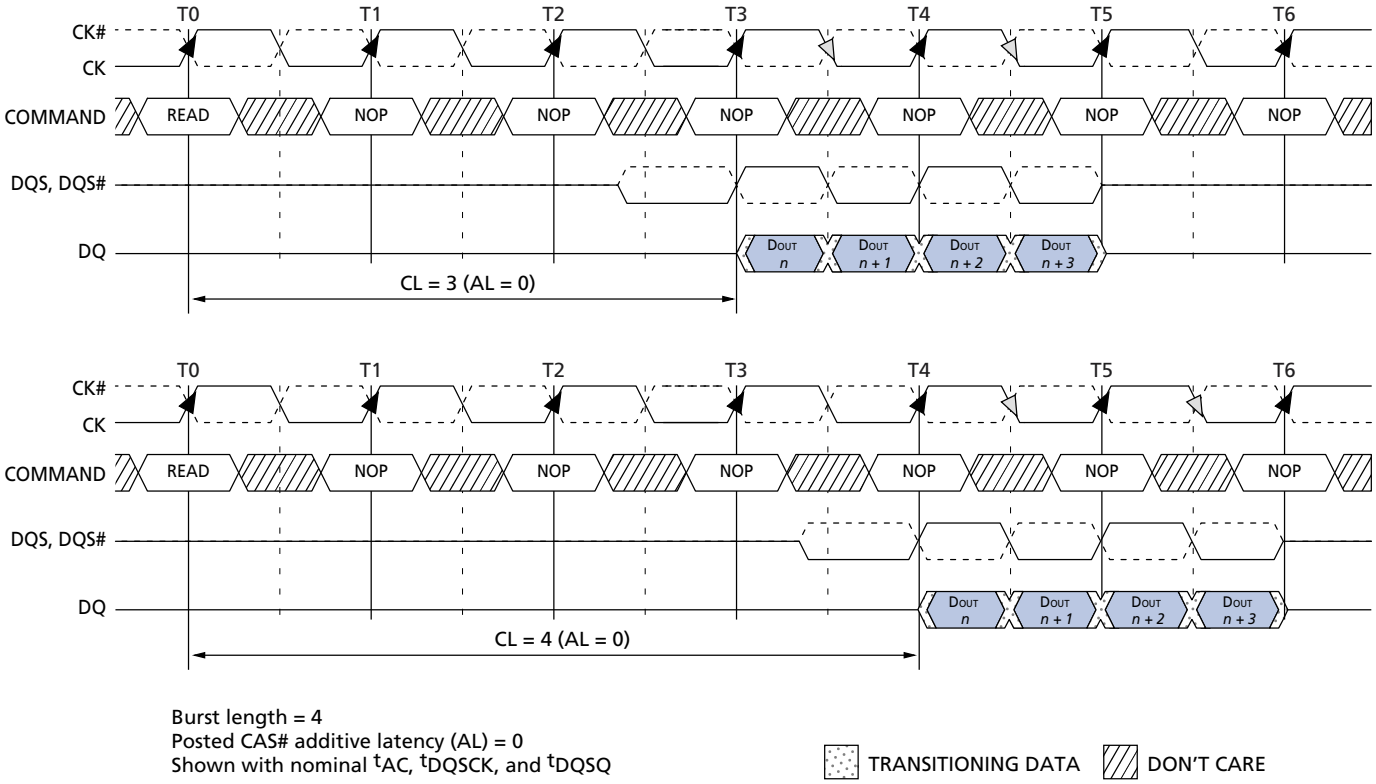
Output Drive Strength

The output drive strength is defined by bit E1 as shown in Figure 7. The normal drive strength for all outputs are specified to be SSTL_18. Programming bit E1 = 0 selects normal (100 percent) drive strength for all outputs. Selecting a reduced drive strength option (bit E1 = 1) will reduce all outputs to approximately 60 percent of the SSTL_18 drive strength. This option is intended for the support of the lighter load and/or point-to-point environments.

DQS# Enable/Disable

The DQS# enable function is defined by bit E10. When enabled (bit E10 = 0), DQS# is the complement of the differential data strobe pair DQS/DQS#. When disabled (bit E10 = 1), DQS is used in a single-ended mode and the DQS# pin is disabled. This function is also used to enable/disable RDQS#. If RDQS is enabled (E11 = 1) and DQS# is enabled (E10 = 0), then both DQS# and RDQS# will be enabled.

Figure 6: CAS Latency (CL)

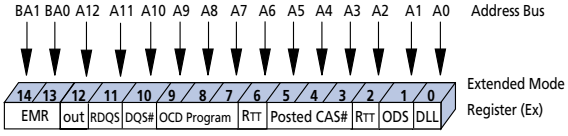


RDQS Enable/Disable

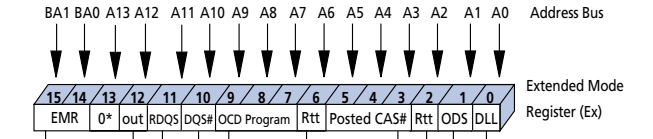
The RDQS enable function is defined by bit E11 as shown in Figure 7, Extended Mode Register Definition. When enabled (E11 = 1), RDQS is identical in function and timing to data strobe DQS during a READ. During a WRITE operation, RDQS is ignored by the DDR2 SDRAM. If RDQS is disabled, RDQS pins are used for data mask.

Figure 7: Extended Mode Register Definition

512MB Address Bus



1GB Address Bus



E12	Outputs
0	Enabled
1	Disabled

E11	RDQS Enable
0	No
1	Yes

E10	DQS# Enable
0	Enable
1	Disable

E9	E8	E7	OCD Operation
0	0	0	OCD calibration mode exit
0	0	1	Drive(1) pull-up
0	1	0	Drive(0) pull-down
1	0	0	OCD Enter Adjust mode
1	1	1	OCD calibration default

E6	E2	Rtt (nominal)
0	0	Rtt Disabled
0	1	75 ohm
1	0	150 ohm
1	1	Reserved

E5	E4	E3	Posted CAS# Additive Latency (AL)
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

E1	Output Drive Strength
0	100%
1	60%

E0	DLL Enable
0	Enable (Normal)
1	Disable (Test/Debug)

E15	E14	Mode Register Definition
0	0	Mode Register (MR)
0	1	Extended Mode Register (EMR)
1	0	Extended Mode Register (EMR2)
1	1	Extended Mode Register (EMR3)

* E13 (A13) is reserved for future use and must be programmed to '0'.

NOTE:

2GB extended mode register TBD.

Output Enable/Disable

The OUTPUT enable function is defined by bit E12 as shown in Figure 7. When enabled (E12 = 0), all outputs (DQs, DQS, DQS#, RDQS/RDQS#) function normally. When disabled (E12 = 1), all DDR2 SDRAM outputs (DQs, DQS, DQS#) are disabled removing output buffer current. The OUTPUT disable feature is intended to be used during IDD characterization of read current.

On Die Termination (ODT)

ODT effective resistance RTT (EFF) is defined by bits E2 and E6 of the EMR as shown in Figure 7. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DDR2 SDRAM controller to independently turn on/off ODT for any or all devices. RTT effective resistance values of 75Ω and 150Ω are selectable and apply to each DQ, DQS/DQS#, RDQS/RDQS# and DM signals.

Bits (E6, E2) determine what ODT resistance is enabled by turning on/off 'sw1' or 'sw2'. The ODT effective resistance value is selected by enabling switch 'sw1,' which enables all 'R1' values that are 150Ω each, enabling an effective resistance of 75Ω (RTT (EFF1) = 'R1' / 2). Similarly, if 'sw2' is enabled, all 'R2' values that are 300Ω each, enable an effective ODT resistance of 150Ω (RTT (EFF2) = 'R2'/2). Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

The ODT control pin is used to determine when RTT(EFF) is turned on and off, assuming ODT has been enabled via bits E2 and E6 of the EMR. The ODT feature and ODT input pin are only used during active, active power-down (both fast-exit and slow-exit modes), and precharge power-down modes of operation. If SELF REFRESH operation is used, RTT (EFF) should *always* be disabled and the ODT input pin is disabled by the DDR2 SDRAM. During power-up and initialization of the DDR2 SDRAM, ODT should be disabled until the EMR command is issued to enable the ODT feature, at which point the ODT pin will determine the RTT (EFF) value.

Off-Chip Driver (OCD) Impedance Calibration

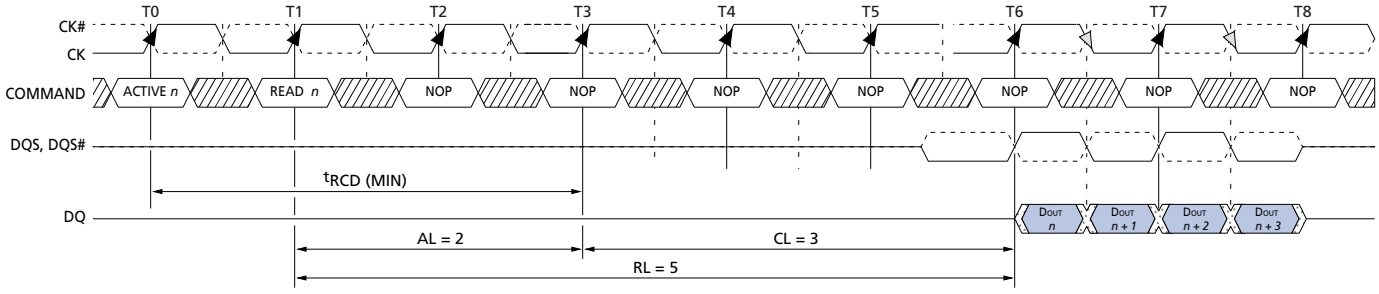
The DDR2 SDRAM output off-chip (OCD) driver impedance calibration operation is defined by bits E7–E9. OCD is intended to allow the system to calibrate and match pull-up to pull-down impedance to 18Ω nominal. OCD is not intended to allow a wide range of impedance calibration outside of the 18Ω nominal driver impedance.

Posted CAS Additive Latency (AL)

Posted CAS additive latency (AL) is supported to make the command and data bus efficient for sustainable bandwidths in DDR2 SDRAM. Bits E3–E5 define the value of AL as shown in Figure 7. Bits E3–E5 allow the user to program the DDR2 SDRAM with a CAS# Additive latency of 0, 1, 2, 3, or 4 clocks. Reserved states should not be used as unknown operation or incompatibility with future versions may result.

In this operation, the DDR2 SDRAM allows a READ or WRITE command to be issued prior to ^{t}RCD (MIN) with the requirement that AL ≤ ^{t}RCD(MIN). A typical application using this feature would set AL = ^{t}RCD (MIN) - 1 x ^{t}CK. The READ or WRITE command is held for the time of the additive latency (AL) before it is issued internally to the DDR2 SDRAM device. READ Latency (RL) is controlled by the sum of the Posted CAS additive latency (AL) and CAS Latency (CL); RL = AL + CL. Write latency (WL) is equal to READ latency minus one clock; WL = AL + CL - 1 x ^{t}CK. An example of a READ latency is shown in Figure 8. An example of a WRITE latency is shown in Figure 9.

Figure 8: READ Latency

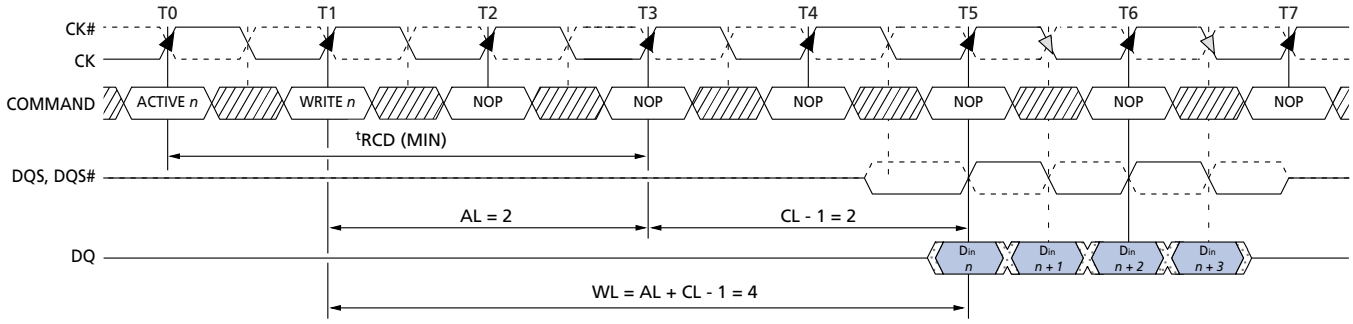


Burst length = 4
Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ

CAS# latency (CL) = 3
Additive latency (AL) = 2
READ latency (RL) = AL + CL = 5

TRANSITIONING DATA DON'T CARE

Figure 9: Write Latency



Burst length = 4

CAS# latency (CL) = 3
Additive latency (AL) = 2
WRITE latency = AL + CL -1 = 4

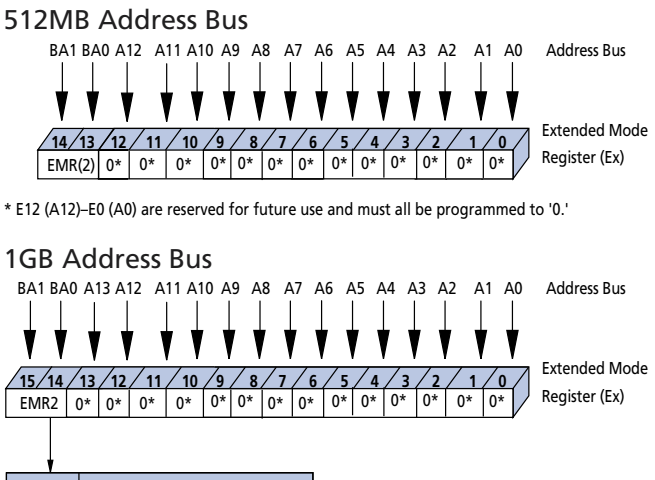
TRANSITIONING DATA DON'T CARE

Extended Mode Register 2 (EMR2)

The Extended Mode Register 2 (EMR2) controls functions beyond those controlled by the mode register. Currently all bits in EMR2 are reserved as shown in Figure 10. The EMR2 is programmed via the LOAD MODE command and will retain the stored information until it is programmed again or the device loses power. Reprogramming the extended mode register will not alter the contents of the memory array, provided it is performed correctly.

The extended mode register must be loaded when all device banks are idle and no bursts are in progress, and the controller must wait the specified time ^{t}MRD before initiating any subsequent operation. Violating either of these requirements could result in unspecified operation.

Figure 10: Extended Mode Register 2 (EMR2) Definition



* E12 (A12)–E0 (A0) are reserved for future use and must all be programmed to '0.'

M15	M14	Mode Register Definition
0	0	Mode Register (MR)
0	1	Extended Mode Register (EMR)
1	0	Extended Mode Register (EMR2)
1	1	Extended Mode Register (EMR3)

* E13 (A13) - E0 (A0) are reserved for future use and must all be programmed to '0'.

NOTE:

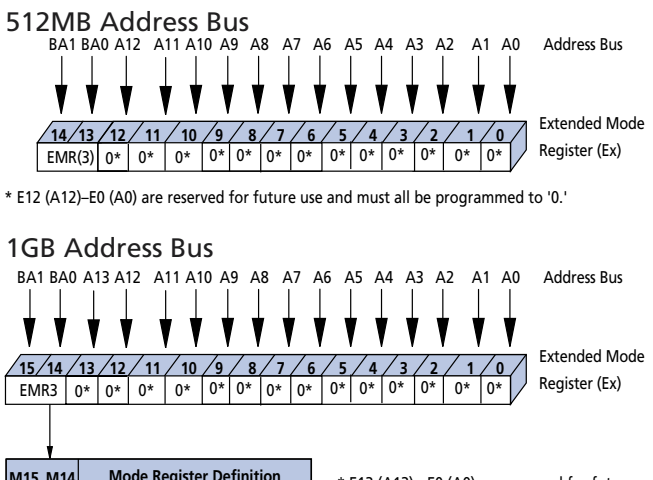
2GB extended mode register TBD.

Extended Mode Register Set 3 (EMR3)

The Extended Mode Register 3 (EMR3) controls functions beyond those controlled by the mode register. Currently all bits in EMR3 are reserved as shown in Figure 11. The EMR3 is programmed via the LOAD MODE command and will retain the stored information until it is programmed again or the device loses power. Reprogramming the extended mode register will not alter the contents of the memory array, provided it is performed correctly.

The extended mode register must be loaded when all device banks are idle and no bursts are in progress, and the controller must wait the specified time ^{t}MRD before initiating any subsequent operation. Violating either of these requirements could result in unspecified operation.

Figure 11: Extended Mode Register 3 (EMR3) Definition



* E12 (A12)–E0 (A0) are reserved for future use and must all be programmed to '0.'

M15	M14	Mode Register Definition
0	0	Mode Register (MR)
0	1	Extended Mode Register (EMR)
1	0	Extended Mode Register (EMR2)
1	1	Extended Mode Register (EMR3)

* E13 (A13) - E0 (A0) are reserved for future use and must all be programmed to '0'.

NOTE:

2GB extended mode register TBD.

Command Truth Tables

Table 7, Commands Truth Table provides a quick reference of DDR2 SDRAM available commands. Refer to the 256Mb, 512Mb, or 1Gb DDR2 SDRAM component data sheet for more Truth Table definitions, including CKE power-down modes and device bank-to-bank commands.

Table 7: Commands Truth Table

Notes: 1, 5

FUNCTION	CKE		CS#	RAS#	CAS#	WE#	BA2, BA1, BA0[8]	A13–A11[8]	A10	A9–A0	NOTES
	PREVIOUS CYCLE	CURRENT CYCLE									
Mode Register Set	H	H	L	L	L	L	BA	OP Code			2
Refresh	H	H	L	L	L	H	X	X	X	X	6
Self Refresh Entry	H	L	L	L	L	H	X	X	X	X	
Self Refresh Exit	L	H	X	X	X	X	X	X	X	X	6, 7
			L	H	H	H	X	X	X	X	
Single Device Bank Precharge	H	H	L	L	H	L	BA	X	L	X	2, 6
ALL Device Banks Precharge	H	H	L	L	H	L	X	X	H	X	6
Device Bank Activate	H	H	L	L	H	H	BA	Row Address			6
Write	H	H	L	H	L	L	BA	Column Address	L	Column Address	2, 3
Write with Auto Precharge	H	H	L	H	L	L	BA	Column Address	H	Column Address	2, 3
Read	H	H	L	H	L	H	BA	Column Address	L	Column Address	2, 3
Read with Auto Precharge	H	H	L	H	L	H	BA	Column Address	H	Column Address	2, 3
No Operation	H	X	L	H	H	H	X	X	X	X	6
Device Deselect	H	X	H	X	X	X	X	X	X	X	6
Power-Down Entry	H	L	H	X	X	X	X	X	X	X	4, 6
			L	H	H	H	X	X	X	X	
Power-Down Exit	L	H	H	X	X	X	X	X	X	X	4, 6
			L	H	H	H	X	X	X	X	

NOTE:

1. All DDR2 SDRAM commands are defined by states of CS#, RAS#, CAS#, WE#, and CKE at the rising edge of the clock.
2. Device Bank addresses (BA) determine which device bank is to be operated upon. For EMR, BA selects an extended mode register.
3. Burst reads or writes at BL = 4 cannot be terminated or interrupted. See sections "Read Interrupted by a Read" and "Write Interrupted by a Write" for other restrictions and details.
4. The Power Down Mode does not perform any refresh operations. The duration of power-down is therefore limited by the refresh requirements outlined in the AC parametric section.
5. The state of ODT does not affect the states described in this table. The ODT function is not available during self refresh. See the ODT section for details.
6. "X" means "H or L" (but a defined logic level).
7. Self refresh exit is asynchronous.
8. BA2 valid for 2GB only; A13 valid for 1GB and 2GB only.

Absolute Maximum Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 8: Absolute Maximum DC Ratings

SYMBOL	PARAMETER		MIN	MAX	UNITS
VDD	VDD Supply Voltage Relative to VSS		-1.0	2.3	V
VDDQ	VDDQ Supply Voltage Relative to VSS		-0.5	2.3	V
VDDL	VDDL Supply Voltage Relative to VSS		-0.5	2.3	V
VIN, VOUT	Voltage on any Pin Relative to VSS		-0.5	2.3	V
TSTG	Storage Temperature		-55	100	°C
T_{OPR}	Operating Temperature (T_{OPR})		0	55	°C
I_I	Input Leakage Current; Any input 0V ≤ VIN ≤ VDD; VREF input 0V ≤ VIN ≤0.95V; (All other pins not under test = 0V)	Command/Address, RAS#, CAS#, WE#, S#, CKE, ODT	-5	5	µA
		CK, CK#	-10	10	
		DM	-10	10	
I_{OZ}	Output Leakage Current; 0V ≤ VOUT ≤ VDDQ; DQs and ODT are disabled	DQ, DQS	-10	10	µA

Table 9: Recommended DC Operating Conditions

All voltages referenced to VSS

PARAMETER	SYMBOL	MIN	NOM	MAX	UNITS	NOTES
Supply Voltage	VDD	1.7	1.8	1.9	V	1
VDDL Supply Voltage	VDDL	1.7	1.8	1.9	V	4
I/O Supply Voltage	VDDQ	1.7	1.8	1.9	V	4
I/O Reference Voltage	VREF	0.49 x VDDQ	0.50 x VDDQ	0.51 x VDDQ	V	2
I/O Termination Voltage (system)	VTT	VREF - 40	VREF	VREF + 40	mV	3

NOTE:

1. VDD and VDDQ must track each other. VDDQ must be less than or equal to VDD.
2. VREF is expected to equal VDDQ/2 of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise (non-common mode) on VREF may not exceed ±1percent of the DC value. Peak-to-peak AC noise on VREF may not exceed ±2 percent of VREF (DC). This measurement is to be taken at the nearest VREF bypass capacitor.
3. VTT is not applied directly to the device. VTT is a system supply for signal termination resistors, is expected to be set equal to VREF and must track variations in the DC level of VREF.
4. VDDQ tracks with VDD; VDDL tracks with VDD.

Input Electrical Characteristics and Operating Conditions

Table 10: Input DC Logic Levels

All voltages referenced to VSS

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage	VIH(DC)	VREF + 125	VDDQ + 300	mV	
Input Low (Logic 0) Voltage	VIL(DC)	-300	VREF - 125	mV	

Table 11: Input AC Logic Levels

All voltages referenced to VSS

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage	VIH(AC)	VREF + 250	-	mV	
Input Low (Logic 0) Voltage	VIL(AC)	–	VREF - 250	mV	

IDD Specifications and Conditions

IDD specifications are tested after the device is properly initialized. 0°C ≤ T_{OPR} ≤ +55°C. VDD = +1.8V ±0.1V, VDDQ = +1.8V ±0.1V, VDDL= +1.8V ±0.1V, VREF=VDDQ/2.

Input slew rate is specified by AC Parametric Test Conditions. IDD parameters are specified with ODT disabled. Data bus consists of DQ, DM, DQS, DQS#. IDD values must be met with all combinations of EMR bits 10 and 11.

Definitions for IDD Conditions:

- LOW is defined as VIN ≤ VIL (AC) (MAX)
- HIGH is defined as VIN ≥ VIH (AC) (MIN)
- STABLE is defined as inputs stable at a HIGH or LOW level
- FLOATING is defined as inputs at VREF = VDDQ/2
- SWITCHING is defined as inputs changing between HIGH and LOW every other clock cycle (once per two clocks) for address and control signals
- Switching is defined as inputs changing between HIGH and LOW every other data transfer (once per clock) for DQ signals not including masks or strobes

Table 12: General IDD Parameters

IDD PARAMETER		-53E	-40E	UNITS
CL (IDD)		4	3	^{t}CK
^{t}RCD (IDD)		15	15	ns
^{t}RC (IDD)		60	60	ns
^{t}RRD (IDD)		7.5	7.5	ns
^{t}CK (IDD)		3.75	5	ns
^{t}RAS MIN (IDD)		45	45	ns
^{t}RAS MAX (IDD)		70,000	70,000	ns
^{t}RP (IDD)		15	15	ns
^{t}RFC (IDD)	512MB	75	75	ns
	1GB	105	105	ns
	2GB	127.5	127.5	ns

IDD7 Conditions

Table 13, IDD7: Operating Current, specifies detailed timing requirements for IDD7. Changes will be required if timing parameter changes are made to the specification.

Table 13: IDD7: Operating Current

All Bank Interleave Read operation; legend: A = active; RA = read auto precharge; D = deselect

SPEED GRADE	IDD7 TIMING PATTERNS
-53E	A0 RA0 D A1 RA1 D A2 RA2 D A3 RA3 D D D D D
-40E	A0 RA0 A1 RA1 A2 RA2 A3 RA3 D D D D

NOTE:

All device banks are being interleaved at minimum ^{t}RC (IDD) without violating ^{t}RRD (IDD) using a burst length of 4. Control and address bus inputs are STABLE during DESELECTs. IOUT = 0mA.

Table 14: DDR2 IDD Specifications and Conditions – 512MB

Notes: 1–5; notes appear on page 25. Values shown for DDR2 SDRAM components only.

PARAMETER/CONDITION		SYMBOL	-53E	-40E	UNITS
Operating one device bank active-precharge current; $^{t}CK = {}^{t}CK$ (IDD), $^{t}RC = {}^{t}RC$ (IDD), $^{t}RAS = {}^{t}RAS$ MIN (IDD); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING.		IDD0[a]	765	707	mA
Operating one device bank active-read-precharge current; IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; $^{t}CK = {}^{t}CK$ (IDD), $^{t}RC = {}^{t}RC$ (IDD), $^{t}RAS = {}^{t}RAS$ MIN (IDD), $^{t}RCD = {}^{t}RCD$ (IDD); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W.		IDD1[a]	855	797	mA
Precharge power-down current; All device banks idle; $^{t}CK = {}^{t}CK$ (IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.		IDD2P[b]	90	63	mA
Precharge quiet standby current; All device banks idle; $^{t}CK = {}^{t}CK$ (IDD); CKE is HIGH, CS# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.		IDD2Q[b]	450	378	mA
Precharge standby current; All device banks idle; $^{t}CK = {}^{t}CK$ (IDD); CKE is HIGH, CS# is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.		IDD2N[b]	540	450	mA
Active power-down current; All device banks open; $^{t}CK = {}^{t}CK$ (IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.	Fast PDN Exit MR[12] = 0	IDD3P[b]	342	270	mA
	Slow PDN Exit MR[12] = 1		162	126	mA
Active standby current; All device banks open; $^{t}CK = {}^{t}CK$(IDD), $^{t}RAS = {}^{t}RAS$ MAX (IDD), $^{t}RP = {}^{t}RP$(IDD); CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.		IDD3N[b]	702	576	mA
Operating burst write current; All device banks open, Continuous burst writes; BL = 4, CL = CL (IDD), AL = 0; $^{t}CK = {}^{t}CK$ (IDD), $^{t}RAS = {}^{t}RAS$ MAX (IDD), $^{t}RP = {}^{t}RP$ (IDD); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING.		IDD4W[a]	1,485	1,157	mA
Operating burst read current; All device banks open, Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL (IDD), AL = 0; $^{t}CK = {}^{t}CK$ (IDD), $^{t}RAS = {}^{t}RAS$ MAX (IDD), $^{t}RP = {}^{t}RP$ (IDD); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING.		IDD4R[a]	1,305	1,022	mA
Burst refresh current; $^{t}CK = {}^{t}CK$ (IDD); Refresh command at every ^{t}RFC (IDD) interval; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.		IDD5[b]	3,060	2,970	mA
Self refresh current; CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING.		IDD6[b]	54	54	mA
Operating device bank interleave read current; All device banks interleaving reads, IOUT= 0mA; BL = 4, CL = CL (IDD), AL = ^{t}RCD (IDD)-1 x ^{t}CK (IDD); $^{t}CK = {}^{t}CK$ (IDD), $^{t}RC = {}^{t}RC$(IDD), $^{t}RRD = {}^{t}RRD$(IDD), $^{t}RCD = {}^{t}RCD$(IDD); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data bus inputs are SWITCHING; See IDD7 Conditions for detail.		IDD7[a]	2,205	2,102	mA

NOTE:

a - Value calculated as one module rank in this operating condition, and all other module ranks in IDD2P (CKE LOW) mode.
b - Value calculated reflects all module ranks in this operating condition.

Table 15: DDR2 IDD Specifications and Conditions – 1GB

Notes: 1–5; notes appear on page 25. Values shown for DDR2 SDRAM components only.

PARAMETER/CONDITION		SYMBOL	-53E	-40E	UNITS
Operating one device bank active-precharge current; $^{t}CK = {}^{t}CK$ (IDD), $^{t}RC = {}^{t}RC$ (IDD), $^{t}RAS = {}^{t}RAS$ MIN (IDD); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING.		I_{DD0}[a]	TBD	TBD	mA
Operating one device bank active-read-precharge current; IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; $^{t}CK = {}^{t}CK$ (IDD), $^{t}RC = {}^{t}RC$ (IDD), $^{t}RAS = {}^{t}RAS$ MIN (IDD), $^{t}RCD = {}^{t}RCD$ (IDD); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W.		I_{DD1}[a]	TBD	TBD	mA
Precharge power-down current; All device banks idle; $^{t}CK = {}^{t}CK$ (IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.		I_{DD2P}[b]	TBD	TBD	mA
Precharge quiet standby current; All device banks idle; $^{t}CK = {}^{t}CK$ (IDD); CKE is HIGH, CS# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.		I_{DD2Q}[b]	TBD	TBD	mA
Precharge standby current; All device banks idle; $^{t}CK = {}^{t}CK$ (IDD); CKE is HIGH, CS# is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.		I_{DD2N}[b]	TBD	TBD	mA
Active power-down current; All device banks open; $^{t}CK = {}^{t}CK$ (IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.	Fast PDN Exit MR[12] = 0	I_{DD3P}[b]	TBD	TBD	mA
	Slow PDN Exit MR[12] = 1		TBD	TBD	mA
Active standby current; All device banks open; $^{t}CK = {}^{t}CK$(IDD), $^{t}RAS = {}^{t}RAS$ MAX (IDD), $^{t}RP = {}^{t}RP$(IDD); CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.		I_{DD3N}[b]	TBD	TBD	mA
Operating burst write current; All device banks open, Continuous burst writes; BL = 4, CL = CL (IDD), AL = 0; $^{t}CK = {}^{t}CK$ (IDD), $^{t}RAS = {}^{t}RAS$ MAX (IDD), $^{t}RP = {}^{t}RP$ (IDD); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING.		I_{DD4W}[a]	TBD	TBD	mA
Operating burst read current; All device banks open, Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL (IDD), AL = 0; $^{t}CK = {}^{t}CK$ (IDD), $^{t}RAS = {}^{t}RAS$ MAX (IDD), $^{t}RP = {}^{t}RP$ (IDD); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING.		I_{DD4R}[a]	TBD	TBD	mA
Burst refresh current; $^{t}CK = {}^{t}CK$ (IDD); Refresh command at every ^{t}RFC (IDD) interval; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.		I_{DD5}[b]	TBD	TBD	mA
Self refresh current; CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING.		I_{DD6}[b]	TBD	TBD	mA
Operating device bank interleave read current; All device banks interleaving reads, IOUT= 0mA; BL = 4, CL = CL (IDD), AL = ^{t}RCD (IDD)-1 x ^{t}CK (IDD); $^{t}CK = {}^{t}CK$ (IDD), $^{t}RC = {}^{t}RC$(IDD), $^{t}RRD = {}^{t}RRD$(IDD), $^{t}RCD = {}^{t}RCD$(IDD); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data bus inputs are SWITCHING; See IDD7 Conditions for detail.		I_{DD7}[a]	TBD	TBD	mA

NOTE:

a - Value calculated as one module rank in this operating condition, and all other module ranks in IDD2P (CKE LOW) mode.
b - Value calculated reflects all module ranks in this operating condition.

Table 16: DDR2 IDD Specifications and Conditions – 2GB

Notes: 1–5; notes appear on page 25; values shown for DDR2 SDRAM components only

PARAMETER/CONDITION		SYMBOL	-53E	-40E	UNITS
Operating one device bank active-precharge current; $^{t}CK = {}^{t}CK$ (IDD), $^{t}RC = {}^{t}RC$ (IDD), $^{t}RAS = {}^{t}RAS$ MIN (IDD); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING.		I_{DD0}[a]	TBD	TBD	mA
Operating one device bank active-read-precharge current; IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; $^{t}CK = {}^{t}CK$ (IDD), $^{t}RC = {}^{t}RC$ (IDD), $^{t}RAS = {}^{t}RAS$ MIN (IDD), $^{t}RCD = {}^{t}RCD$ (IDD); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W.		I_{DD1}[a]	TBD	TBD	mA
Precharge power-down current; All device banks idle; $^{t}CK = {}^{t}CK$ (IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.		I_{DD2P}[b]	TBD	TBD	mA
Precharge quiet standby current; All device banks idle; $^{t}CK = {}^{t}CK$ (IDD); CKE is HIGH, CS# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.		I_{DD2Q}[b]	TBD	TBD	mA
Precharge standby current; All device banks idle; $^{t}CK = {}^{t}CK$ (IDD); CKE is HIGH, CS# is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.		I_{DD2N}[b]	TBD	TBD	mA
Active power-down current; All device banks open; $^{t}CK = {}^{t}CK$ (IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.	Fast PDN Exit MR[12] = 0	I_{DD3P}[b]	TBD	TBD	mA
	Slow PDN Exit MR[12] = 1		TBD	TBD	mA
Active standby current; All device banks open; $^{t}CK = {}^{t}CK$(IDD), $^{t}RAS = {}^{t}RAS$ MAX (IDD), $^{t}RP = {}^{t}RP$(IDD); CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.		I_{DD3N}[b]	TBD	TBD	mA
Operating burst write current; All device banks open, Continuous burst writes; BL = 4, CL = CL (IDD), AL = 0; $^{t}CK = {}^{t}CK$ (IDD), $^{t}RAS = {}^{t}RAS$ MAX (IDD), $^{t}RP = {}^{t}RP$ (IDD); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING.		I_{DD4W}[a]	TBD	TBD	mA
Operating burst read current; All device banks open, Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL (IDD), AL = 0; $^{t}CK = {}^{t}CK$ (IDD), $^{t}RAS = {}^{t}RAS$ MAX (IDD), $^{t}RP = {}^{t}RP$ (IDD); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING.		I_{DD4R}[a]	TBD	TBD	mA
Burst refresh current; $^{t}CK = {}^{t}CK$ (IDD); Refresh command at every ^{t}RFC (IDD) interval; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.		I_{DD5}[b]	TBD	TBD	mA
Self refresh current; CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING.		I_{DD6}[b]	TBD	TBD	mA
Operating device bank interleave read current; All device banks interleaving reads, IOUT= 0mA; BL = 4, CL = CL (IDD), AL = ^{t}RCD (IDD)-1 x ^{t}CK (IDD); $^{t}CK = {}^{t}CK$ (IDD), $^{t}RC = {}^{t}RC$(IDD), $^{t}RRD = {}^{t}RRD$(IDD), $^{t}RCD = {}^{t}RCD$(IDD); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data bus inputs are SWITCHING; See IDD7 Conditions for detail.		I_{DD7}[a]	TBD	TBD	mA

NOTE:

a - Value calculated as one module rank in this operating condition, and all other module ranks in IDD2P (CKE LOW) mode.
b - Value calculated reflects all module ranks in this operating condition.

Table 17: Capacitance

Parameters are sampled; V_{DD} = +1.8V ±0.1V, V_{DDQ} = +1.8V ±0.1V, V_{REF} = V_{SS}, f = 100 MHz, 0°C ≤ T_{OPR} ≤ +55°C, V_{OUT} (DC) = V_{DDQ}/2, V_{OUT} (peak to peak) = 0.1V; DM input is grouped with I/O pins, reflecting the fact that they are matched in loading

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Capacitance: CK, CK#	C_{I1}	2.0	3.0	pF
Input Capacitance: BA0–BA2, A0–A13, RAS#, CAS#, WE#, S#, CKE, ODT	C_{I2}	2.5	3.5	pF
Input/Output Capacitance: DQ, DQS, DM	C_{IO}	5.0	8.0	pF

Table 18: AC Operating Conditions

Notes: 1–5; notes appear on page 25; 0°C ≤ T_{OPR} ≤ +55°C; V_{DDQ} = +1.8V ±0.1V, V_{DD} = +1.8V ±0.1V

AC CHARACTERISTICS				-53E		-40E			
PARAMETER			SYMBOL	MIN	MAX	MIN	MAX	UNITS	NOTES
Clock	Clock cycle time	CL = 4	^tCK (4)	3,750	8,000	5,000	8,000	ps	16, 25
		CL = 3	^tCK (3)	5,000	8,000	–	–	ps	16, 25
	CK high-level width		^tCH	0.45	0.55	0.45	0.55	^tCK	19
	CK low-level width		^tCL	0.45	0.55	0.45	0.55	^tCK	19
	Half clock period		^tHP	MIN (^tCH, ^tCL)		MIN (^tCH, ^tCL)		ps	20
	Clock jitter		^tJIT	TBD	TBD	TBD	TBD	ps	18
Data	DQ output access time from CK/CK#		^tAC	-500	+500	-600	+600	ps	
	Data-out high-impedance window from CK/CK#		^tHZ		^tAC MAX		^tAC MAX	ps	8, 9
	Data-out low-impedance window from CK/CK#		^tLZ	^tAC MIN	^tAC MAX	^tAC MIN	^tAC MAX	ps	8, 10
	DQ and DM input setup time relative to DQS		^tDS	100		150		ps	7, 15, 22
	DQ and DM input hold time relative to DQS		^tDH	225		275		ps	7, 15, 22
	DQ and DM input pulse width (for each input)		^tDIPW	0.35		0.35		^tCK	
	Data hold skew factor		^tQHS		400		450	ps	
	DQ–DQS hold, DQS to first DQ to go nonvalid, per access		^tQH	^tHP -^tQHS		^tHP -^tQHS		ps	15, 17
	Data valid output window (DVW)		^tDVW	^tQH - ^tDQSQ		^tQH - ^tDQSQ		ns	15, 17

Table 18: AC Operating Conditions (Continued)

Notes: 1–5; notes appear on page 25; 0°C ≤ T_{OPR} ≤ +55°C; VDDQ = +1.8V ±0.1V, VDD = +1.8V ±0.1V

AC CHARACTERISTICS				-53E		-40E			
	PARAMETER		SYMBOL	MIN	MAX	MIN	MAX	UNITS	NOTES
Data Strobe	DQS input high pulse width		^{t}DQSH	0.35		0.35		^{t}CK	
	DQS input low pulse width		^{t}DQSL	0.35		0.35		^{t}CK	
	DQS output access time from CK/CK#		^{t}DQSCK	-450	+450	-500	+500	ps	
	DQS falling edge to CK rising – setup time		^{t}DSS	0.2		0.2		^{t}CK	
	DQS falling edge from CK rising – hold time		^{t}DSH	0.2		0.2		^{t}CK	
	DQS–DQ skew, DQS to last DQ valid, per group, per access		^{t}DQSQ		300		350	ps	15, 17
	DQS read preamble		^{t}RPRE	0.9	1.1	0.9	1.1	^{t}CK	23
	DQS read postamble		^{t}RPST	0.4	0.6	0.4	0.6	^{t}CK	
	DQS write preamble setup time		^{t}WPRES	0		0		ps	12, 13
	DQS write preamble		^{t}WPRE	0.25		0.25		^{t}CK	
	DQS write postamble		^{t}WPST	0.4	0.6	0.4	0.6	^{t}CK	11
	Write command to first DQS latching transition		^{t}DQSS	WL - 0.25	WL + 0.25	WL - 0.25	WL + 0.25	^{t}CK	
Command and Address	Address and control input pulse width for each input		^{t}IPW	0.6		0.6		^{t}CK	
	Address and control input setup time		^{t}IS	250		350		ps	6, 22
	Address and control input hold time		^{t}IH	375		475		ps	6, 22
	CAS# to CAS# command delay		^{t}CCD	2		2		^{t}CK	
	ACTIVE to ACTIVE (same bank) command		^{t}RC	60		65		ns	
	ACTIVE bank *a* to ACTIVE bank *b* command		^{t}RRD	7.5		7.5		ns	28
	ACTIVE to READ or WRITE delay		^{t}RCD	15		20		ns	
	ACTIVE to PRECHARGE command		^{t}RAS	45	70,000	45	70,000	ns	21
	Internal READ to precharge command delay		^{t}RTP	7.5		7.5		ns	24, 28
	Write recovery time		^{t}WR	15		15		ns	28
	Auto precharge write recovery + precharge time		^{t}DAL	^{t}WR + ^{t}RP		^{t}WR + ^{t}RP		ns	23
	Internal WRITE to READ command delay		^{t}WTR	7.5		10		ns	28
	PRECHARGE command period		^{t}RP	15		20		ns	
	LOAD MODE command cycle time		^{t}MRD	2		2		^{t}CK	
	OCD Drive mode delay		^{t}OIT	0	12	0	12	ns	
	CKE low to CK,CK# uncertainty		^{t}DELAY	4.375	4.375	5.83	5.83	ns	29
Refresh	REFRESH to REFRESH command interval	512MB	^{t}RFC	75	70,000	75	70,000	ns	14
		1GB		105		105			
		2GB		127.5		127.5			
	Average periodic refresh interval		^{t}REFI		7.8		7.8	µs	14

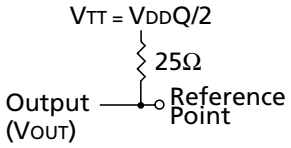
Table 18: AC Operating Conditions (Continued)

Notes: 1–5; notes appear on page 25; 0°C ≤ T_{OPR} ≤ +55°C; VDDQ = +1.8V ±0.1V, VDD = +1.8V ±0.1V

AC CHARACTERISTICS			-53E		-40E			
PARAMETER		SYMBOL	MIN	MAX	MIN	MAX	UNITS	NOTES
Self Refresh	Exit self refresh to non-READ command	tXSNR	tRFC (MIN) + 10		tRFC (MIN) + 10		ns	
	Exit self refresh to READ command	tXSRD	200		200		tCK	
	Exit self refresh timing reference	tISXR	250		350		ps	6, 30
ODT	ODT turn-on delay	tAOND	2	2	2	2	tCK	
	ODT turn-on	tAON	tAC (MIN)	tAC (MAX) + 1,000	tAC (MIN)	tAC (MAX) + 1000	ps	26
	ODT turn-off delay	tAOFD	2.5	2.5	2.5	2.5	tCK	
	ODT turn-off	tAOF	tAC (MIN)	tAC (MAX) + 600	tAC (MIN)	tAC (MAX) + 600	ps	27
	ODT turn-on (power-down mode)	tAONPD	tAC (MIN) + 2000	2 x tCK + tAC (MAX) + 1,000	tAC (MIN) + 2,000	2 x tCK + tAC (MAX) + 1000	ps	
	ODT turn-off (power-down mode)	tAOFPD	tAC (MIN) + 2,000	2.5 x tCK + tAC (MAX) + 1,000	tAC (MIN) + 2,000	2.5 x tCK + tAC (MAX) + 1,000	ps	
	ODT to power-down entry latency	tANPD	3		3		tCK	
	ODT power-down exit latency	tAXPD	8		8		tCK	
Power-Down	Exit active power-down to READ command, MR[bit12=0]	tXARD	2		2		tCK	
	Exit active power-down to READ command, MR[bit12=1]	tXARDS	6 - AL		6 - AL		tCK	
	Exit precharge power-down to any non-READ command.	tXP	2		2		tCK	
	Exit precharge power-down to READ command.	tXPRD	6 - AL		6 - AL		tCK	
	CKE minimum high/low time	tCKE	3		3		tCK	

Notes

1. All voltages referenced to V_{SS}.
2. Tests for AC timing, I_{DD}, and electrical AC and DC characteristics may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. Outputs measured with equivalent load:



4. AC timing and I_{DD} tests may use a V_{IL}-to-V_{IH} swing of up to 1.0V in the test environment and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals used to test the device is 1.0V/ns for signals in the range between V_{IL} (AC) and V_{IH} (AC).
5. The AC and DC input level specifications are as defined in the SSTL_18 standard (i.e., the receiver will effectively switch as a result of the signal crossing the AC input level and will remain in that state as long as the signal does not ring back above [below] the DC input LOW [HIGH] level).
6. Command/Address minimum input slew rate = 1.0V/ns and is referenced to the crosspoint of CK/CK#. ^{t}IS timing is referenced to Vih(ac) for a rising signal and V_{IL} (AC) for a falling signal . tIH timing is referenced to V_{IH} (DC) for a rising signal and V_{IL} (DC) for a falling signal. Derating values for Command/Address input signal slew rates < 1.0V/ns are TBD.
7. Data minimum input slew rate = 1.0V/ns and is referenced to the crosspoint of DQS/DQS# if differential strobe feature is enabled. tDS timing is referenced to V_{IH} (AC) for a rising signal and V_{IL} (AC) for a falling signal. ^{t}DH timing is referenced to V_{IH} (DC) for a rising signal and V_{IL} (DC) for a falling signal. Derating values for Data input signal slew rates < 1.0V/ns are TBD.
8. ^{t}HZ and ^{t}LZ transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (^{t}HZ) or begins driving (^{t}LZ).
9. This maximum value is derived from the referenced test load. ^{t}HZ (MAX) will prevail over ^{t}DQSCK (MAX) + ^{t}RPST (MAX) condition.
10. ^{t}LZ (MIN) will prevail over a ^{t}DQSCK (MIN) + ^{t}RPRE (MAX) condition.
11. The intent of the Don't Care state after completion of the postamble is the DQS-driven signal should either be high, low or high-Z and that any signal transition within the input switching region must follow valid input requirements. That is if DQS transitions high [above V_{IH} DC (MIN)] then it must not transition low (below V_{IH} DC) prior to ^{t}DQSH(min).
12. This is not a device limit. The device will operate with a negative value, but system performance could be degraded due to bus turnaround.
13. It is recommended that DQS be valid (HIGH or LOW) on or before the WRITE command. The case shown (DQS going from High-Z to logic LOW) applies when no WRITEs were previously in progress on the bus. If a previous WRITE was in progress, DQS could be HIGH during this time, depending on ^{t}DQSS.
14. The refresh period is 64ms. This equates to an average refresh rate of 7.8125µs. However, an REFRESH command must be asserted at least once every 70.3µs or ^{t}RFC (MAX); issuing more than eight REFRESH commands back-to-back at ^{t}RFC (MIN) is not allowed.
15. Each byte lane has a corresponding DQS.
16. CK and CK# input slew rate must be ≥ 1 V/ns (≥ 2 V/ns if measured differentially).
17. The data valid window is derived by achieving other specifications: ^{t}HP, (^{t}CK/2), ^{t}DQSQ, and ^{t}QH (^{t}QH = ^{t}HP - ^{t}QHS). The data valid window derates in direct proportion to the clock duty cycle and a practicle data valid window can be derived.
18. ^{t}JIT specification is currently TBD.
19. MIN(^{t}CL, ^{t}CH) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for ^{t}CL and ^{t}CH). For example, ^{t}CL and ^{t}CH are = 50 percent of the period, less the half period jitter [^{t}JIT(HP)] of the clock source, and less the half period jitter due to cross talk [^{t}JIT(cross talk)] into the clock traces.
20. ^{t}HP (MIN) is the lesser of ^{t}CL minimum and ^{t}CH minimum actually applied to the device CK and CK# inputs.

21. READs and WRITEs with auto precharge *are* allowed to be issued before ^{t}RAS (MIN) is satisfied since ^{t}RAS lockout feature is supported in DDR2 SDRAM.
22. VIL/VIH DDR2 overshoot/undershoot. Refer to 256Mb, 512Mb, or 1Gb DDR2 SDRAM component data sheet for more detailed information.
23. ^{t}DAL = (nWR) + (^{t}RP/^{t}CK): For each of the terms above, if not already an integer, round to the next highest integer. ^{t}CK refers to the application clock period; nWR refers to the ^{t}WR parameter stored in the MR[11,10,9]. Example: For -53E at tCK = 3.75 ns with ^{t}WR programmed to four clocks. ^{t}DAL = 4 + (15 ns/3.75 ns) clocks = 4 +(4)clocks = 8 clocks.
24. This is a minimum requirement. Minimum READ to internal PRECHARGE timing is AL + BL/2 providing the ^{t}RTP and ^{t}RAS (MIN) have been satisfied. The DDR2 SDRAM will automatically delay the internal PRECHARGE command until ^{t}RAS (MIN) has been satisfied.
25. Operating frequency is only allowed to change during self refresh mode or precharge power-down mode. Anytime the operating frequency is changed, not including jitter, the DLL is required to be reset, followed by 200 clock cycles.
26. ODT turn-on time ^{t}AON (MIN) is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn-on time ^{t}AON (MAX) is when the ODT resistance is fully on. Both are measured from ^{t}AOND.
27. ODT turn-off time ^{t}AOF (MIN) is when the device starts to turn off ODT resistance. ODT turn off time ^{t}AOF (MAX) is when the bus is in high impedance. Both are measured from ^{t}AOFD.
28. This parameter has a two clock minimum requirement at any ^{t}CK.
29. ^{t}DELAY is calculated from ^{t}IS + ^{t}CK + ^{t}IH so that CKE registration LOW is guaranteed prior to CK, CK# being removed in a system RESET condition.
30. ^{t}ISXR is equal to ^{t}IS and is used for CKE setup time during self refresh exit.

Table 19: Register Timing Requirements and Switching Characteristics

SYMBOL	PARAMETER	CONDITION	0°C ≤ T_{OPR} ≤ +55°C, V_{DD} = +1.8V ±0.1V		UNITS
			MIN	MAX	
V_{OH}		I_{OH} = -TBD mA	TBD	–	V
V_{OL}		I_{OL} = TBD mA	–	TBD	V
I_I	All Inputs	V_I = V_{DD} or GND	–	5	µA
I_{DD}	Static Standby	RESET# = GND	–	100	µA
	Static Operating	RESET# = V_{DD}, V_I = V_{IH}(AC) or V_{IL}(AC), I_0 = 0	–	TBD	mA
I_{DDD}	Dynamic Operating – Clock Only	RESET# = V_{DD}, V_I = V_{IH}(AC) or V_{IL}(AC), I_0 = 0; CK and CK# switching 50% duty cycle	TBD	TBD	µA
	Dynamic Operating – per each data input, 1:1 mode	RESET# = V_{DD}, V_I = V_{IH}(AC) or V_{IL}(AC), I_0 = 0; CK and CK# switching 50% duty cycle; one data input switching at $^tCK/2$, 50% duty cycle	TBD	TBD	
	Dynamic Operating – per each data input, 1:2 mode	RESET# = V_{DD}, V_I = V_{IH}(AC) or V_{IL}(AC), I_0 = 0; CK and CK# switching 50% duty cycle; one data input switching at $^tCK/2$, 50% duty cycle	TBD	TBD	
C_I	Data Inputs	V_I = V_{REF} ±250mV	2.5	3.5	pF
	CK and CK#	V_{ICR} = 0.9V, V_{ID} = 600mV	2	3	
	RESET	V_I = V_{DD} or GND	TBD	TBD	

Table 20: Register Electrical Characteristics

Note: 1

REGISTER	SYMBOL	PARAMETER	CONDITION	0°C ≤ T_{OPR} ≤ +55°C, V_{DD} = +1.8V ±0.1V		UNITS	NOTES
				MIN	MAX		
SSTL (bit pattern by JESD82)	f_{clock}	Clock Frequency		–	270	MHz	
	t_w	Pulse Duration		1	–	ns	
	t_{act}	Differential Inputs Active Time		–	TBD	ns	2, 3
	t_{inact}	Differential Inputs Inactive Time		–	TBD	ns	2, 4
	t_{su}	Setup Time	Data Before CK HIGH, CK# LOW	0.7	–	ns	
			Data Before CK HIGH, CK# LOW	0.5	–	ns	
			ODT, CKE, and Data before CK HIGH, CK# LOW	0.5	–		
	t_h	Hold Time	OKE, CKE, and Data after CK HIGH, CK# LOW	0.50	–	ns	

NOTE:

1. Timing and switching specifications for the register listed above are critical for proper operation of the DDR2 SDRAM Registered DIMMs. These are meant to be a subset of the parameters for the specific device used on the module. Detailed information for this register is available in JEDEC Standard JESD82.
2. This parameter is not necessarily production tested.
3. Data inputs must be low a minimum time of t_{act} (MAX), after RESET# is taken HIGH.
4. Data and clock inputs must be held at valid levels (not floating) a minimum time of t_{inact} (MAX), after RESET# is taken LOW.

Table 21: PLL Clock Driver Electrical Characteristics

Total I_{DD} = I_{DDQ} = I_{ADD} = F_{CK} x C_{PD} x V_{DDQ}, solving for C_{PD} = (I_{DDQ} + I_{ADD})/(F_{CK} x V_{DDQ}) where F_{CK} is the input frequency, V_{DDQ} is the power supply and $_{Cpd}$ is the power dissipation capacitance

SYMBOL	PARAMETER	TEST CONDITION	0°C ≤ T_{OPR} ≤ +55°C V_{DD} = +1.8V ±0.1V			UNITS	NOTES
			MIN	NOMINAL	MAX		
V_{IK}	All inputs	I_I = -18mA	–	–	-1.2	V	
V_{OH}	High output voltage	I_{OH} = -100µA	V_{DDQ}/2 - 0.2	–	–	V	
		I_{OH} = -9mA	1.1	–	–	V	
V_{OL}	Low output voltage	I_{OL} = 100µA		–	0.1	µA	
		I_{OL} = 9mA			0.6	V	
I_{ODL}	Output disabled low current	OE = L, V_{ODL} = 100mV	100	–	–	µA	
V_{OD}	Output differential voltage, the magnitude of the difference between the true and complimentary outputs		0.5	–	–	V	
I_I	CK, CK#	V_I = V_{DDQ} or GND	–	–	±250	µA	
I_{DDLD}	Static supply current: I_{DDQ} + I_{ADD}	CK and CK# = L	–	–	500	µA	
I_{DD}	Dynamic supply current: I_{DDQ} + I_{ADD}	CK and CK# = 270 MHz, all outputs are open (not connected to a PCB)	–	–	300	mA	1
C_I	CI and CK#	V_I = V_{DDQ} or GND	2	–	3	pF	
$C_I(\Delta)$	CI and CK#	V_I = V_{DDQ} or GND	V_{DDQ}/2 - 0.2	–	0.25	pF	

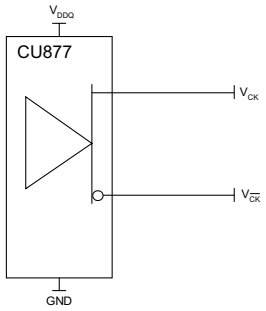
Table 22: PLL Clock Driver Timing Requirements and Switching Characteristics

Note: 1

PARAMETER	SYMBOL	0°C ≤ T_{OPR} ≤ +55°C VDD = 1.85V ± 0.1V			UNITS	NOTES
		MIN	NOMINAL	MAX		
Output Enable to any Y/Y#	^tEN	–	–	8	ns	
Output Enable to any Y/Y#	^tDIS	–	–	8	ns	
Cycle to Cycle Jitter	$^tJIT_{CC}$	-40	–	40	ps	
Static Phase Offset	$^t\varnothing$	-50	0	50	ps	2
Dynamc Phase Offset	$^t\varnothing_{dyn}$	-50	0	50	ps	2
Output Clock Skew	^tSK_O	–	–	40	ps	
Period Jitter	$^tJIT_{PER}$	-40	–	40	ps	3, 4
Half-Period Jitter	$^tJIT_{HPER}$	-75	–	75	ps	3
Input Clock Slew Rate	^tLS_I	1.0	2.5	4	V/ns	
Output Clock Slew Rate	^tLS_O	1.5	2.5	3	V/ns	6
Output Differential-Pair Cross-Voltage	VOX	VDDQ/2 - 0.1	–	VDDQ/2 + 0.1	V	5
SSC Modulation Frequency		30	–	33	kHZ	
SSC Clock Input Frequency Deviation		0.0	–	-0.50	%	
PLL Loop Bandwidth (-3dB from unity gain)		2.0	–	–	MHz	

NOTE:

1. Timing and switching specifications for the PLL listed above are critical for proper operation of the DDR2 SDRAM Registered DIMMs. These are meant to be a subset of the parameters for the specific device used on the module. Detailed information for this PLL is available in JEDEC Standard JESD82.
2. Static Phase Offset does not include Jitter.
3. Period Jitter and Half-Period Jitter specifications are separate specifications that must be met independently of each other.
4. Design target is 60ps, unless it is unachievable.
5. VOX spedified at the DRAM clock input, or the test load.
6. The Output Slew Rate is determined from the IBIS model:



SPD Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions (Figure 12, Data Validity, and Figure 13, Definition of Start and Stop).

SPD Start Condition

All commands are preceded by the start condition, which is a HIGH-to-LOW transition of SDA when SCL is HIGH. The SPD device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

SPD Stop Condition

All communications are terminated by a stop condition, which is a LOW-to-HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the SPD device into standby power mode.

SPD Acknowledge

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data (Figure 14, Acknowledge Response From Receiver).

The SPD device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a WRITE operation have been selected, the SPD device will respond with an acknowledge after the receipt of each subsequent eight-bit word. In the read mode the SPD device will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to standby power mode.

Figure 12: Data Validity

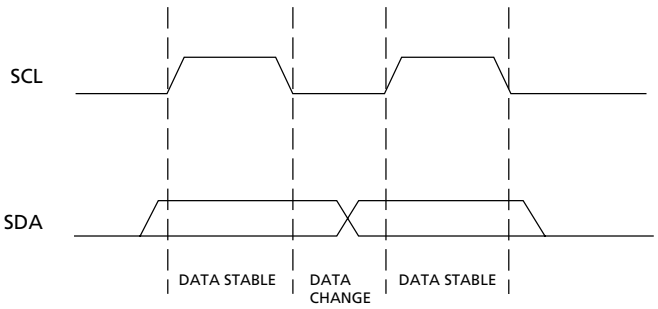


Figure 13: Definition of Start and Stop

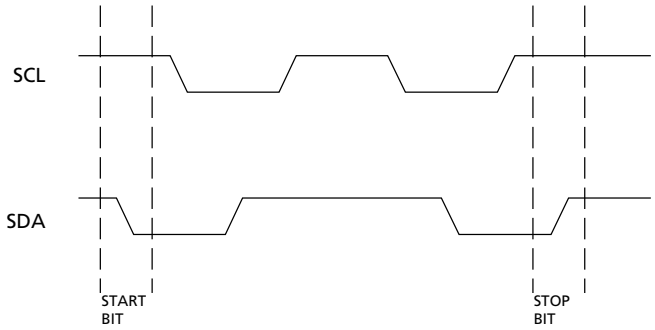


Figure 14: Acknowledge Response From Receiver

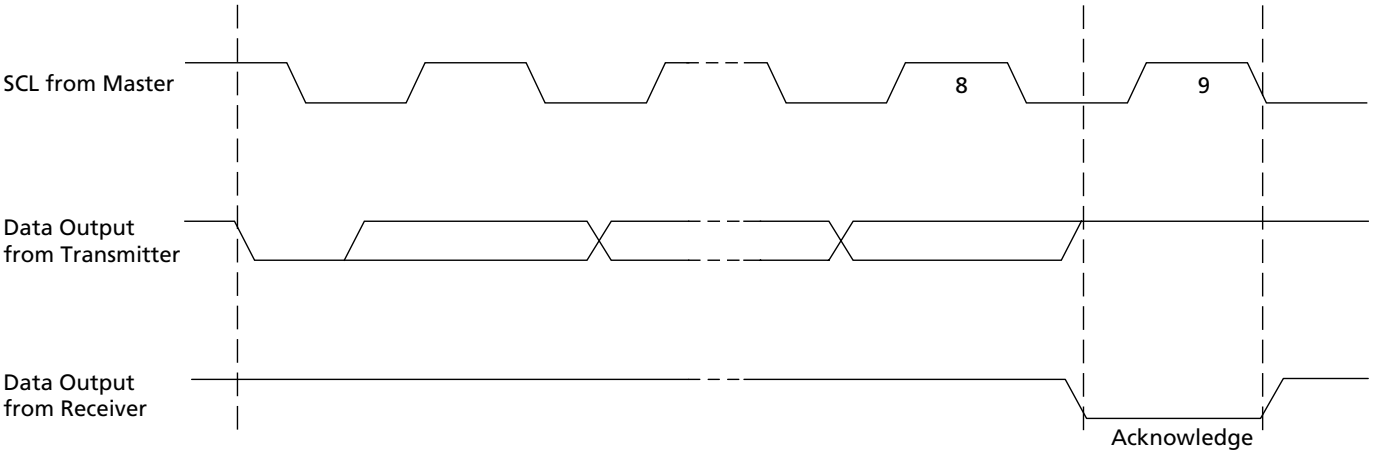


Table 23: EEPROM Device Select Code

The most significant bit (b7) is sent first

SELECT CODE	DEVICE TYPE IDENTIFIER				CHIP ENABLE			RW
	b7	b6	b5	b4	b3	b2	b1	b0
Memory Area Select Code (two arrays)	1	0	1	0	SA2	SA1	SA0	RW
Protection Register Select Code	0	1	1	0	SA2	SA1	SA0	RW

Table 24: EEPROM Operating Modes

MODE	RW BIT	WC	BYTES	INITIAL SEQUENCE
Current Address Read	1	VIH or VIL	1	START, Device Select, RW = '1'
Random Address Read	0	VIH or VIL	1	START, Device Select, RW = '0', Address
	1	VIH or VIL	1	reSTART, Device Select, RW = '1'
Sequential Read	1	VIH or VIL	≥ 1	Similar to Current or Random Address Read
Byte Write	0	VIL	1	START, Device Select, RW = '0'
Page Write	0	VIL	≤ 16	START, Device Select, RW = '0'

Figure 15: SPD EEPROM Timing Diagram

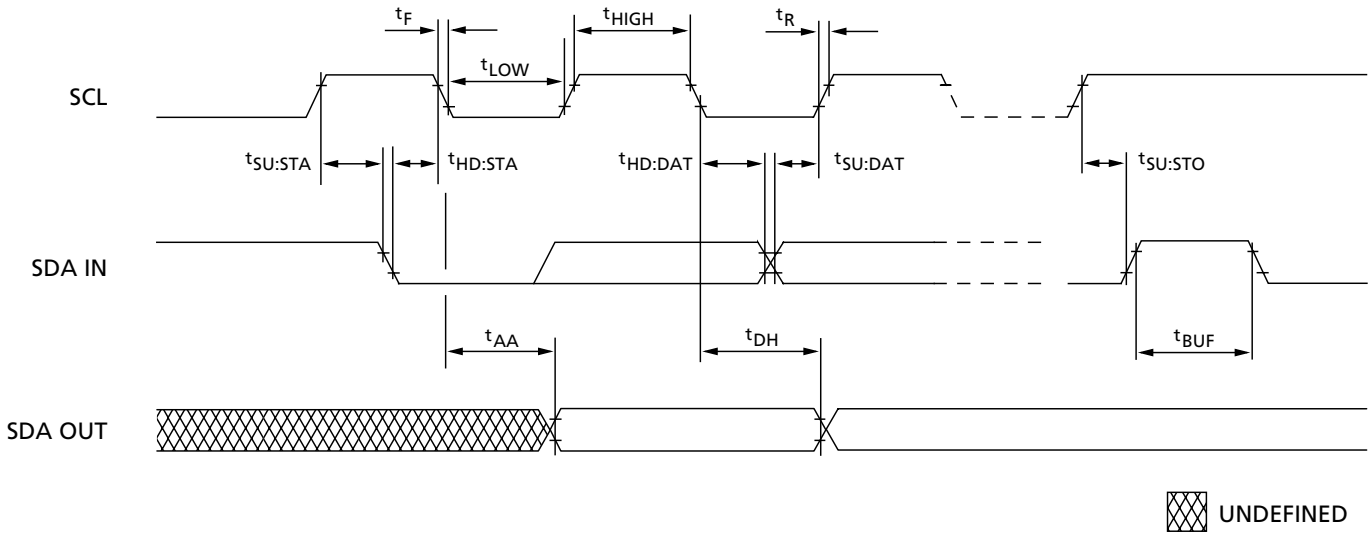


Table 25: Serial Presence-Detect EEPROM DC Operating Conditions

All voltages referenced to V_{SS}; V_{DDSPD} = +1.7V to +3.6V

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS
Supply Voltage	V_{DDSPD}	1.7	3.6	V
Input High Voltage: Logic 1; All inputs	V_{IH}	V_{DDSPD} x 0.7	V_{DDSPD} + 0.5	V
Input Low Voltage: Logic 0; All inputs	V_{IL}	-0.6	V_{DDSPD} x 0.3	V
Output Low Voltage: I_{OUT} = 3mA	V_{OL}	–	0.4	V
Input Leakage Current: V_{IN} = GND to V_{DD}	I_{LI}	0.10	3	µA
Output Leakage Current: V_{OUT} = GND to V_{DD}	I_{LO}	0.05	3	µA
Standby Current:	I_{SB}	1.6	4	µA
Power Supply Current, READ: SCL clock frequency = 100 KHz	ICC_R	0.4	1	mA
Powr Supply Current, WRITE: SCL clock frequency = 100 KHz	ICC_W	2	3	mA

Table 26: Serial Presence-Detect EEPROM AC Operating Conditions

All voltages referenced to V_{SS}; V_{DDSPD} = +1.7V to +3.6V

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
SCL LOW to SDA data-out valid	^tAA	0.2	0.9	µs	1
Time the bus must be free before a new transition can start	^tBUF	1.3		µs	
Data-out hold time	^tDH	200		ns	
SDA and SCL fall time	^tF		300	ns	2
Data-in hold time	$^tHD:DAT$	0		µs	
Start condition hold time	$^tHD:STA$	0.6		µs	
Clock HIGH period	^tHIGH	0.6		µs	
Noise suppression time constant at SCL, SDA inputs	^tI		50	ns	
Clock LOW period	^tLOW	1.3		µs	
SDA and SCL rise time	^tR		0.3	µs	2
SCL clock frequency	^fSCL		400	KHz	
Data-in setup time	$^tSU:DAT$	100		ns	
Start condition setup time	$^tSU:STA$	0.6		µs	3
Stop condition setup time	$^tSU:STO$	0.6		µs	
WRITE cycle time	^tWRC		10	ms	4

NOTE:

1. To avoid spurious START and STOP conditions, a minimum delay is placed between SCL = 1 and the falling or rising edge of SDA.
2. This parameter is sampled.
3. For a reSTART condition, or following a WRITE cycle.
4. The SPD EEPROM WRITE cycle time (^tWRC) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal erase/program cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistor, and the EEPROM does not respond to its slave address.

Table 27: Serial Presence-Detect Matrix

"1"/"0": Serial Data, "driven to HIGH"/"driven to LOW"

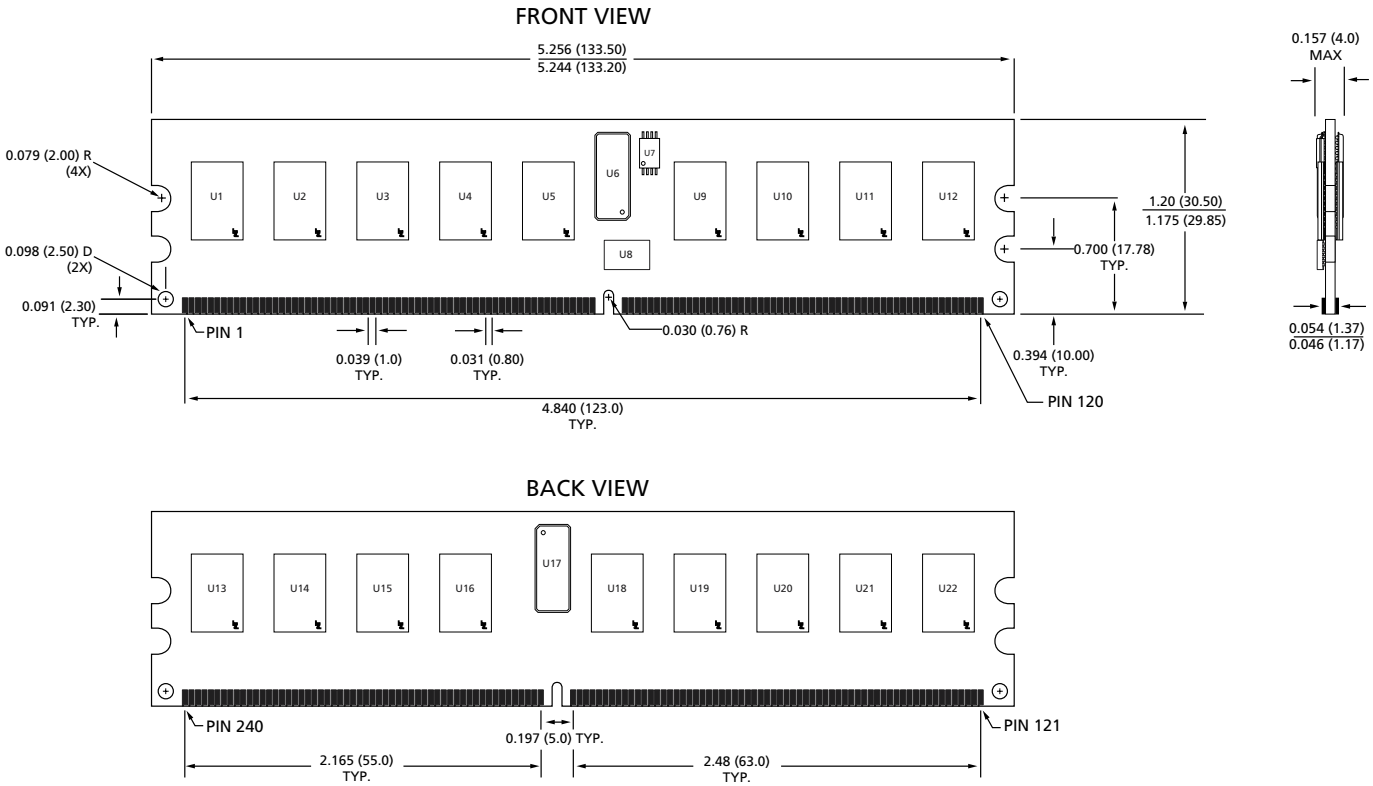
BYTE	DESCRIPTION	ENTRY (VERSION)	MT18HTF6472D	MT18HTF12872D	MT18HTF25672D
0	Number of SPD Bytes Used by Micron	128	80	TBD	TBD
1	Total Number of Bytes in SPD Device	256	08	TBD	TBD
2	Fundamental Memory Type	SDRAM DDR2	08	TBD	TBD
3	Number of Row Addresses on Assembly	13 or 14	0D	TBD	TBD
4	Number of Column Addresses on Assembly	10	0A	TBD	TBD
5	DIMM Height and Module Ranks	1.18in., Dual Rank	61	TBD	TBD
6	Module Data Width	64	48	TBD	TBD
7	Module Data Width (Continued)	0	00	TBD	TBD
8	Module Voltage Interface Levels	SSTL 1.8V	05	TBD	TBD
9	SDRAM Cycle Time, ^{t}CK (CAS Latency = 4)	-53E -40E	3D 50	TBD	TBD
10	SDRAM Access from Clock, ^{t}AC (CAS Latency = 4)	-53E -40E	50 60	TBD	TBD
11	Module Configuration Type	ECC	02	TBD	TBD
12	Refresh Rate/Type	7.81µs/SELF	82	TBD	TBD
13	SDRAM Device Width (Primary SDRAM)	8	08	TBD	TBD
14	Error-checking SDRAM Data Width	8	08	TBD	TBD
15	Minimum Clock Delay, Back-to-Back Random Column Access	1 clock	00	TBD	TBD
16	Burst Lengths Supported	4, 8	0C	TBD	TBD
17	Number of Banks on SDRAM Device	4	04	TBD	TBD
18	CAS Latencies Supported	2, 3, 4	18	TBD	TBD
19	Reserved	0	00	TBD	TBD
20	DDR2 DIMM Type	RDIMM	01	TBD	TBD
21	SDRAM Module Attributes		00	TBD	TBD
22	SDRAM Device Attributes: General	Weak Driver	01	TBD	TBD
23	SDRAM Cycle Time, ^{t}CK, (CAS Latency = 3)	-53E -40E	50 50	TBD	TBD
24	SDRAM Access from CK, ^{t}AC, (CAS Latency = 3)	-53E -40E	50 60	TBD	TBD
25	SDRAM Cycle Time, ^{t}CK, (CAS Latency = 2)	N/A	00	TBD	TBD
26	SDRAM Access from CK, ^{t}AC, (CAS Latency = 2)	N/A	00	TBD	TBD
27	Minimum Row Precharge Time, ^{t}RP	-53E -40E	3C 3C	TBD	TBD
28	Minimum Row Active to Row Active, ^{t}RRD	-53E -40E	1E 1E	TBD	TBD
29	Minimum RAS# to CAS# Delay, ^{t}RCD	-53E -40E	3C 3C	TBD	TBD
30	Minimum RAS# Pulse Width, ^{t}RAS	-53E -40E	2D 2D	TBD	TBD
31	Module Rank Density	256MB, 512MB, 1GB	40	TBD	TBD

Table 27: Serial Presence-Detect Matrix

"1"/"0": Serial Data, "driven to HIGH"/"driven to LOW"

BYTE	DESCRIPTION	ENTRY (VERSION)	MT18HTF6472D	MT18HTF12872D	MT18HTF25672D
32	Address and Command Setup Time, ^{t}IS	-53E -40E	50 60	TBD	TBD
33	Address and Command Hold Time, ^{t}IH	-53E -40E	50 60	TBD	TBD
34	Data/ Data Mask Input Setup Time, ^{t}DS	-53E -40E	35 40	TBD	TBD
35	Data/ Data Mask Input Hold Time, ^{t}DH	-53E -40E	35 40	TBD	TBD
36	Write Recovery Time, ^{t}WR		3C	TBD	TBD
37	Write to Read CMD Delay, ^{t}WTR	-53E -40E	1E 28	TBD	TBD
38	Read to Precharge CMD Delay, ^{t}RTP		1E	TBD	TBD
39	Mem Analysis Probe		00	TBD	TBD
40	Extension for bytes 41 and 42		00	TBD	TBD
41	Min Active Auto Refresh Time, ^{t}RC		3C	TBD	TBD
42	Minimum Auto Refresh to Active/ Auto Refresh Command Period, ^{t}RFC		4B	TBD	TBD
43	SDRAM Device Max Cycle Time, ^{t}CKMAX		80	TBD	TBD
44	SDRAM Device Max DQS-DQ Skew Time, ^{t}DQSQ	-53E -40E	1E 23	TBD	TBD
45	SDRAM Device Max Read Data Hold Skew Factor, ^{t}QHS	-53E -40E	28 2D	TBD	TBD
46	PLL Relock Time		0F	TBD	TBD
47-61	Reserved	Reserved	00	TBD	TBD
62	SPD Revision	Release 1.0	10	10	10
63	Checksum For Bytes 0-62	-53E -40E	31 AE	TBD TBD	TBD TBD
64	Manufacturer's JEDEC ID Code	MICRON	2C	2C	2C
65-71	Manufacturer's JEDEC ID Code	(Continued)	FF	FF	FF
72	Manufacturing Location	01–12	01–0C	01–0C	01–0C
73-90	Module Part Number (ASCII)		Variable Data	Variable Data	Variable Data
91	PCB Identification Code	1-9	01-09	01-09	01-09
92	Identification Code (Continued)	0	00	00	00
93	Year of Manufacture in BCD		Variable Data	Variable Data	Variable Data
94	Week of Manufacture in BCD		Variable Data	Variable Data	Variable Data
95-98	Module Serial Number		Variable Data	Variable Data	Variable Data
99-127	Manufacturer-Specific Data (RSVD)		–	–	–

Figure 16: 240-pin DDR2 DIMM Dimensions



NOTE:

All dimensions are in inches (millimeters); $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

Data Sheet Designation

Advance: This datasheet contains initial descriptions of products still under development. The Advance designation applies to MT18HTF12872D and MT18HTF25672D only.

Preliminary: Initial characterization limits, subject to change upon full characterization of production devices. The Preliminary designation applies to MT18HTF6472D only.

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