# TRAILING EDGE PRODUCT - MINIMUM ORDER APPLIES PRODUCT MAY BE MADE OBSOLETE WITHOUT NOTICE



# 128K x 8 SRAM

# MSM8128 - 85/10/12

Issue 4.4 : February 2000

#### Description

The MSM8128 is a 1Mbit monolithic SRAM organised as 128K x 8. It is available in with access times of 85, 100 & 120ns. It has a low power standby version and has 3.0V battery backup capability. It is directly TTL compatible and has common data inputs and outputs. Two pinout variants (single and dual CS) are available.

All versions may be screened in accordance with MIL-STD-883.

131,072 x 8 CMOS Static RAM

#### **Features**

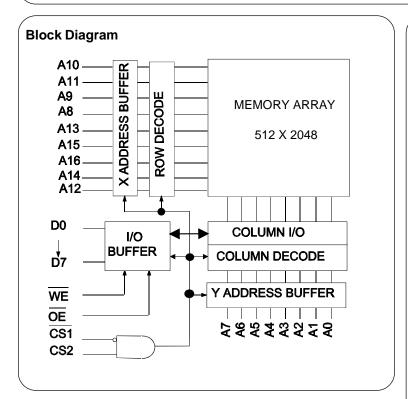
Access Times of 85/100/120 ns JEDEC standard Dual  $\overline{\text{CS}}$  footprints.

Operating Power 605 mW (max) Low Power Standby (-L) 2.53 mW (max)

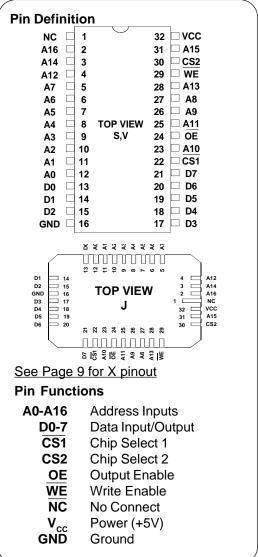
Low Voltage Data Retention.
Completely Static Operation

Directly TTL compatible.

May be processed in accordance with MIL-STD-883



Package De Pin Count	Description	Package Type
32	Flatpack	G
32	LCC	W
32	JLCC	J
Package deta	ils on pages 8 & 9.	



### **DC OPERATING CONDITIONS**

# **Absolute Maximum Ratings**

Voltage on any pin relative to V <sub>ss</sub>	$V_{T}$	-0.5V	to	+7.0	V
Power Dissipation	$P_{T}$		1		W
Storage Temperature	$T_{\mathtt{STG}}$	-55	to	+150	°С

Notes: (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions									
		min	typ	max					
Supply Voltage	V <sub>cc</sub>	4.5	5.0	5.5	V				
Input High Voltage	V <sub>IH</sub>	2.2	-	5.8	V				
Input Low Voltage	$V_{_{\rm IL}}$	-0.3	-	8.0	V				
Operating Temperature	$T_{A}$	0	-	70	°C				
	T <sub>AI</sub>	-40	-	85	°C (I suffix)				
	T <sub>AM</sub>	-55	-	125	°C (M, MB suffix)				

DC Electrical Characteristics ( $V_{CC} = 5.0V \pm 10\%$ , $T_A = -55$ °C to +125°C)										
Parameter	Symbol	Test Condition	min	typ	max	Unit				
Input Leakage Current	I <sub>LI</sub>	$V_{IH}$ =0V to $V_{cc}$	-1	-	1	μΑ				
Output Leakage Current	I <sub>1/0</sub>	$\overline{\text{CS1}} = V_{\text{IH}}$ , CS2 = $V_{\text{IL}}$ , $V_{\text{I/O}} = 0V$ to $V_{\text{cc}}$ , $\overline{\text{OE}} = V_{\text{IH}}$	-1	-	1	μΑ				
Average Supply Current		Min. Cycle, V <sub>IN</sub> =V <sub>IL</sub> or V <sub>IH</sub>	-	-	110	mΑ				
Standby Supply Current	I <sub>SB1</sub>	$\overline{\text{CS1}} = V_{\text{IH}}, \text{CS2} = V_{\text{IL}}, \text{ I/P's static}$	-	-	3.5	mΑ				
-L Part	$I_{\mathtt{SB2}}$	$\overline{\text{CS1}} \ge \text{V}_{\text{CC}}$ -0.2V, 0.2V $\ge \text{CS2} \ge \text{V}_{\text{CC}}$ -0.2V , $\text{V}_{\text{IN}} \ge 0.2$ V	-	-	460	uA				
Output Voltage	$V_{OL}$	I <sub>OL</sub> = 2.1 mA	-	-	0.4	V				
	$V_{OH}$	$I_{OH} = -1.0 \text{ mA}$	2.4	-	-	V				

Capacitance (V <sub>CC</sub> =5V±10%,T <sub>A</sub> =25°C)								
Parameter	Symbol	Test Condition	typ	max	Unit			
I/P Capacitance	$C_{_{IN}}$	V <sub>IN</sub> =0V	-	8	pF			
I/O Capacitance	$C_{_{I/O}}$	$V_{I/O}=0V$	-	10	pF			

Note: This parameter is sampled and not 100% tested.

MSM8128-70/85/10/12

## **Operating Modes**

The table below shows the logic inputs required to control the MSM8128 SRAM.

Mode	CS1	CS2	ŌĒ	WE	V <sub>cc</sub> Current	I/O Pin	Reference Cycle
Not Selected	1	Х	Х	Х		High Z	Power Down
Not Selected	Х	0	Х	Х	I <sub>SB</sub> ,I <sub>SB1</sub>	High Z	Power Down
Output Disable	0	1	1	1	I <sub>cc</sub>	High Z	
Read	0	1	0	1	I <sub>cc</sub>	D <sub>OUT</sub>	Read Cycle
Write	0	1	Х	0	I <sub>cc</sub>	D <sub>IN</sub>	Write Cycle

$$1 = V_{IH}$$
,  $0 = V_{IL}$ ,  $X = Don't Care$ 

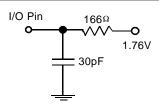
Low V <sub>cc</sub> Data Retention Characteristics - L Version Only (T <sub>A</sub> =-55°C to +125°C)									
Parameter	Symbol	Test Condition	min	typ	max	Unit			
V <sub>cc</sub> for Data Retention	$V_{DR}$	$\overline{\text{CS1}} \ge \text{V}_{\text{cc}}$ -0.2V, CS2 $\ge \text{V}_{\text{cc}}$ -0.2V or							
		$0V \le CS2 \le 0.2V. V_{IN} \ge 0V$	2.0	-	-	V			
Data Retention Current	I <sub>CCDR</sub>	$V_{CC}=3.0V, V_{IN} \ge 0V, \overline{CS1} \ge V_{CC}-0.2V,$							
		$CS2 \ge V_{CC}$ -0.2V or $0V \le CS2 \le 0.2V$ .	-	-	700	μΑ			
Chip Deselect to Data Retention	n t <sub>CDR</sub>	See Retention Waveform	0	-	-	ns			
Operation Recovery Time	t <sub>B</sub>	See Retention Waveform	5	-	-	ms			

Notes (1) CS2 controls address buffer, WE buffer,  $\overline{\text{CS1}}$  buffer and  $\overline{\text{OE}}$  buffer. If CS2 controls data retention mode, Vin levels ( $\overline{\text{WE}}$ , $\overline{\text{OE}}$ , $\overline{\text{CS1}}$ ,I/O) can be in the high impedance state. If  $\overline{\text{CS1}}$  controls Data Retention mode, CS2 must be ≥ V<sub>CC</sub> - 0.2V or 0V ≤ CS2 ≤ 0.2V. The other input levels (address,  $\overline{\text{WE}}$ , $\overline{\text{OE}}$ ,I/O) can be in the high impedance state.

# AC Test Conditions

**Output Load** 

- \* Input pulse levels: 0V to 3.0V
- \* Input rise and fall times: 5ns
- \* Input and Output timing reference levels: 1.5V
- \* Output load: See Load Diagram
- \* V<sub>cc</sub>=5V±10%



# **AC OPERATING CONDITIONS**

# Read Cycle

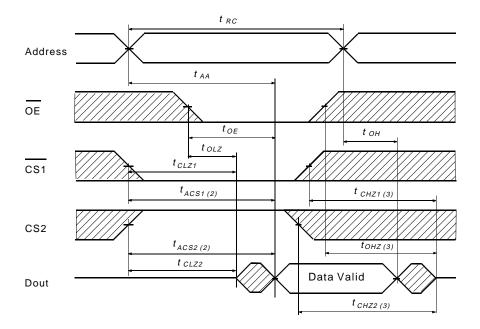
			ε	35	1	0	1	2	
Parameter	Symbol	\/bbib///bb/ax//	min	max	min	max	min	max	Unit
Read Cycle Time	t <sub>RC</sub>	V/398/////////	85	-	100	-	120	-	ns
Address Access Time	t <sub>AA</sub>	<i>\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\</i>	-	85	-	100	-	120	ns
Chip Select (CS1) Access Time(2)	t <sub>ACS1</sub>	<i>\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\</i>	-	85	-	100	-	120	ns
Chip Select (CS2) Access Time(2)	t <sub>ACS2</sub>	<i>\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\</i>	-	85	-	100	-	120	ns
Output Enable to Output Valid	t <sub>OE</sub>	<i>\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\</i>	-	45	-	50	-	60	ns
Output Hold from Address Change	t <sub>oh</sub>	V/34/////////	5	-	10	-	10	-	ns
Chip Selection (CS1) to Output in Low Z	t <sub>CLZ1</sub>	<i>\(\)</i> \\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	10	-	10	-	10	-	ns
Chip Selection (CS2) to Output in Low Z	t <sub>CLZ2</sub>	<i>\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\</i>	10	-	10	-	10	-	ns
Output Enable to Output in Low Z	t <sub>OLZ</sub>	V//\$/////////	5	-	5	-	5	-	ns
Chip Disable ( $\overline{CS1}$ ) to Output in High $Z^{(3)}$		V//8////35///	0	35	0	35	0	45	ns
Chip Disable (CS2) to Output in High Z <sup>(3)</sup>		V//9////35///	0	35	0	35	0	45	ns
Output Disable to Output in High Z <sup>(3)</sup>	t <sub>OHZ</sub>	V/ <i>/9</i> //// <i>//</i> 399///	0	30	0	35	0	45	ns
	0.12		1						

Write Cycle	W	rite	Cyc	le
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			ε	3 <i>5</i>	1	0	1	2	
Parameter	Symbol	//00/00///00/a/X//	min	max	min	max	min	max	Unit
Write Cycle Time	$t_{wc}$	V/799//////////	85	-	100	-	120	-	ns
Chip Selection to End of Write	t <sub>cw</sub>	<b>1/566/////////</b>	75	-	85	-	100	-	ns
Address Valid to End of Write	t <sub>AW</sub>	V/89///////////////////////////////////	75	-	85	-	100	-	ns
Address Setup Time	t <sub>AS</sub>	<i>\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\</i>	0	-	0	-	0	-	ns
Write Pulse Width	t <sub>wp</sub>	V/58/////////	60	-	70	-	70	-	ns
Write Recovery Time (WE, CS1)	t <sub>WR1</sub>	V/15///////////////////////////////////	5	-	5	-	5	-	ns
(CS2)	t <sub>WR2</sub>	V//\$/////////	5	-	5	-	5	-	ns
Write to Output in High Z	t <sub>whz</sub>	V//9////399///	0	30	0	35	0	40	ns
Data to Write Time Overlap	t <sub>DW</sub>	V/399//////////////////////////////////	35	-	40	-	45	-	ns
Data Hold from Write Time	$t_{DH}$	<i>\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\</i>	0	-	0	-	0	-	ns
Output Active from End of Write	t <sub>ow</sub>	<i>\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\</i>	5	-	5	-	5	-	ns



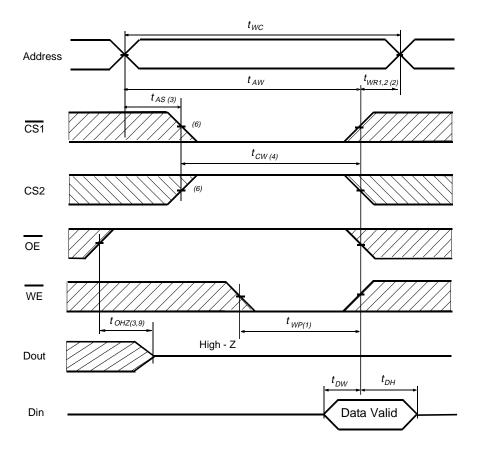
# Read Cycle Timing Waveform (1,2)



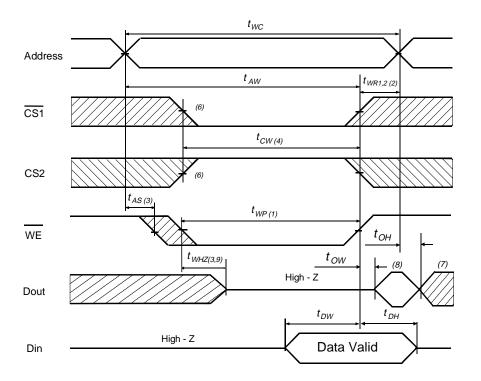
#### Notes:

- (1) WE is High for Read Cycle.
- (2) Address valid prior to or coincident with CS1 transition low or CS2 high.
- (3) t<sub>CHZ</sub> and t<sub>OHZ</sub> are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels. At any given temperature and voltage condition, t<sub>CHZ</sub> max is less than t<sub>CLZ</sub> min both for a given device and from device to device. This parameter is sampled and not 100% tested.

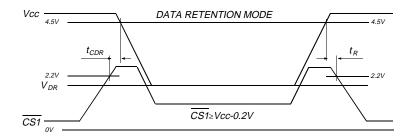
# Write Cycle No.1 Timing Waveform



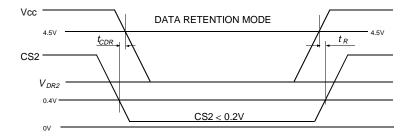
# Write Cycle No.2 Timing Waveform (5)



# Low V<sub>cc</sub> Data Retention Timing Waveform 1 (CS1 controlled)



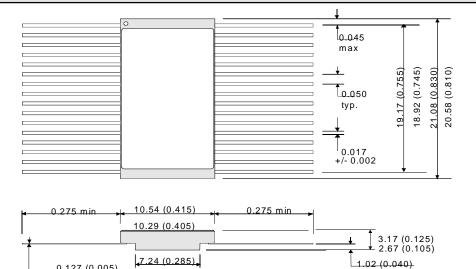
# Low V<sub>cc</sub> Data Retention Timing Waveform 2 (CS2 controlled)



#### **AC Characteristics Notes**

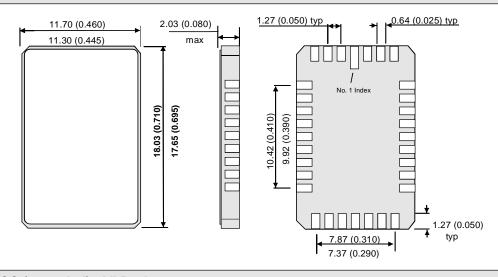
- (1) A write occurs during the overlap of a low  $\overline{CS1}$ , a high CS2 and a low  $\overline{WE}$ . A write begins at the latest transition among  $\overline{CS1}$  going low,  $\overline{CS2}$  going high and  $\overline{WE}$  going low. A write ends at the earliest transition among  $\overline{CS1}$  going high,  $\overline{CS2}$  going low and  $\overline{WE}$  going high.  $\overline{t_{WP}}$  is measured from the beginning of write to the end of write.
- (2)  $t_{WR}$  is measured from the earlier of  $\overline{CS1}$  or  $\overline{WE}$  going high or CS2 going high to the end of write cycle.
- (3) During this period, I/O pins are in the output state. Input signals out of phase must not be applied.
- (4) If  $\overline{\text{CS1}}$  goes low simultaneously with  $\overline{\text{WE}}$  going low or after  $\overline{\text{WE}}$  going low, outputs remain in high impedance state.
- (5) OE is continuously low. (OE=V<sub>11</sub>)
- (6) Dout is in the same phase as written data of this write cycle.
- (7) Dout is the read data of next address.
- (8) If CS1 is low and CS2 is high during this period, I/O pins are in the output state. Input signals out of phase must not be applied to I/O pins.
- (9) t<sub>whz</sub> is defined as the time at which the outputs achieve the open circuit conditions and is not referenced to output voltage levels. These parameters are sampled and not 100% tested.

# 32 pin Flatpack - 'G' Package

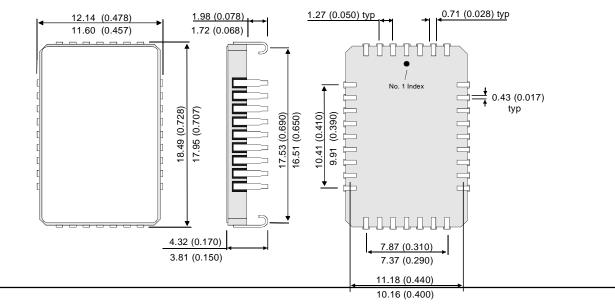


# 32 pad LCC (extended) -'W' Package

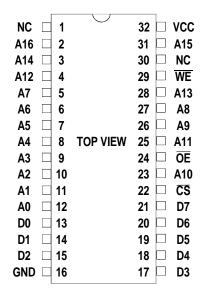
0.127 (0.005)

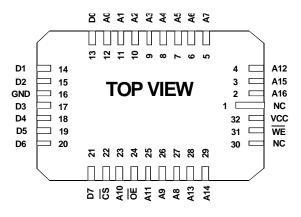


# 32 pad JLCC (extended) - 'J' Package



### **Alternate Pin Definition**



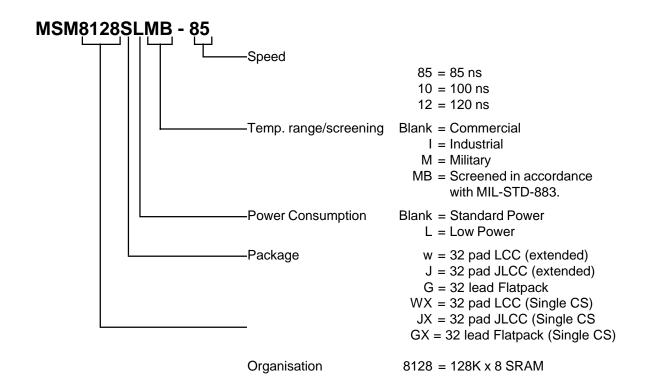


# **Military Screening Procedure**

Component Screening Flow for high reliability product is in accordance with Mil-883 method 5004

MB COMPONENT SCREENING FLOW								
SCREEN	TEST METHOD	LEVEL						
Visual and Mechanical								
Internal visual Temperature cycle Constant acceleration Pre-Burn-in electrical Burn-in	2010 Condition B or manufacturers equivalent 1010 Condition C (10 Cycles,-65°C to +150°C) 2001 Condition E (Y, only) (30,000g)  Per applicable device specifications at T <sub>A</sub> =+25°C Method 1015,Condition D,T <sub>A</sub> =+125°C,160hrs min	100% 100% 100% 100% 100%						
Final Electrical Tests	Per applicable Device Specification							
Static (dc)	a) @ T <sub>A</sub> =+25°C and power supply extremes b) @ temperature and power supply extremes	100% 100%						
Functional	<ul> <li>a) @ T<sub>A</sub>=+25°C and power supply extremes</li> <li>b) @ temperature and power supply extremes</li> </ul>	100% 100%						
Switching (ac)	a) @ T <sub>A</sub> =+25°C and power supply extremes b) @ temperature and power supply extremes	100% 100%						
Percent Defective allowable (PDA)	Calculated at post-burn-in at T <sub>A</sub> =+25°C	5%						
Hermeticity	1014							
Fine Gross	Condition A Condition C	100% 100%						
External Visual	2009 Per vendor or customer specification	100%						

#### **Ordering Information**



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