32K×8 Bit High-Speed CMOS Static RAM

FEATURES

- **Fast Access Time: 15, 20, 25ns (max)**
- **Low Power Dissipation**
  - **Standby (TTL) : 40mA (max.)**
    2mA(Max.)
  - **Operating KM68257B-15 : 150mA (max.)**
    KM68257B-20 : 140mA (max.)
    KM68257B-25 : 130mA (max.)
- **Single 5V±10% Power Supply**
- **TTL Compatible inputs and outputs**
- **Fully Static Operation**
  —No clock or refresh required
- **Three State Outputs**
- **Standard Pin Configuration**
  KM68257BP : 28-DIP-300
  KM68257BJ : 28-SOJ-300

GENERAL DESCRIPTION

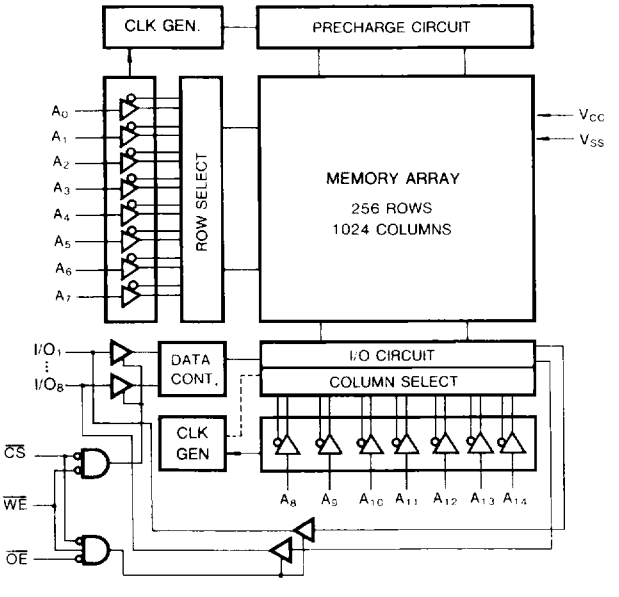
The KM68257B is a 262,144-bit high-speed Static Random Access Memory organized as 32,768 words by 8 bits.

The KM68257B uses eight common input and output lines and has an output enable pin which operates faster than address access time at read cycle. The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology.

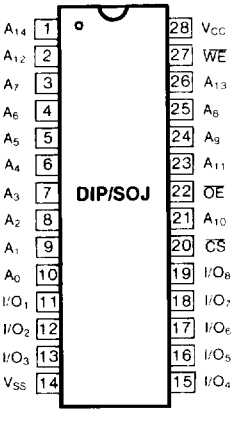
It is particularly well suited for use in high-density high-speed system applications.

The KM68257B is packaged in a 300 mil. 28-pin plastic DIP or SOJ

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top View)



Pin Name	Pin Function
A_0-A_{14}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O_1~I/O_8	Data Inputs/Outputs
V_{CC}	Power (+5V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{stg}	−65 to 150	°C
Operating Temperature	T_A	0 to 70	°C
Soldering Temperature and Time	T_{solder}	260°C, 10sec (Lead only)	—

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

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RECOMMENDED OPERATING CONDITIONS (T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.5	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

* V_{IL}(min.)=−3.0V for ⩽10ns pulse

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70°C, V_{CC}=5V±10%, unless otherwise specified)

Item	Symbol	Test Condition		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=Vss to Vcc		-	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IN} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} or $V_{I/O}$=Vss to Vcc		-	2	μA
Average Operating Current	I_{CC}	Min Cycle, 100% Duty $\overline{CS}$=V_{IL}, $I_{I/O}$=0mA	15ns	-	150	mA
			20ns	-	140	mA
			25ns	-	130	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}, Min Cycle.		-	40	mA
	I_{SB1}	$\overline{CS}$≥Vcc-0.2V, f= o V_{IN}≥Vcc-0.2 or V_{IN}≤0.2V		-	2	mA
Output Low Voltage	V_{OL}	I_{OL}=8mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4mA		2.4	-	V

CAPACITANCE* (f=1MHz, T_A=25°C)

Item	Symbol	Test Conditions	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	—	7	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	—	7	pF

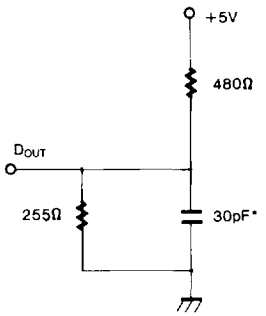
* Note: Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS

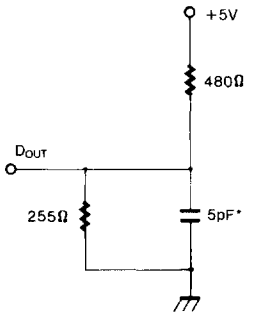
TEST CONDITIONS (T_A=0 to 70°C, V_{CC}=5V±10%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B)
(for t_{HZ}, t_{LZ}, t_{WZ}, t_{OW}, t_{OLZ} & t_{OHZ})



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM68257BP-15 KM68257BJ-15		KM68257BP-20 KM68257BJ-20		KM68257BP-25 KM68257BJ-25		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	15		20		25		ns
Address Access Time	t_{AA}		15		20		25	ns
Chip Select to Output	t_{CO}		15		20		25	ns
Output Enable to Valid Output	t_{OE}		8		10		12	ns
Chip Enable to Low-Z Output	t_{LZ}	3		3		3		ns
Output Enable to Low-Z Output	t_{OLZ}	0		0		0		ns
Chip Disable to High-Z Output	t_{HZ}	0	10	0	10	0	10	ns
Chip Disable to High-Z Output	t_{OHZ}	0	8	0	8	0	10	ns
Output Hold from Address Change	t_{OH}	3		3		3		ns
Chip Select to Power Up Time	t_{PU}	0		0		0		ns
Chip Disable to Power Down Time	t_{PD}		15		20		25	ns

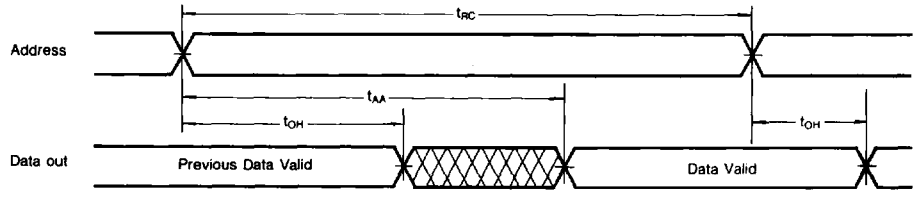
WRITE CYCLE

Parameter	Symbol	KM68257BP-15 KM68257BJ-15		KM68257BP-20 KM68257BJ-20		KM68257BP-25 KM68257BJ-25		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	15		20		25		ns
Chip Select to End of Write	t_{CW}	12		13		15		ns
Address Set-up Time	t_{AS}	0		0		0		ns
Address Valid to End of Write	t_{AW}	12		13		15		ns
Write Pulse Width	t_{WP}	12		13		15		ns
Write Recovery Time	t_{WR}	0		0		0		ns
Write to Output High-Z	t_{WZ}	0	8	0	8	0	10	ns
Data to Write Time Overlap	t_{DW}	9		10		12		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns
End Write to Output Low-Z	t_{OW}	0		0		0		ns

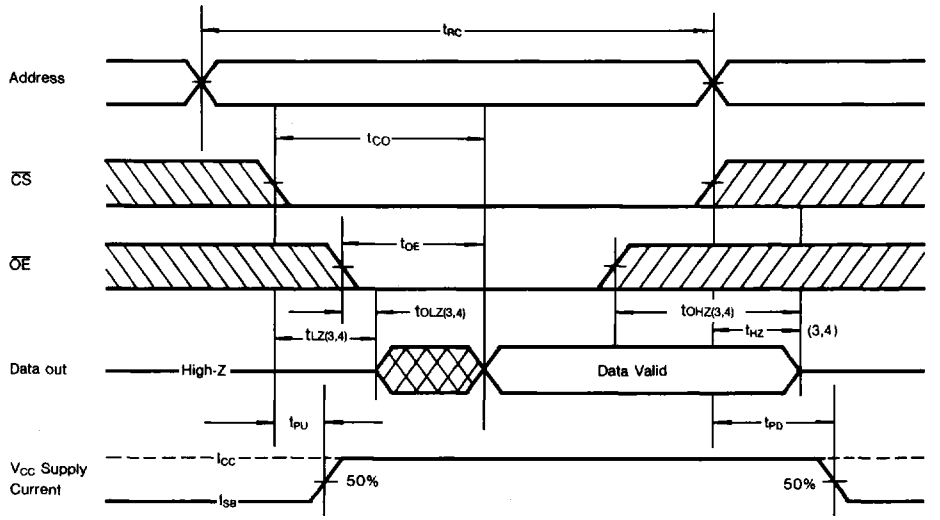
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (Address Controlled)

($\overline{CS}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH})



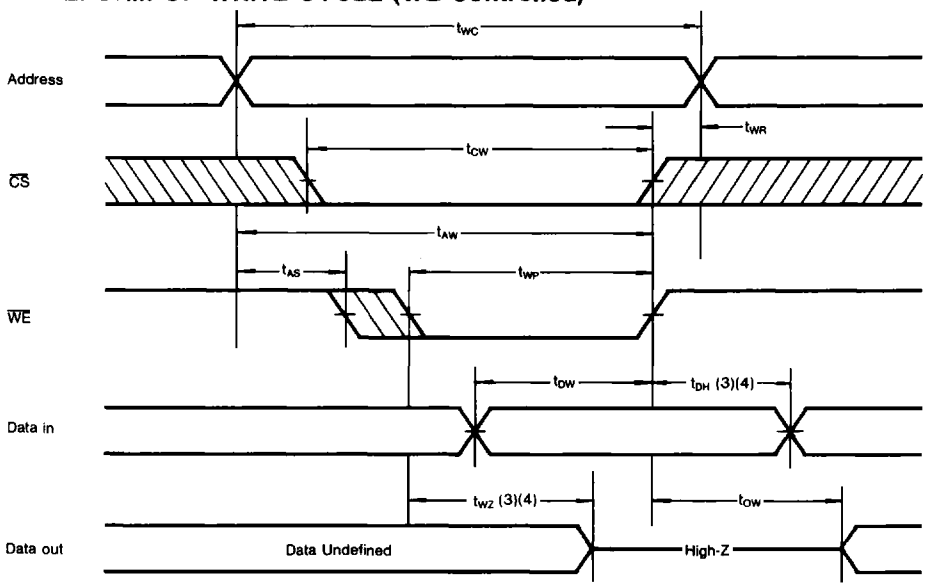
TIMING WAVEFORM OF READ CYCLE



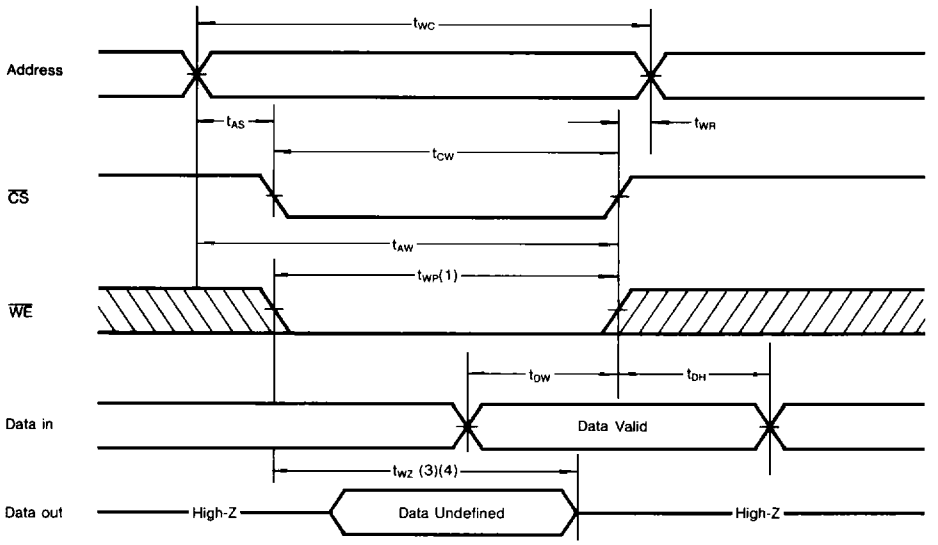
Note (READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. At any given temperature and voltage condition, t_{HZ}(max.) is less than t_{LZ}(min.) both for a given device and from device to device.
4. Transition is measured ±200mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.
5. Address valid prior to or coincident with $\overline{CS}$ transition low
6. Device is continuously selected with $\overline{CS}$=VIL.

TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS}$ Controlled)



Notes (WRITE CYCLE)

1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$.
2. All write cycle timing is referenced from the last valid address to the first transition address.
3. Transition is measured ±200mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.
4. At any given temperature and voltage condition, t_{WZ}(max.) is less than t_{OW}(min.) both for a given device and from device to device.
5. $\overline{CS}$ or $\overline{WE}$ must be in high during address transition.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X *	X	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

* Note: X means Don't Care