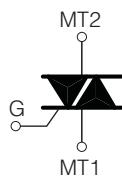
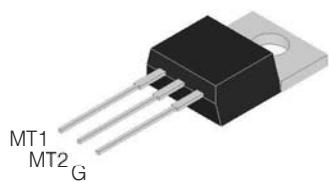


INSULATED LOGIC LEVEL TRIAC

INSULATED TO-220AB



On-State Current

8 Amp

Gate Trigger Current

 $\leq 10 \text{ mA (08)}$
 $\leq 5 \text{ mA (04)}$

Off-State Voltage

200 V ÷ 800 V

- * Logic Level current TRIAC
- * Low thermal resistance with clip bounding
- * Low thermal resistance isolation ceramic for FT....J

This series of TRIACs uses a high performance PNPN technology.

These parts are intended for general purpose AC switching applications with highly inductive loads. The FT....J series provides an isolated tab (rated at 2500 Vrms).

Absolute Maximum Ratings, according to IEC publication No. 134

SYMBOL	PARAMETER	CONDITIONS	Value	Unit
$I_{T(\text{RMS})}$	RMS On-state Current (full sine wave)	All Conduction Angle, $T_C = 100 \text{ }^\circ\text{C}$	8	A
I_{TSM}	Non-repetitive On-State Current	Full Cycle, 60 Hz ($t = 16.7 \text{ ms}$)	84	A
I_{TSM}	Non-repetitive On-State Current	Full Cycle, 50 Hz ($t = 20 \text{ ms}$)	80	A
I^2t	Fusing Current	$t_p = 10 \text{ ms}$, Half Cycle	32	A^2s
I_{GM}	Peak Gate Current	$20 \mu\text{s}$ max. $T_j = 125 \text{ }^\circ\text{C}$	4	A
$P_{G(\text{AV})}$	Average Gate Power Dissipation	$T_j = 125 \text{ }^\circ\text{C}$	1	W
dI/dt	Critical rate of rise of on-state current	$I_G = 2x I_{GT}$, $t_r \leq 100\text{ns}$ $f = 120 \text{ Hz}$, $T_j = 125 \text{ }^\circ\text{C}$	50	$\text{A}/\mu\text{s}$
T_j	Operating Temperature		(-40 + 125)	$^\circ\text{C}$
T_{stg}	Storage Temperature		(-40 + 150)	$^\circ\text{C}$
T_{sld}	Soldering Temperature	10s max	260	$^\circ\text{C}$

SYMBOL	PARAMETER	VOLTAGE				Unit
		B	D	M	N	
V_{DRM} / V_{RRM}	Repetitive Peak Off State Voltage	200	400	600	800	V

INSULATED LOGIC LEVEL TRIAC

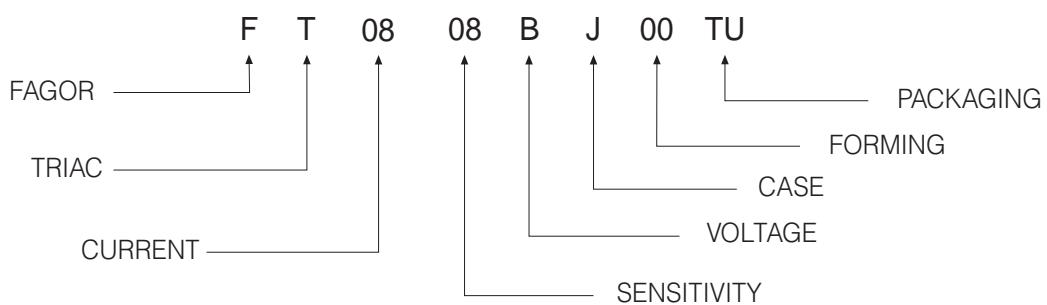
Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	Quadrant	SENSITIVITY		Unit
				04	08	
$I_{GT}^{(1)}$	Gate Trigger Current	$V_D = 12 \text{ V}_{DC}$, $R_L = 33\Omega$, $T_j = 25 \text{ }^\circ\text{C}$	Q1÷Q3	MAX	5	mA
			Q4	MAX	-	mA
V_{GT}	Gate Trigger Voltage	$V_D = 12 \text{ V}_{DC}$, $R_L = 33\Omega$, $T_j = 25 \text{ }^\circ\text{C}$	Q1÷Q3	MAX	1.3	V
			Q1÷Q4	MAX	-	V
V_{GD}	Gate Non Trigger Voltage	$V_D = V_{DRM}$, $R_L = 3.3 \text{ K}\Omega$, $T_j = 125 \text{ }^\circ\text{C}$	Q1÷Q3	MIN	0.2	V
			Q1÷Q4	MIN	0.2	V
$I_H^{(2)}$	Holding Current	$I_T = 100 \text{ mA}$, Gate open, $T_j = 25 \text{ }^\circ\text{C}$		MAX	10	mA
				MAX	15	mA
$dV/dt^{(2)}$	Critical Rate of Voltage Rise	$V_D = 0.67 \times V_{DRM}$, Gate open $T_j = 125 \text{ }^\circ\text{C}$		MIN	20	V/ μ s
				MIN	40	V/ μ s
$(dI/dt)c^{(2)}$	Critical Rate of Current Rise	$(dV/dt)c = 0.1 \text{ V}/\mu\text{s}$ $T_j = 125 \text{ }^\circ\text{C}$ $(dV/dt)c = 10 \text{ V}/\mu\text{s}$ $T_j = 125 \text{ }^\circ\text{C}$		MIN	3.5	A/ms
				MIN	1.5	A/ms
$V_{TM}^{(2)}$	On-state Voltage	$I_T = 11 \text{ Amp}$, $t_p = 380 \mu\text{s}$, $T_j = 25 \text{ }^\circ\text{C}$		MAX	1.55	V
				MAX	0.85	V
$r_d^{(2)}$	Dynamic resistance	$T_j = 125 \text{ }^\circ\text{C}$		MAX	50	$\text{m}\Omega$
				MAX	1	mA
I_{DRM}/I_{RRM}	Off-State Leakage Current	$V_D = V_{DRM}$, $V_R = V_{RRM}$, $T_j = 125 \text{ }^\circ\text{C}$		MAX	5	μA
				MAX	2.5	$^\circ\text{C/W}$
$R_{th(j-c)}$	Thermal Resistance Junction-Case	for AC 360° conduction angle				
$R_{th(j-a)}$	Thermal Resistance Junction-Ambient	$S = 1 \text{ cm}^2$			60	$^\circ\text{C/W}$

(1) Minimum I_{GT} is guaranteed at 5% of I_{GT} max.

(2) For either polarity of electrode MT2 voltage with reference to electrode MT1.

PART NUMBER INFORMATION



INSULATED LOGIC LEVEL TRIAC

Fig. 1: Maximum power dissipation versus RMS on-state current (full cycle).

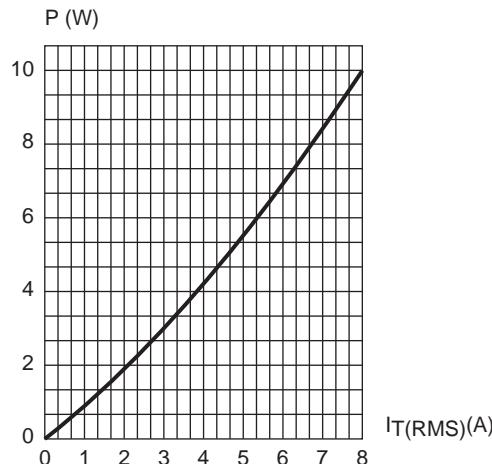


Fig. 2: RMS on-state current versus case temperature (full cycle).

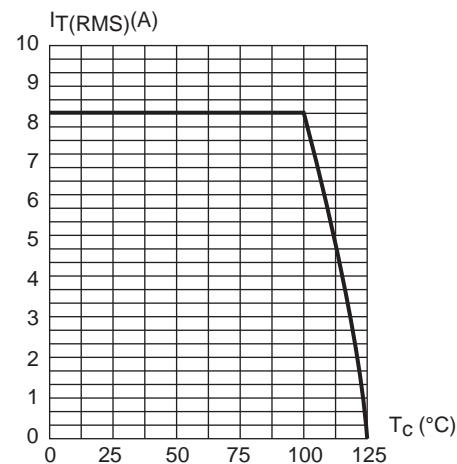


Fig. 3: Relative variation of thermal impedance versus pulse duration.

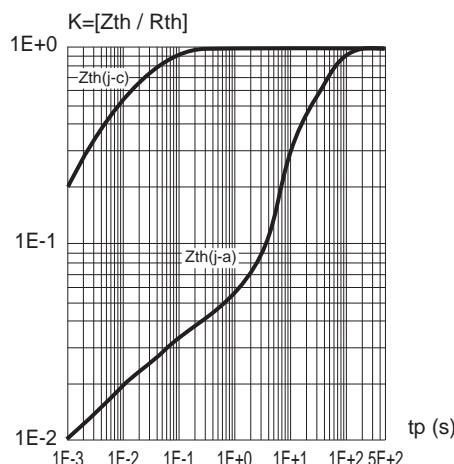


Fig. 5: Surge peak on-state current versus number of cycles

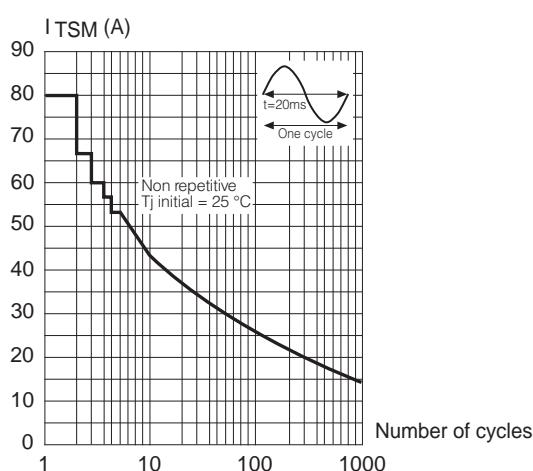


Fig. 4: On-state characteristics (maximum values)

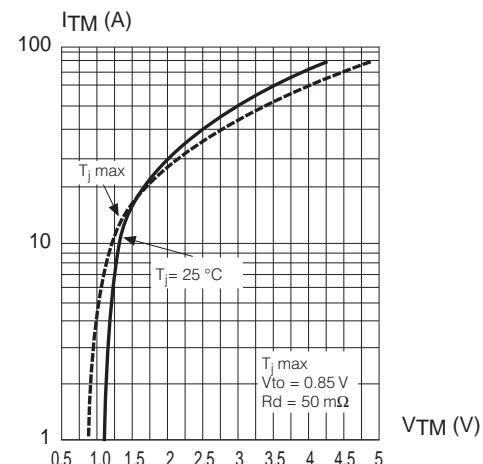
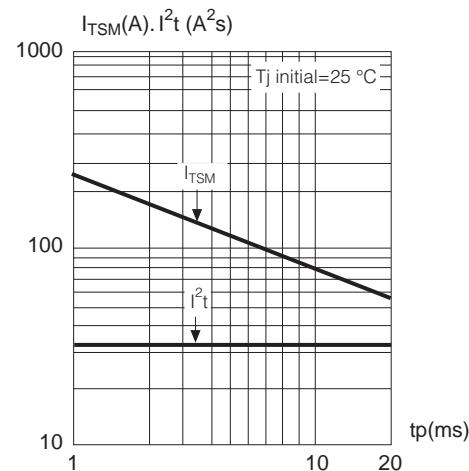


Fig. 6: Non repetitive surge peak on-state current for a sinusoidal pulse with width: $t_p < 10 \text{ ms}$, and corresponding value of I^2t .



INSULATED LOGIC LEVEL TRIAC

Fig. 7: Relative variation of gate trigger current, holding current and latching versus junction temperature (typical values)

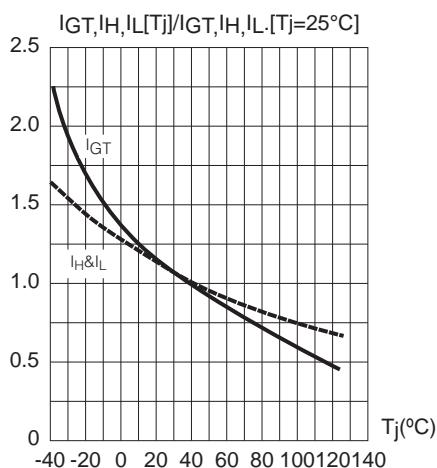


Fig. 8: Relative variation of critical rate of decrease of main current versus junction temperature

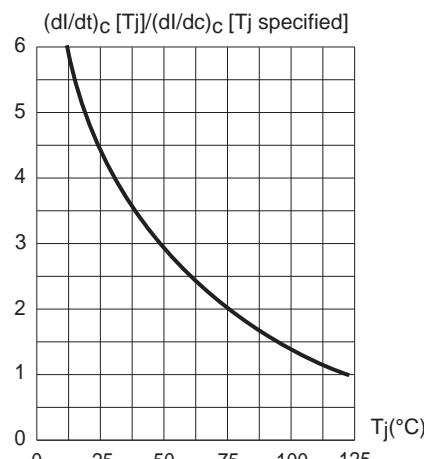
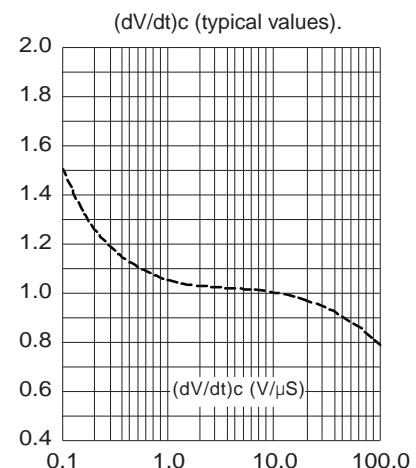
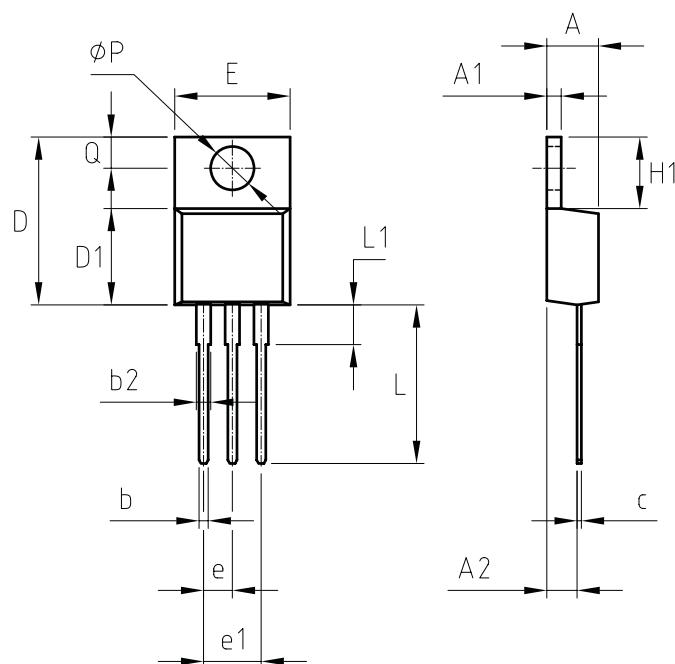


Fig. 9: Relative variation of critical rate of decrease of main current versus



PACKAGE MECHANICAL DATA: INSULATED TO-220AB



REF.	DIMENSIONS	
	Milimeters	
	Min.	Max.
A	3.56	4.83
A1	0.50	1.40
A2	2.00	2.92
b	0.38	1.02
b2	1.14	1.78
c	0.31	0.61
D	14.22	16.51
D1	8.38	9.02
E	9.65	10.67
e	2.49	2.59
e1	5.03	5.18
H1	5.84	6.86
L	12.70	14.74
L1		6.35
P	3.53	4.09
Q	2.54	3.43

Mounting Torque

1 N.m

(*) Limiting values and life support applications, see Web page.