



Features

- Automatic power-down when deselected
- CMOS for optimum speed/power
- High speed
— 12 ns
- Low active power
— 935 mW
- Low standby power
— 220 mW
- TTL-compatible inputs and outputs
- Capable of withstanding greater than 2001V electrostatic discharge

Functional Description

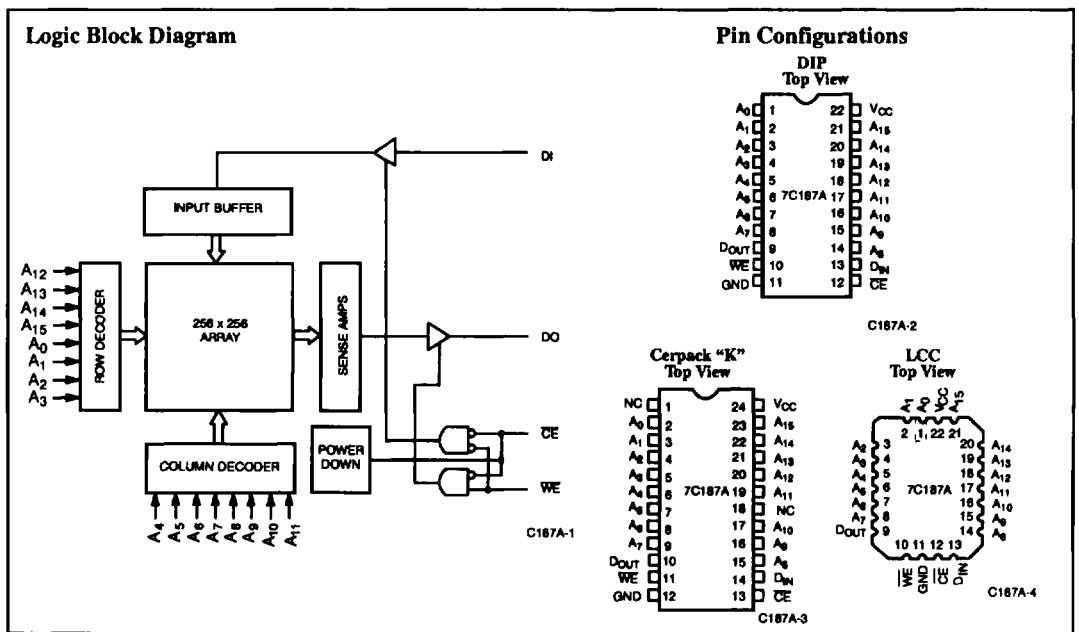
The CY7C187A is a high-performance CMOS static RAM organized as 65,536 words by 1 bit. Easy memory expansion is provided by an active LOW chip enable (CE) and three-state drivers. The CY7C187A has an automatic power-down feature, reducing the power consumption by 50% when deselected.

Writing to the device is accomplished when the chip enable (CE) and write enable (WE) inputs are both LOW. Data on the input pin (DI) is written into the memory location specified on the address pins (A₀ through A₁₅).

Reading the device is accomplished by taking the chip enable (CE) LOW, while write enable (WE) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the data output (DO) pin.

The output pin stays in high-impedance state when chip enable (CE) is HIGH or write enable (WE) is LOW.

The 7C187A utilizes a die coat to insure alpha immunity.



Selection Guide⁽¹⁾

		7C187A-12	7C187A-15	7C187A-20	7C187A-25	7C187A-35	7C187A-45
Maximum Access Time (ns)		12	15	20	25	35	45
Maximum Operating Current (mA)	Military	170	160	90	80	80	80
Maximum Standby Current (mA)	Military	40/20	40/20	40/20	40/20	30/20	30/20

Shaded area contains advanced information.

Note:

1. For commercial specifications, see CY7C187 datasheet.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	- 65°C to +150°C
Ambient Temperature with Power Applied	- 55°C to +125°C
Supply Voltage to Ground Potential (Pin 22 to Pin 11)	- 0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State	- 0.5V to +7.0V
DC Input Voltage	- 3.0V to +7.0V

Output Current into Outputs (Low)	20 mA
Static Discharge Voltage (per MIL-STD-883, Method 3015)	> 2001V
Latch-Up Current	> 200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Military ^[2]	- 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range^[3]

Parameters	Description	Test Conditions	7C187A-12		7C187A-15		7C187A-20		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
V _{OIH}	Output HIGH Voltage	V _{CC} = Min., I _{OIH} = - 4.0 mA	2.4		2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 12.0 mA		0.4		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC}	2.2	V _{CC}	2.2	V _{CC}	V
V _{IL}	Input LOW Voltage ^[4]		- 3.0	0.8	- 3.0	0.8	- 3.0	0.8	V
I _{Ix}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-10	+10	-10	+10	-10	+10	µA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	-10	+10	-10	+10	-10	+10	µA
I _{OS}	Output Short Circuit Current ^[5]	V _{CC} = Max., V _{OUT} = GND		- 350		- 350		- 350	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA		170		160		90	mA
I _{SB1}	Automatic CE Power-Down Current ^[6]	Max. V _{CC} , CE ≥ V _{IH}		40		40		40	mA
I _{SB2}	Automatic CE Power-Down Current ^[6]	Max. V _{CC} , CE ≥ V _{CC} - 0.3V, V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V		20		20		20	mA

Shaded area contains advanced information.

Notes:

- T_A is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.
- V_{IL} min. = -3.0V for pulse durations less than 30 ns.
- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- A pull-up resistor to V_{CC} on the CE input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.

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SRAMS

Electrical Characteristics Over the Operating Range^[3] (continued)

Parameters	Description	Test Conditions	7C187A-25		7C187A-35, 45		Units
			Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC}	2.2	V _{CC}	V
V _{IL}	Input LOW Voltage ^[4]		-3.0	0.8	-3.0	0.8	V
I _{Ix}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-10	+10	-10	+10	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	-10	+10	-10	+10	μA
I _{OS}	Output Short Circuit Current ^[5]	V _{CC} = Max., V _{OUT} = GND		-350		-350	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA		80		80	mA
I _{SB1}	Automatic \overline{CE} Power Down Current ^[6]	Max. V _{CC} , $\overline{CE} \geq V_{IH}$		40		30	mA
I _{SB2}	Automatic \overline{CE} Power Down Current ^[6]	Max. V _{CC} , $\overline{CE} \geq V_{CC} - 0.3V$, V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V		20		20	mA

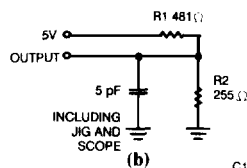
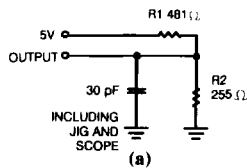
Capacitance^[7]

Parameters	Description	Test Conditions	Max.	Units
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz,	10	pF
C _{OUT}	Output Capacitance	V _{CC} = 5.0V	10	pF

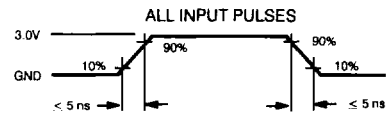
Note:

7. Tested initially and after any design or process changes that may affect these parameters.

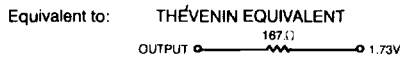
AC Test Loads and Waveforms



C187A-5



C187A-6



Switching Characteristics Over the Operating Range^[3, 8]

Parameters	Description	7C187A-12		7C187A-15		7C187A-20		7C187A-25		7C187A-35		7C187A-45		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE														
t _{RC}	Read Cycle Time	12		15		20		25		35		45		ns
t _{AA}	Address to Data Valid		12		15		20		25		35		45	ns
t _{OHA}	Output Hold from Address Change	3		3		3		3		3		3		ns
t _{ACE}	\overline{CE} LOW to Data Valid		12		15		20		25		35		45	ns
t _{LZCE}	\overline{CE} LOW to Low Z ^[9]	3		3		5		5		5		5		ns
t _{HZCE}	\overline{CE} HIGH to High Z ^[9, 10]		7		8		8		10		15		15	ns
t _{PU}	\overline{CE} LOW to Power-Up	0		0		0		0		0		0		ns
t _{PD}	\overline{CE} HIGH to Power-Down		12		15		20		20		20		25	ns
WRITE CYCLE^[11]														
t _{WC}	Write Cycle Time	12		15		20		20		25		40		ns
t _{SCE}	\overline{CE} LOW to Write End	8		10		15		20		25		30		ns
t _{AW}	Address Set-Up to Write End	8		10		15		20		25		30		ns
t _{HA}	Address Hold from Write End	0		0		0		0		0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		0		0		0		0		ns
t _{PWE}	\overline{WE} Pulse Width	8		10		15		15		20		20		ns
t _{SD}	Data Set-Up to Write End	6		7		10		10		15		15		ns
t _{HD}	Data Hold from Write End	0		0		0		0		0		0		ns
t _{LZWE}	\overline{WE} HIGH to Low Z ^[9]	3		3		5		5		5		5		ns
t _{HZWE}	\overline{WE} LOW to High Z ^[9, 10]		6		7		7		7		10		15	ns

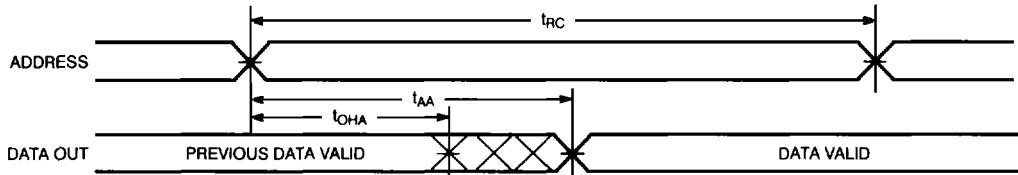
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Notes:

- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device.
- t_{HZCE} and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
- The internal write time of the memory is defined by the overlap of \overline{CE} LOW and \overline{WE} LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

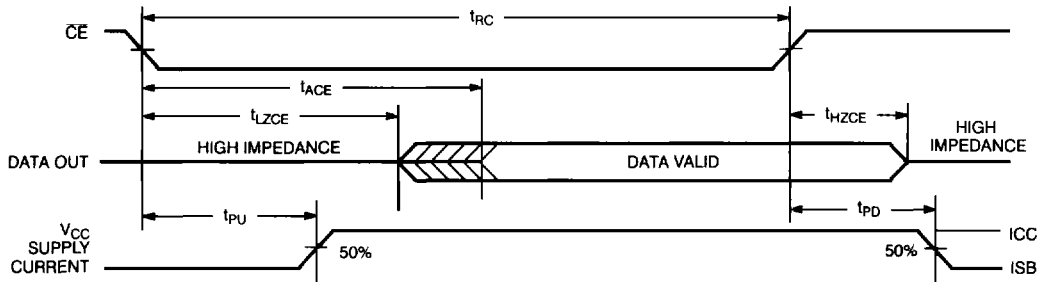
Switching Waveforms

Read Cycle No. 1^[12, 13]



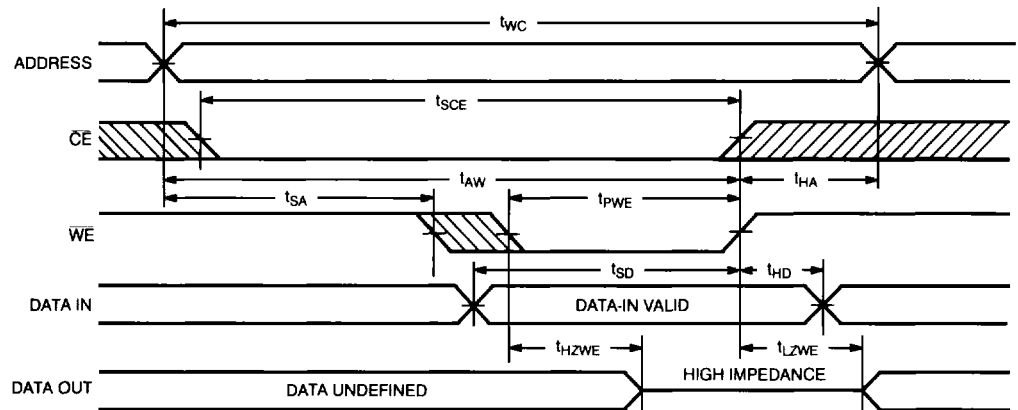
C187A-7

Read Cycle No. 2^[12, 14]



C187A-8

Write Cycle No. 1 (\overline{WE} Controlled)^[11]



C187A-9

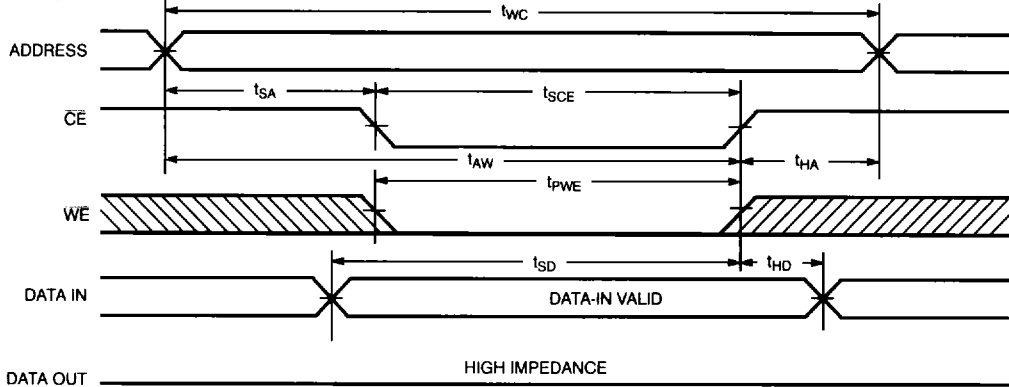
Notes:

12. \overline{WE} is HIGH for read cycle.
13. Device is continuously selected, $\overline{CE} = V_{IL}$.

14. Address valid prior to or coincident with \overline{CE} transition LOW.

Switching Waveforms (continued)

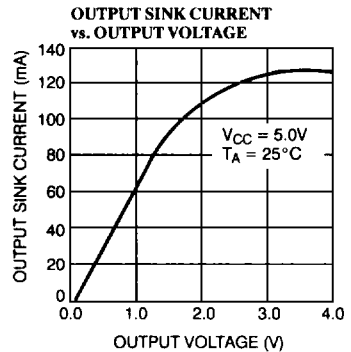
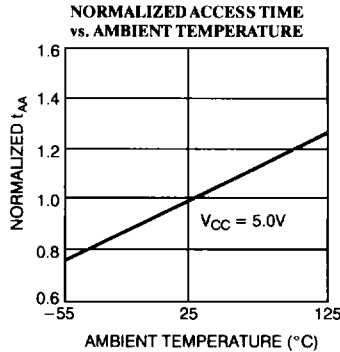
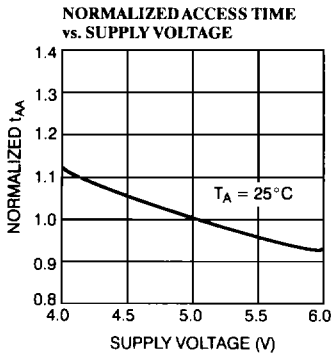
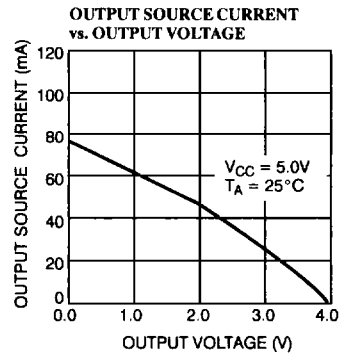
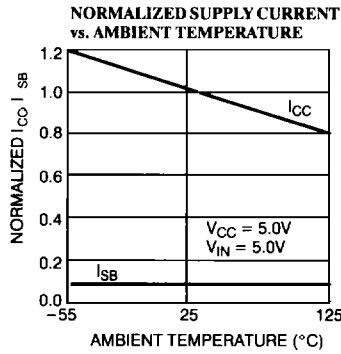
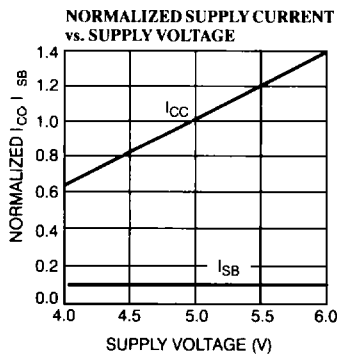
Write Cycle No. 2 (CE Controlled) [11, 15]

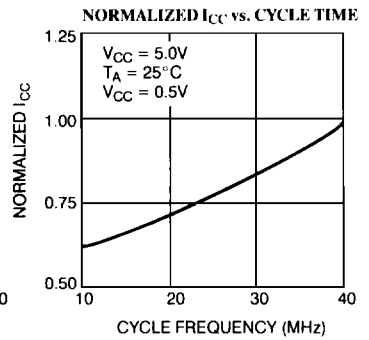
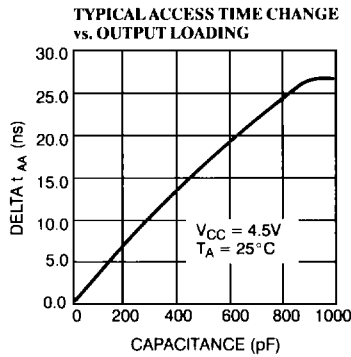
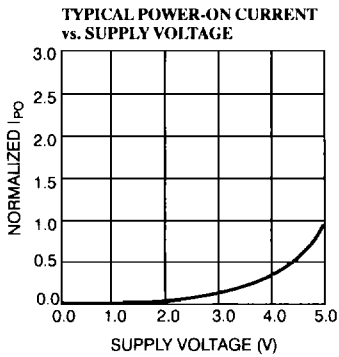


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Note:
15. If \overline{CE} goes HIGH simultaneously with \overline{WE} HIGH, the output remains in a high-impedance state.

Typical DC and AC Characteristics



Typical DC and AC Characteristics (continued)

Address Designators

Address Name	Address Function	Pin Number
A0	X3	1
A1	X4	2
A2	X5	3
A3	X6	4
A4	X7	5
A5	Y7	6
A6	Y6	7
A7	Y2	8
A8	Y3	14
A9	Y1	15
A10	Y0	16
A11	Y4	17
A12	Y5	18
A13	X0	19
A14	X1	20
A15	X2	21

Truth Table

CE	WE	Inputs/Outputs	Mode
H	X	High Z	Deselect/Power-Down
L	H	Data Out	Read
L	L	Data In	Write

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
12	CY7C187A-12DMB	D10	Military
	CY7C187A-12KMB	K73	
	CY7C187A-12LMB	L52	
15	CY7C187A-15DMB	D10	Military
	CY7C187A-15KMB	K73	
	CY7C187A-15LMB	L52	
20	CY7C187A-20DMB	D10	Military
	CY7C187A-20KMB	K73	
	CY7C187A-20LMB	L52	
25	CY7C187A-25DMB	D10	Military
	CY7C187A-25KMB	K73	
	CY7C187A-25LMB	L52	
35	CY7C187A-35DMB	D10	Military
	CY7C187A-35KMB	K73	
	CY7C187A-35LMB	L52	
45	CY7C187A-45DMB	D10	Military
	CY7C187A-45KMB	K73	
	CY7C187A-45LMB	L52	

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MILITARY SPECIFICATIONS
Group A Subgroup Testing
DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
$V_{IL Max.}$	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{OS}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

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