FEATURES

- 72-pin industry standard 4-byte single-in-line memory module
- JEDEC compliant: 21-C, Fig. 4-18 A,B, Fig 4-6 (Release 6); No.95 MO-116
- Supports 90°, 40° and 22.5° connectors
- High performance, CMOS
- Single 5V ± 10% power supply
- TTL-compatible inputs and outputs
- FAST PAGE MODE access cycle
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, HIDDEN
- Refresh: 2048 refresh cycles every 32 ms
- Dimensions: 4.25" (length) x 1.00" (height) x 0.360" (max thickness)

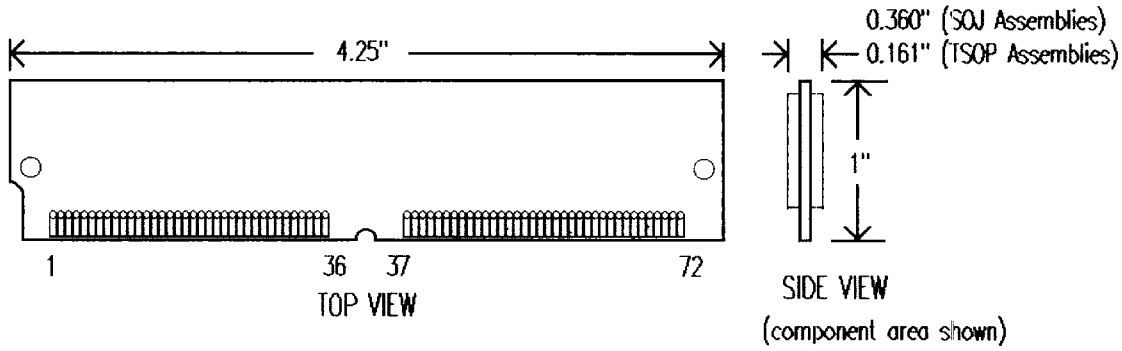
PERFORMANCE RANGE

SYMBOL	PARAMETER	Rating	
		60 ns	70 ns
t_{RAC}	$\overline{RAS}$ Access Time	60 ns (max)	70 ns (max)
t_{CAC}	$\overline{CAS}$ Access Time	15 ns (max)	20 ns (max)
t_{AA}	Access Time from Column Address	30 ns (max)	35 ns (max)
t_{RC}	Random Read or Write Cycle Time	110 ns (min)	130 ns (min)
t_{PC}	Fast Page Mode Cycle Time	40 ns (min)	45 ns (min)

ORDERING INFORMATION

DESCRIPTION	PART NUMBER	ENGINEERING DESCRIPTOR
8M x 32, 60 ns, Gold Tabs, SOJ	20022C	CL001E08320B0DJ-60
8M x 32, 60 ns, Gold Tabs, TSOP	20603C	CL001E08320B0DT-60
8M x 32, 60 ns, Tin/Lead Tabs, SOJ	14864C	CL001D08320B0DJ-60
8M x 32, 60 ns, Tin/Lead Tabs, TSOP	20604C	CL001D08320B0DT-60
8M x 32, 70 ns, Gold Tabs, SOJ	20004C	CL001E08320B0DJ-70
8M x 32, 70 ns, Gold Tabs, TSOP	20605C	CL001E08320B0DT-70
8M x 32, 70 ns, Tin/Lead Tabs, SOJ	4779C	CL001D08320B0DJ-70
8M x 32, 70 ns, Tin/Lead Tabs, TSOP	20606C	CL001D08320B0DT-70
8M x 32, 60 ns, Gold Tabs, SOJ	20092C	CL001E08320B0EJ-60
8M x 32, 60 ns, Tin/Lead Tabs, SOJ	20093C	CL001D08320B0EJ-60
8M x 32, 70 ns, Gold Tabs, SOJ	20094C	CL001E08320B0EJ-70
8M x 32, 70 ns, Tin/Lead Tabs, SOJ	20095C	CL001D08320B0EJ-70

CARD OUTLINE



GENERAL DESCRIPTION

The 8M x 32 SIMM uses dynamic RAM devices and is designed for use as a general-purpose 4-byte wide memory assembly with 8 data bits per byte. The SIMM is populated with sixteen 4M x 4 DRAMs.

Presence Detect (PD) bits provide information about SIMM density, addressing, performance and features.

During Read or Write Cycles, each byte may be uniquely addressed via 22 address bits, with the first eleven bits (A0~A10) latched on $\overline{RAS}$ and the latter eleven bits (A0~A10) latched on $\overline{CAS}$. READ or WRITE cycles are selected with the $\overline{WE}$ input, with a logic low indicating a WRITE cycle and a logic HIGH indicating a READ cycle. During a WRITE cycle, data-in is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last.

FAST PAGE MODE operation allows for faster READs or WRITEs within a row-address-defined page boundary. A FAST PAGE MODE cycle is initiated with $\overline{RAS}$ followed by $\overline{CAS}$, then strobing $\overline{CAS}$ to latch different column addresses while holding $\overline{RAS}$ LOW.

Returning $\overline{RAS}$ and $\overline{CAS}$ high terminates a memory cycle and returns the DRAMs to a reduced-current STANDBY state.

Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE) or $\overline{RAS}$ refresh cycle ($\overline{RAS}$-ONLY, CBR, or HIDDEN) so that all 2048 combinations of $\overline{RAS}$ addresses (A0~A10) are executed at least every 32 ms. The CBR refresh and HIDDEN refresh cycles will invoke the on-chip refresh address counters for automatic $\overline{RAS}$ addressing.

PIN DESCRIPTION

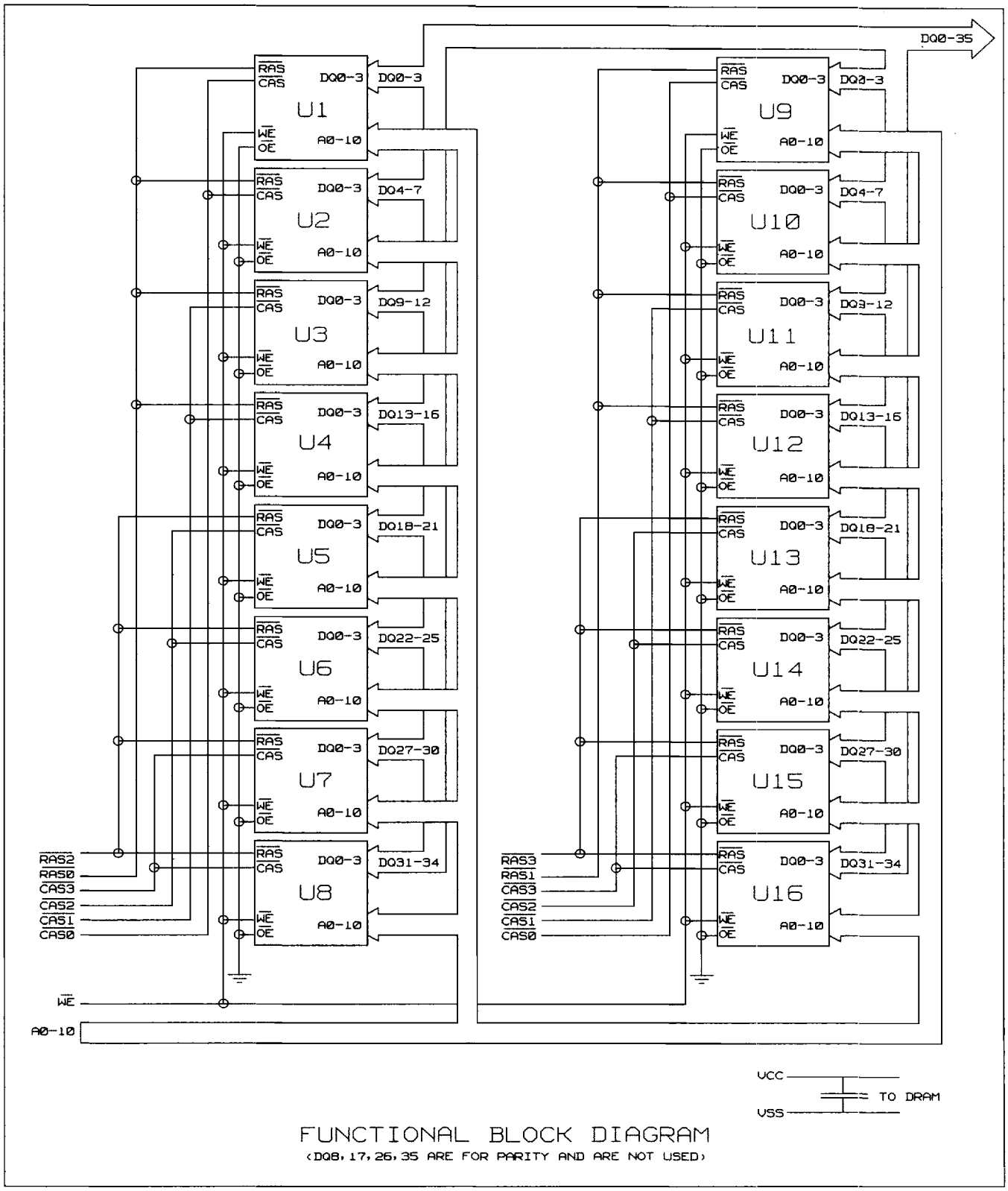
$\overline{RAS0}$~$\overline{RAS3}$	Row Address Strobe
$\overline{CAS0}$~$\overline{CAS3}$	Column Address Strobe
$\overline{WE}$	Write Enable
A0~A10	Address Inputs
DQ0~7,DQ9~16, DQ18~25,DQ27~34	Data In/Out
VCC	Power (+5.0V)
VSS	Ground
NC	No Connection
PD1~4	Presence Detects

PRESENCE DETECT

PIN SYMBOL	CONFIGURATION	
	60 ns	70 ns
PD1	NC	NC
PD2	VSS	VSS
PD3	NC	VSS
PD4	NC	NC

PIN CONFIGURATION

#	Name	#	Name	#	Name	#	Name	#	Name	#	Name
1	VSS	13	A1	25	DQ24	37	NC	49	DQ9	61	DQ14
2	DQ0	14	A2	26	DQ7	38	NC	50	DQ27	62	DQ33
3	DQ18	15	A3	27	DQ25	39	VSS	51	DQ10	63	DQ15
4	DQ1	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ28	64	DQ34
5	DQ19	17	A5	29	NC	41	$\overline{CAS2}$	53	DQ11	65	DQ16
6	DQ2	18	A6	30	VCC	42	$\overline{CAS3}$	54	DQ29	66	NC
7	DQ20	19	A10	31	A8	43	$\overline{CAS1}$	55	DQ12	67	PD1
8	DQ3	20	DQ4	32	A9	44	$\overline{RAS0}$	56	DQ30	68	PD2
9	DQ21	21	DQ22	33	$\overline{RAS3}$	45	$\overline{RAS1}$	57	DQ13	69	PD3
10	VCC	22	DQ5	34	$\overline{RAS2}$	46	NC	58	DQ31	70	PD4
11	NC	23	DQ23	35	NC	47	$\overline{WE}$	59	VCC	71	NC
12	A0	24	DQ6	36	NC	48	NC	60	DQ32	72	VSS



FUNCTIONAL BLOCK DIAGRAM

(DQ8, 17, 26, 35 ARE FOR PARITY AND ARE NOT USED)

TRUTH TABLE

FUNCTION		RAS	CAS	WE	ROW ADDR	COL ADDR	DATA IN/OUT
Standby		H	H→X	X	X	X	Hi-Z
Read		L	L	H	ROW	COL	Valid D_{OUT}
Early-Write		L	L	L	ROW	COL	Valid D_{IN}
Fast Page Mode-Read	1st Cycle	L	H→L	H	ROW	COL	Valid D_{OUT}
	2nd Cycle	L	H→L	H	N/A	COL	Valid D_{OUT}
Fast Page Mode-Write	1st Cycle	L	H→L	L	ROW	COL	Valid D_{IN}
	2nd Cycle	L	H→L	L	N/A	COL	Valid D_{IN}
RAS-Only Refresh		L	H	X	ROW	N/A	Hi-Z
Hidden Refresh	Read	L→H→L	L	H	ROW	COL	Valid D_{OUT}
	Write	L→H→L	L	L	ROW	COL	Valid D_{IN}
CAS-Before-RAS Refresh		H→L	L	H	X	X	Hi-Z

X:"H" or "L" D_{IN}:Data In D_{OUT}:Data Out Hi-Z:High Impedance N/A:Not Applicable

ABSOLUTE MAXIMUM RATINGS (Note 1,22)

SYMBOL	PARAMETER	RATING	UNITS	NOTES
V_{CC}	Power Supply Voltage	-1.0 to 7.0	V	2
V_{IN}	Voltage on any Pin Relative to V_{SS}	-1.0 to 7.0	V	2
V_{OUT}		-1.0 to 7.0	V	2
T_{opr}	Operating Temperature	0 to 70	°C	
T_{stg}	Storage Temperature	-55 to 125	°C	
P_D	Power Dissipation	16.0	W	17,31
I_{OS}	Short Circuit Output Current	50	mA	17

RECOMMENDED OPERATING CONDITIONS (T_A= 0 to 70 °C) (Note 2)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Ground	0	0	0	V	
V_{IH}	Input High Voltage	2.4	-	V_{CC}+1.0	V	22
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	22

T_A: Ambient temperature

CAPACITANCE (f = 1 MHz; T_A = 25 °C) (Note 22)

SYMBOL	PARAMETER	MAX.	UNITS	NOTES
C_{I1}	Input Capacitance (A0-A10)	96	pF	
C_{I2}	Input Capacitance ($\overline{RAS0}$~$\overline{RAS3}$)	28	pF	
C_{I3}	Input Capacitance ($\overline{CAS0}$~$\overline{CAS3}$)	28	pF	
C_{I4}	Input Capacitance ($\overline{WE}$)	112	pF	
C_{O1}	Output Capacitance (Data In/Out)	14	pF	

T_A: Ambient temperature

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) (Note 18,22)

SYMBOL	PARAMETER	SPEED	MIN.	MAX.	NOTES
I_{CC1}	OPERATING CURRENT: Average Power Supply Operating Current ($\overline{RAS}$,$\overline{CAS}$, Address Cycling@t_{RC} = $t_{RC(min)}$,V_{CC} = $V_{CC\ (max)}$) (mA)	60 ns	-	896	3,4,5,6,16
		70 ns	-	816	
I_{CC2}	STANDBY CURRENT (TTL): Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=Vcc, Data out is disabled (Hi-Z), all other inputs =Vcc, V_{CC} =$V_{CC\ (max)}$) (mA)	Don't Care	-	32	
I_{CC3}	$\overline{RAS}$-ONLY REFRESH CURRENT: Average Power Supply Current, $\overline{RAS}$-Only Mode ($\overline{RAS}$, Address Cycling, $\overline{CAS}$=V_{IH}@t_{RC}=$t_{RC(min)}$,V_{CC}=$V_{CC(max)}$) (mA)	60 ns	-	1760	3,4,5,6,16, 31
		70 ns	-	1600	
I_{CC4}	FAST PAGE MODE CURRENT: Average Power Supply Current, FPM ($\overline{RAS}$=V_{IL},$\overline{CAS}$, Address Cycling@ t_{PC}=$t_{PC(min)}$,V_{CC}=$V_{CC(max)}$) (mA)	60 ns	-	656	3,4,5,7,16
		70 ns	-	576	
I_{CC5}	STANDBY CURRENT (CMOS): Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V, Data Out is disabled (Hi-Z),V_{CC} = $V_{CC(max)}$) (mA)	Don't Care	-	16	
I_{CC6}	$\overline{CAS}$-BEFORE-$\overline{RAS}$, REFRESH CURRENT: Average Power Supply Current, $\overline{CAS}$-Before-$\overline{RAS}$ Mode ($\overline{RAS}$,$\overline{CAS}$ Cycling@t_{RC}=$t_{RC(min)}$, V_{CC} = $V_{CC(max)}$)(mA)	60 ns	-	1760	3,4,5,6,16, 31
		70 ns	-	1600	
I_{LI}	INPUT LEAKAGE CURRENT: Input Leakage Current, any input (0≤V_{IN}≤V_{cc}, all other pins not under test=0V, $V_{CC=}$ $V_{CC(max)}$) (µA)	**A0~A10, $\overline{WE}$**	-160	160	
		$\overline{RAS0}$~$\overline{RAS3}$	-40	40	
		$\overline{CAS0}$~$\overline{CAS3}$	-40	40	
I_{LO}	OUTPUT LEAKAGE CURRENT: (Data Out is disabled (Hi-Z), 0≤V_{OUT}≤V_{CC})(µA)		-20	20	
V_{OH}	OUTPUT HIGH LEVEL: Output "H" Level Voltage (I_{OUT}=-5mA) (V)		2.4	-	2
V_{OL}	OUTPUT LOW LEVEL: Output "L" Level Voltage (I_{OUT}=+4.2mA) (V)		-	0.4	2

AC CHARACTERISTICS
READ, WRITE, AND REFRESH CYCLES (COMMON PARAMETERS)
(Recommended operating conditions unless otherwise noted.) (Note 8,18)

SYMBOL	PARAMETER	60 ns		70 ns		NOTES
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Random READ or WRITE Cycle Time (ns)	110	-	130	-	
t_{RP}	$\overline{RAS}$ Precharge Time (ns)	40	-	50	-	
t_{CP}	$\overline{CAS}$ Precharge Time (ns)	10	-	10	-	
t_{RAS}	$\overline{RAS}$ Pulse Width (ns)	60	10000	70	10000	23
t_{CAS}	$\overline{CAS}$ Pulse Width (ns)	15	10000	20	10000	23
t_{ASR}	Row Address Setup Time (ns)	0	-	0	-	22
t_{RAH}	Row Address Hold Time (ns)	10	-	10	-	
t_{ASC}	Column Address Setup Time (ns)	0	-	0	-	22
t_{CAH}	Column Address Hold Time (ns)	10	-	15	-	22
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time (ns)	20	45	20	50	10
t_{RAD}	$\overline{RAS}$ to Col. Address Delay Time (ns)	15	30	15	35	15,23
t_{RSH}	$\overline{RAS}$ Hold Time (ns)	15	-	20	-	22
t_{CSH}	$\overline{CAS}$ Hold Time (ns)	60	-	70	-	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time (ns)	5	-	5	-	22
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ hold Time (ns)	5	-	5	-	22
t_T	Transition Time (Rise and Fall) (ns)	3	30	3	30	22
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$ (ns)	-	-	-	-	

READ CYCLES (Note 8,18)

SYMBOL	PARAMETER	60 ns		70 ns		NOTES
		MIN.	MAX.	MIN.	MAX.	
t_{RAC}	Access Time from $\overline{RAS}$ (ns)	-	60	-	70	9,10,15,30
t_{CAC}	Access Time from $\overline{CAS}$ (ns)	-	15	-	20	9,10,30
t_{AA}	Access Time from Address (ns)	-	30	-	35	9,15,30
t_{RCS}	Read Command Setup Time (ns)	0	-	0	-	22
t_{RCH}	Read Command Hold Time to $\overline{CAS}$ (ns)	0	-	0	-	14,22
t_{RRH}	Read Command Hold Time to $\overline{RAS}$ (ns)	0	-	0	-	14,22
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time(ns)	30	-	35	-	22
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z (ns)	0	-	0	-	9,22
t_{DZC}	Data to $\overline{CAS}$ Low Delay Time (ns)	-	-	-	-	
t_{CDD}	$\overline{CAS}$ High to Data Delay Time (ns)	15	-	18	-	27
t_{OFF}	Output Buffer Turn-Off Delay (ns)	0	15	0	20	12,24

WRITE CYCLES (Note 8,18)

SYMBOL	PARAMETER	60 ns		70 ns		NOTES
		MIN.	MAX.	MIN.	MAX.	
t_{WCS}	Write Command Set Up Time (ns)	0	-	0	-	13
t_{WCH}	Write Command Hold Time (ns)	10	-	15	-	
t_{WP}	Write Command Pulse Width (ns)	10	-	15	-	22
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time (ns)	15	-	20	-	22
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time (ns)	15	-	20	-	22
t_{DS}	D_{IN} Setup Time (ns)	0	-	0	-	25
t_{DH}	D_{IN} Hold Time (ns)	10	-	15	-	22,25
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$ (ns)	-	-	-	-	
t_{DHR}	Data in Hold Time Referenced to $\overline{RAS}$ (ns)	-	-	-	-	

FAST PAGE MODE CYCLES (Note 8,18)

SYMBOL	PARAMETER	60 ns		70 ns		NOTES
		MIN.	MAX.	MIN.	MAX.	
t_{PC}	Fast Page Mode Cycle Time (ns)	40	-	45	-	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width (ns)	60	100000	70	100000	22
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge (ns)	35	-	40	-	22
t_{CPA}	Access Time from $\overline{CAS}$ Precharge (ns)	-	35	-	40	21,22
t_{CPW}	$\overline{WE}$ Delay Time From $\overline{CAS}$ Precharge (ns)	60	-	70	-	

REFRESH CYCLE (Note 8,18)

SYMBOL	PARAMETER	60 ns		70 ns		NOTES
		MIN.	MAX.	MIN.	MAX.	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle) (ns)	10	-	15	-	22
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle) (ns)	5	-	5	-	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle) (ns)	10	-	10	-	22
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle) (ns)	10	-	10	-	22
t_{REF}	Refresh Period (2048 cycles) (ms)	-	32	-	32	

NOTES

1. Permanent damage to the device may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. All voltages referenced to V_{SS}.

3. I_{CC} is specified as an average current.

4. This parameter depends on output loading and/or cycle rates.

5. Specified values are obtained with the output open.

6. Address can be changed a maximum of once while $\overline{RAS}=V_{IL}$.

7. Address can be changed a maximum of once while $\overline{CAS}=V_{IH}$.

8. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition time (t_T) is measured between $V_{IH(min)}$ and $V_{IL(max)}$, and is assumed to be 5ns for all inputs. All input signals must transit between V_{IH} and V_{IL} (or V_{IL} and V_{IH}) without slope reversal.

9. Measured with a load equivalent to 2 TTL loads and 100pF.

10. Operation within the $t_{RCD(max)}$ limit ensures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.

11. Assumes that $t_{RCD} \geq t_{RCD(max)}$, $t_{RAD} \leq t_{RAD(max)}$.

12. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

13. This is a non-restrictive operating parameter. It is included in the data sheet as an electrical characteristic only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data out pins will remain high impedance (open circuit) for the duration of the cycle. If the above condition is not satisfied, the condition of the data out (at access time) is indeterminate.

14. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

15. Operation within the $t_{RAD(max)}$ limit ensures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled exclusively by t_{AA}.

16. Specified values are obtained with minimum cycle time.

17. Specified values are obtained with $T_A=25°C$.

18. An initial pause of 200µs is required after power-up followed by a minimum of eight initialization cycles (any 8 $\overline{CAS}$-before-$\overline{RAS}$ or $\overline{RAS}$-only Refresh cycles with $\overline{WE}$ high) before proper device operation is assured. Also, any 8 $\overline{CAS}$-before-$\overline{RAS}$ or $\overline{RAS}$-only Refresh cycles with $\overline{WE}$ high are required after prolonged periods (greater than t_{REF}) of $\overline{RAS}$ inactivity before proper device operation is assured.

19. Measured with a load equivalent to 50pF and 500 ohms.

20. Write cycle is applicable instead of read cycle. Timing requirements for $\overline{RAS}$,$\overline{CAS}$ and Address are the same for Hidden Refresh Write Cycle as that shown for Hidden Refresh Read Cycle. $\overline{WE}$, D_{IN} and D_{OUT} for Hidden Refresh Write Cycle are the same as for Write Cycle.

21. t_{CPA} is access time from $\overline{CAS}$ precharge (that is caused by changing $\overline{CAS}$ from "L" to "H"). Therefore, if t_{CP} is long, then t_{CPA} is longer than $t_{CPA(max)}$.

22. Calculated based on data supplied by the DRAM manufacturer(s).

23. Maximum value is calculated based on data supplied by the DRAM manufacturer(s).

24. Minimum value is calculated based on data supplied by the DRAM manufacturer(s).

25. This parameter is referenced to the $\overline{CAS}$ leading edge in Early Write cycles and to the $\overline{WE}$ leading edge in Read-Modify-Write cycles.

26. V_{IN} = 0 Volt.

27. Either t_{CDD} or t_{ODD} must be satisfied.

28. Either t_{DZC} or t_{DZO} must be satisfied.

29. $t_{RASP(MIN)}$ is specified as two cycles of $\overline{CAS}$ input are performed.

30. The access time is limited by all four parameters t_{RAC}, t_{CAC}, t_{AA}, t_{CPA}.

31. This assumes all $\overline{RAS}$ (and all $\overline{CAS}$ for CBR refresh) are active.

For Timing Diagrams see **"FPM Timing Diagrams"** (Document No. **20432C**).

Available from fax-on-demand and Website: **http://www.celestica.com/memory/**

Celestica Inc. 1996
Contact Information
For further information on this product, please call:

Celestica 1-888-889-9998

The information provided is believed to be accurate and reliable. Celestica reserves the right to make changes to this document and to the product described without notice. No liability is assumed as a result of its use nor for any infringement on the rights of others.

TM Celestica is a trademark of Celestica, Inc.

August 13, 1996