

#### **FEATURES**

- Small 14 pin SOIC/DIP package
- Supports 3.3V and 5V operation and Pentium™ processor
- Up to three output clocks available
- **W**42C26-01 provides: Selectable CPU clock 14.3 MHz system clock 7.2 MHz keyboard clock
- /STOPCPU input pin instantly starts and stops CPU clock glitch free
- /SLOWCPU input pin smoothly slows CPU clock to 8 MHz
- Customizable with single metal layer change
- Up to 16 selectable frequencies
- Smooth, glitch-free frequency transition
- TTL or CMOS input level compatible
- Integral loop filter components
- High performance, low power CMOS

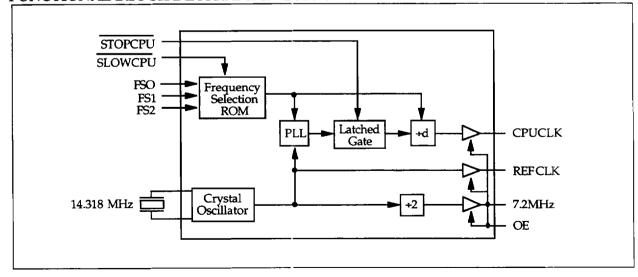
#### FUNCTIONAL DESCRIPTION

The **w**42C26 provides a low cost solution for generating up to three simultaneous clock frequencies. It is ideal for CPU motherboard or portable applications.

The **W**42C26 incorporates an improved crystal oscillator circuit that provides excellent REFCLK duty cycle, jitter characteristics and frequency accuracy. On chip PLL loop filter components ensure excellent CPU clock stability, even with the noise typical of a digital system. Device functionality, including input/output options and frequency selection, is determined by a single metal mask that allows quick-turn customization capability. Both 3.3 volt and 5 volt VCC operation is supported. Smooth frequency transitions are provided between selected output frequencies.

The standard **w**42C26-01 and **w**42C26-14 options are designed for x86 based motherboards. They include CPU clock slow and stop functions for green PC implementation. The **w**42C26-16 is designed for NexGen based systems. The **w**42C26-15 is a general purpose clock device.

#### FUNCTIONAL BLOCK DIAGRAM: w42C26-01



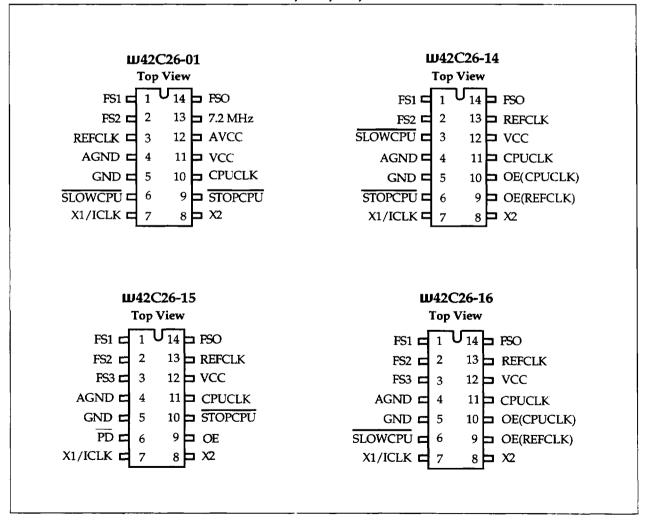
# IMPROVED CRYSTAL OSCILLATOR CIRCUIT

The w42C26 incorporates a crystal oscillator circuit designed to provide 50% duty cycle over a range of operating conditions including the addition of external crystal load capacitors to pins X1 and X2. (Crystal load capacitance is sometimes increased to match a particular crystal load requirement when absolute frequency accuracy is important.) Duty

cycle is also maintained when using an external clock source (connected to pin X1, pin X2 is left open), as long as the external clock has good duty cycle.

Crystal load capacitance of the w42C26 is about 12pf, which is becoming an industry standard. This helps to control frequency accuracy, assuming that a crystal which specifies a 12pf load condition is used. The circuit exhibits about 50% less clock jitter from the REFCLK output when compared to similar devices.

## PIN CONFIGURATIONS: w42C26-01, -14, -15, and -16



FREQUENCY SELECTION FOR w42C26 (using 14.318 MHz input)

Select Address	-01	-14	-15	-16
FS3-FS0	CPUOUT	CPUOUT	CPUOUT	CPUOUT
	(MHz)	(MHz)	(MHz)	(MHz)
0	25	25	14.318	30
1	66.6	33.3	14.75	31
2	60	40	15.288	33.3
3	50	50	17.496	34.5
4	80	66.6	19.0	35
5	40	60	19.5	35.5
6	33.3	80	21.0	36
7	<i>7</i> 5	50	22.0	37.5
8	-	-	24.0	38.5
9	-	-	40.0	40
Α	-	-	41.0	42
В	-	-	42.0	43.5
С		-	43.0	45
D	-	_	44.0	<b>46.</b> 5
E	-	~	45.0	48.5
F			<b>46.</b> 0	50.0

# PIN DESCRIPTIONS: w42C26-01

Input Selection	Input/ Output	Function	
7.2 MHz	0	7.2 MHz output clock for use in keyboard applications (REFCLK + 2)	
AGND	-	Analog ground connection	
AVCC	-	Analog power supply connection	
CPUCLK	0	CPU Clock output (refer to Frequency Selection Table)	
FS0	I	Frequency Selection input, LSB (1)	
FS1	I	Frequency Selection input (1)	
FS2	I	Frequency Selection input, MSB (1)	
GND	-	Ground connection	
OE(REFCLK)	I	REFCLK Output Enable, puts REFCLK output in high impedance state when low (Note 1)	
OE(CPUCLK)	I	CPUCLK Output Enable, puts CPUCLK output in high impedance state when low (Note 1)	
REFCLK	0	Reference Clock output, outputs crystal or input clock frequency (14.318 MHz)	
SLOWCPU	I	Slow CPU input. Slows CPUCLK output to 8 MHz when low (1)	
STOPCPU	I	Stop CPU input. When /STOPCPU is brought low, CPUCLK stops low (within a few CPUCLK clock cycles) without clock glitches or short output cycles. Likewise, when /STOPCPU is brought high, CPUCLK resumes to the selected frequency (again within a few CPUCLK clocks; the internal VCO is not stopped) without glitches. (1)	
VCC	-	Power supply connection	
X1/ICLK	I	Crystal connection or external clock frequency input (14.318 MHz)	
X2	0	Crystal connection, leave this pin unconnected when using external clock	

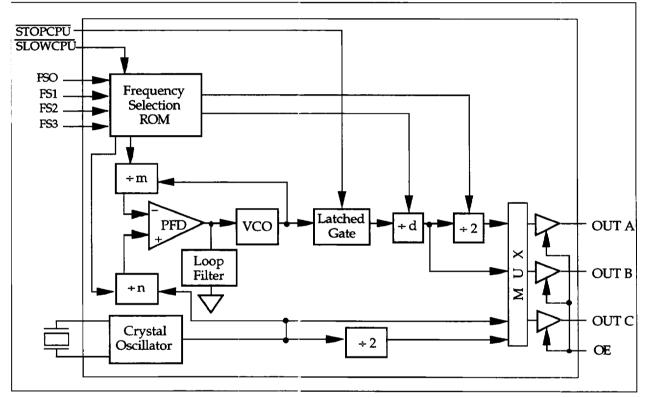
**Note 1:** All inputs, except for X1/ICLK, have an internal pull-up resistor. Unconnected inputs will assume a logic high condition.

## **ш42C26 CUSTOMIZATION**

Like other IC WORKS clock generator devices, the  $\mathbf{w}$ 42C26 is mask customizable to fit individual needs. Customizable features include frequency

selection and various input and output functions. Please contact IC WORKS for further information.

# FUNCTIONAL BLOCK DIAGRAM: w42C26 BASE FEATURE SET



# ABSOLUTE MAXIMUM RATINGS (Note 1)

Parameter	Symbol	Rating	Unit
Voltage on Any Pin with Respect to Ground	VCCVIN	-0.5 to 7.0	V
Storage Temperature	T <sub>STG</sub>	-65 to +150	℃
Ambient Temperature Under Bias	TB	-55 to +125	℃
Operating Temperature	$T_A$	0 to +70	°C

**Note 1:** Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

#### **ELECTRICAL CHARACTERISTICS AT 5.0V**

# DC ELECTRICAL CHARACTERISTICS (0°C $\leq$ T<sub>A</sub> $\leq$ 70°C, V<sub>CC</sub> = 5 V $\pm$ 10 %)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current	I <sub>CC</sub>	Note 2		25	30	mA
Input Low Voltage	$V_{IL}$	$V_{CC} = 5V$			0.8	V
Input High Voltage	$v_{IH}$	$V_{CC} = 5V$	2.0			V
Output Low Voltage	V <sub>OL</sub>	$I_{OL} = 8 \text{ mA}$			0.4	V
Output High Voltage	VOH	$I_{OH} = -1 \text{ InA}$	Vcc4V			
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -4 mA	2.4			V
Input Capacitance	CI	Except X1, X2			10	рF
Load Capacitance	$c_L$	Pins X1, X2		12		рF
Input Low Current	IIL	VIN = 0V (incls pull-up resistor)			-100	μΑ
Input High Current	IIH	$V_{IN} = V_{CC}$			10	μΑ
Input Pull-Up Resistor	Rp	VIN = 0V		250		kΩ

Note 2: W42C26-01 with no load, with 14.318 MHz crystal input, and CPUCLK running at 40 MHz. Power supply current varies with frequency.

#### AC CHARACTERISTICS (0°C $\leq$ T<sub>A</sub> $\leq$ 70°C, V<sub>CC</sub> = 5V $\pm$ 10 %)

Parameter	Symbol	Min	Тур	Max	Unit
Output Frequency	FO	2	<u> </u>	120	MHz
Input Frequency	FI	2	14.318	32	MHz
Output Rise Time, 0.8 to 2.0V, 25pF Load	$T_{R}$		1	2	ns
Output Rise Time, 20 to 80% V <sub>CC</sub> , 25pF Load	$T_{\mathbf{R}}$		2	4	ns
Output Fall Time, 2.0 to 0.8V, 25pF Load	$T_{F}$		1	2	ns
Fall Time, 80 to 20% V <sub>CC</sub> , 25pF Load	TF		2	4	ns
Duty Cycle, 15pF Load	DT	<b>4</b> 0	50	60	%
Jitter, 1 Sigma, All Frequencies	T <sub>J1S</sub>			±150	ps
Jitter, Absolute, All Frequencies	TJABS			±250	ps
Frequency Transition Time, 50 to 4MHz	$T_{FT}$			20	ms
Power-up Time, Off to 80 MHz	T <sub>PU</sub>		15	30	ms

## **ELECTRICAL CHARACTERISTICS AT 3.3V**

**DC ELECTRICAL CHARACTERISTICS**  $(0^{\circ}C \le T_A \le 70^{\circ}C, V_{CC} = 3.3V \pm 10\%)$  (Note 2)

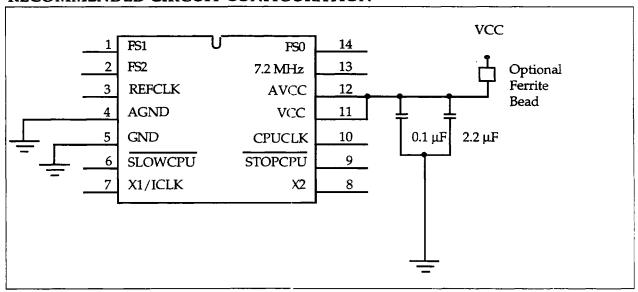
Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit
Supply Current	I <sub>CC</sub>	Note 2		12	20	mA
Input Low Voltage	$v_{IL}$	$V_{CC} = 3.3V$			0.15Vcc	V
Input High Voltage	$v_{IH}$	$V_{CC} = 3.3V$	0.7Vcc			V
Output Low Voltage	VOL	$I_{OL} = 8 \text{ mA}$			0.4	V
Output High Voltage	V <sub>OH</sub>	$I_{OH} = -4 \text{ mA}$	2.4			V
Input Capacitance	CI	Except X1, X2			10	рF
Load Capacitance	CL	Pins X1, X2		12		рF
Input Low Current	III	$V_{IN} = 0V$ (incl. pull-up res.)			-100	μΑ
Input High Current	IIH	$V_{IN} = V_{CC}$			10	μA
Input Pull-Up Resistor	Rp	$V_{IN} = 0V$		250		kΩ

Note 2: **W**42C26-01 with no load, with 14.318 MHz crystal input, and CLK1 running at 40 MHz. Power supply current varies with frequency and output load capacitance.

# AC CHARACTERISTICS (0°C $\leq$ T<sub>A</sub> $\leq$ 70°C, V<sub>CC</sub> = 3.3V $\pm$ 10 %)

Parameter	Symbol	Min	Тур	Max	Unit
Output Frequency (CPUCLK)	FO	2		80	MHz
Input Frequency	FI	2	14.318	32	MHz
Rise Time, 20 to 80% VCC, 15pF load	TR		2	4	ns
Fall Time, 80 to 20% VCC, 15pF Load	T <sub>F</sub>		2	4	ns
Duty Cycle, 15pF Load	$D_{\mathrm{T}}$	40	50/50	60	%
Jitter, 1 Sigma, All Frequencies	T <sub>J1S</sub>			± 150	ps
Jitter, Absolute, All Frequencies	T <sub>JABS</sub>			± 250	ps
Frequency Transition Time, 50 to 4 MHz	T <sub>FT</sub>			20	ms
Power-up Time, Off to 80 MHz	T <sub>PU</sub>		15	30	ms

# RECOMMENDED CIRCUIT CONFIGURATION



#### RECOMMENDED BOARD LAYOUT: W42C26

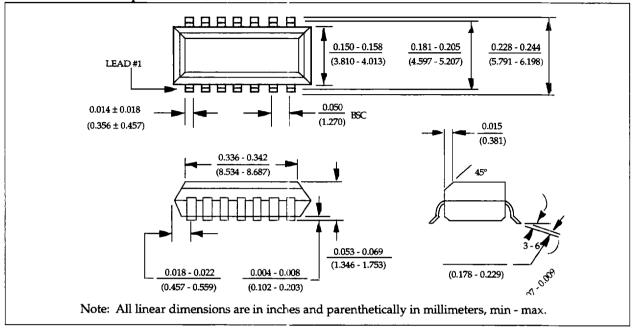
For optimum performance in system applications, the above power supply decoupling scheme should be used. Both GND pins are connected directly to the power plane.

VCC decoupling is important to reduce phase jitter and EMI radiation. The 0.1µF decoupling capacitor should be placed as close to the VCC pins as possible, otherwise the increased trace inductance will negate its decoupling capability. The 2.2µF decoupling capacitor shown is optional but will improve power supply rejection. For

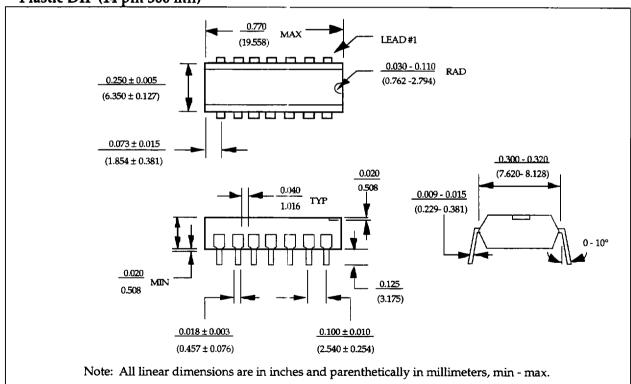
further EMI protection, the VCC connection can be made via a ferrite bead, as shown above. When using the w42C26, unused input select pins may be tied to either ground or VCC, or may be left unconnected; since internal pull-up resistors are incorporated on all logic input pins, an unconnected input will assume a logic 1 condition. Output clocks should use a series termination resistor (about 33 ohms) placed as close to the clock outputs as possible; this will also help to decrease jitter, EMI and clock signal ringing.

### **PACKAGING INFORMATION**

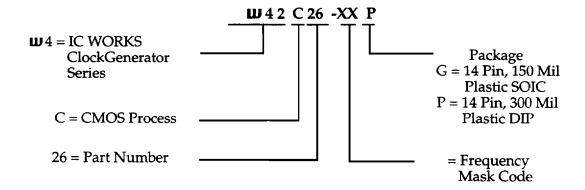
### Plastic SOIC (14 pin 150 mil)



#### Plastic DIP (14 pin 300 mil)



#### ORDERING INFORMATION



#### VALID PART NUMBERS

**W**42C26-01G **W**4

**ш**42C26-14G

ш42C26-15G

**ш**42С26-16G **ш**42С26-16Р

**W42**C26-01P **W42**C26-14P

**w**42C26-15P

ic works

IC WORKS, Inc. 3725 N. First Street San Jose, CA 95134-1700 Tel: (408) 922-0202

Fax: (408) 922-0833

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