Data Sheet
June 2007

TruePHY™ ET1011C
Gigabit Ethernet Transceiver

Features

- 10Base-T, 100Base-TX, and 1000Base-T gigabit Ethernet transceiver:
  - — 0.13 µm process
  - — 128-pin TQFP and 84-pin MLCC:
    - ❑ RGMII, GMII, MII, RTBI, and TBI interfaces to MAC or switch
  - — 68-pin MLCC:
    - ❑ RGMII and RTBI interfaces to MAC or switch
- Low power consumption:
  - — Typical power less than 750 mW in 1000Base-T mode
  - — Advanced power management
  - — ACPI compliant wake-on-LAN support
- Oversampling architecture to improve signal integrity and SNR
- Optimized, extended performance echo and NEXT filters
- All-digital baseline wander correction
- Digital PGA control
- On-chip diagnostic support
- Automatic speed negotiation
- Automatic speed downshift
- Single supply 3.3 V or 2.5 V operation:
  - — On-chip regulator controllers
  - — 3.3 V or 2.5 V digital I/O
  - — 3.3 V tolerant I/O pins (MDC, MDIO, COMA, RESET_N, and JTAG pins)
  - — 1.0 V or 1.1 V core power supplies
  - — 1.8 V or 2.5 V for transformer center tap
- JTAG
- ET1011C is a pin-compatible replacement for the ET1011 device
- Commercial- and industrial-temperature versions available

Introduction

The LSI ET1011C is a Gigabit Ethernet transceiver fabricated on a single CMOS chip. Packaged in either an 128-pin TQFP, an 84-pin MLCC, or a 68-pin MLCC, the ET1011C is built on 0.13 µm technology for low power consumption and application in server and desktop NIC cards. It features single power supply operation using on-chip regulator controllers. The 10/100/1000Base-T device is fully compliant with *IEEE*® 802.3, 802.3u, and 802.3ab standards.

The ET1011C uses an oversampling architecture to gather more signal energy from the communication channel than possible with traditional architectures. The additional signal energy or analog complexity transfers into the digital domain. The result is an analog front end that delivers robust operation, reduced cost, and lower power consumption than traditional architectures.

Using oversampling has allowed for the implementation of a fractionally spaced equalizer, which provides better equalization and has greater immunity to timing jitter, resulting in better signal-to-noise ratio (SNR) and thus improved BER. In addition, advanced timing algorithms are used to enable operation over a wider range of cabling plants.

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Functional Description

The LSI ET1011C is a Gigabit Ethernet transceiver that simultaneously transmits and receives on each of the four UTP pairs of category 5 cable (signal dimensions or channels A, B, C, and D) at 125 Msymbols/s using five-level pulse-amplitude modulation (PAM). Figure 1 is a block diagram of its basic configuration.

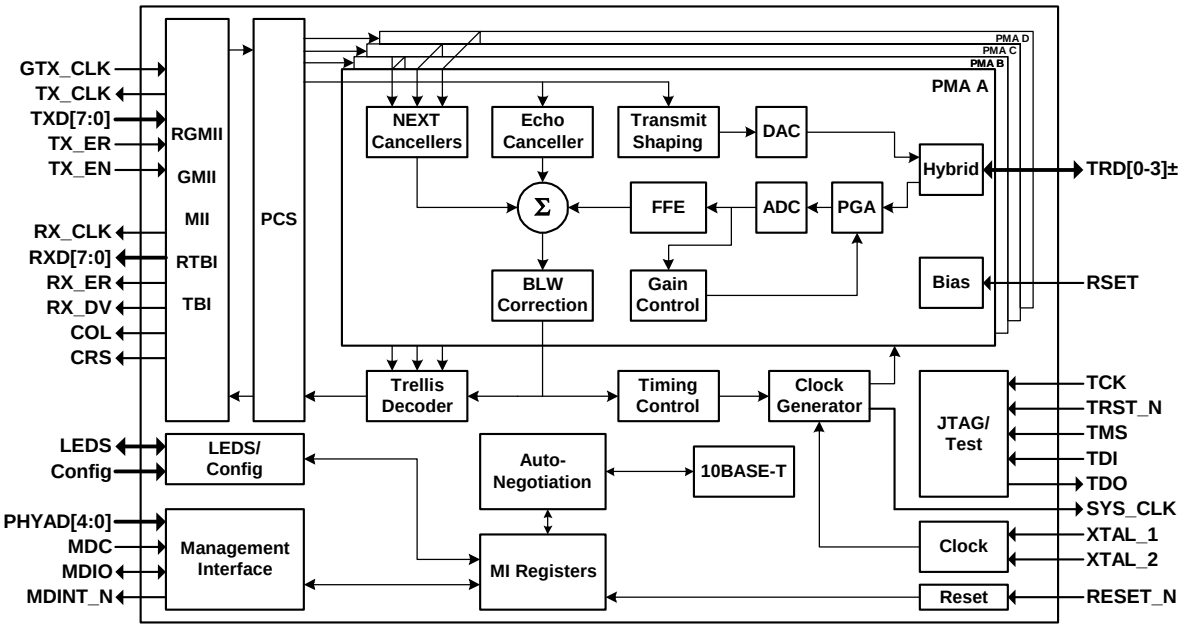

Figure 1. ET1011C Block Diagram

Oversampling Architecture

The ET1011C architecture uses oversampling techniques to sample at two times the symbol rate. A fractionally spaced feed forward equalizer (FFE) adapts to remove intersymbol interference (ISI) and to shape the spectrum of the received signal to maximize the (SNR) at the trellis decoder input. The FFE equalizes the channel to a fixed target response. Oversampling enables the use of a fractionally spaced equalizer (FSE) structure for the FFE, resulting in symbol rate clocking for both the FFE and the rest of the receiver. This provides robust operation and substantial power savings.

Automatic Speed Downshift

Automatic speed downshift is an enhanced feature of autonegotiation that allows the ET1011C to:

- Fallback in speed, based on cabling conditions or link partner abilities.
- Operate over CAT-3 cabling (in 10Base-T mode).
- Operate over two-pair CAT-5 cabling (in 100Base-TX mode).

For speed fallback, the ET1011C first tries to autonegotiate by advertising 1000Base-T capability. After a number of failed attempts to bring up the link, the ET1011C falls back to advertising 100Base-TX and restarts the autonegotiation process. This process continues through all speeds down to 10Base-T. At this point, there are no lower speeds to try and so the host enables all technologies and starts again.

PHY configuration register, address 22, bits 11 and 10 enable automatic speed downshift and specifies if fallback to 10Base-T is allowed. PHY control register, address 23, bits 11 and 12 specify the number of failed attempts before downshift (programmable to 1, 2, 3, or 4 attempts).

Functional Description (continued)

Transmit Functions

1000Base-T Encoder

In 1000Base-T mode, the ET1011C translates 8-bit data from the MAC interfaces into a code group of four quinary symbols that are then transmitted by the PMA as 4D five-level PAM signals over the four pairs of CAT-5 cable.

100Base-TX Encoder

In 100Base-TX mode, 4-bit data from the media independent interface (MII) is 4B/5B encoded to output 5-bit serial data at 125 MHz. The bit stream is sent to a scrambler, and then encoded to a three-level MLT3 sequence that is then transmitted by the PMA.

10Base-T Encoder

In 10Base-T mode, the ET1011C transmits and receives Manchester-encoded data.

Receive Functions

Decoder 1000Base-T

In 1000Base-T mode, the PMA recovers the 4D PAM signals after compensating for the cabling conditions. The resulting code group is decoded to 8-bit data. Data stream delimiters are translated appropriately, and the data is output to the receive data pins of the MAC interfaces. The GMII receive error signal is asserted when invalid code groups are detected in the data stream.

Decoder 100Base-TX

In 100Base-TX mode, the PMA recovers the three-level MLT3 sequence that is descrambled and 5B/4B decoded to 4-bit data. This is output to the MII receive data pins after data stream delimiters have been translated appropriately. The MII receive error signal is asserted when invalid code groups are detected in the data stream.

Decoder 10Base-T

In 10Base-T mode, the ET1011C decodes the Manchester-encoded received signal.

Hybrid

The hybrid subtracts the transmitted signal from the input signal allowing full-duplex operation on each of the twisted-pair cables.

Programmable Gain Amplifier (PGA)

The PGA operates on the received signal in the analog domain prior to the analog-to-digital converter (ADC). The gain control module monitors the signal at the output of the ADC in the digital domain to control the PGA. It implements a gain that maximizes the signal at the ADC while ensuring that no hard clipping occurs.

Clock Generator

A clock generator circuit uses the 25 MHz input clock signal and a phase-locked loop (PLL) circuit to generate all the required internal analog and digital clocks. A 125 MHz system clock is also generated and is available as an output clock.

Analog-to-Digital Converter

The ADC operates at 250 MHz oversampling at twice the symbol rate in 1000Base-T and 100Base-TX. This enables innovative timing recovery and fractional skew correction and has allowed transfer of analog complexity to the digital domain.

Timing Recovery/Generation

The timing recovery and generator block creates transmit and receive clocks for all modes of operation. In transmit mode, the 10Base-T and 100Base-TX modes use the 25 MHz clock input. While in receive mode, the input clock is locked to the receive data stream. 1000Base-T is implemented using a master-slave timing scheme, where the master transmit and receive are locked to the 25 MHz clock input, and the slave acquires timing information from the receive data stream. Timing recovery is accomplished by first acquiring lock on one channel and then making use of the constant phase relationship between channels to lock on the other pairs, resulting in a simplified PLL architecture. Timing shifts due to changing environmental conditions are tracked by the ET1011C.

Functional Description (continued)

Adaptive Fractionally Spaced Equalizer

The ET1011C's unique oversampling architecture employs an FSE in place of the traditional FFE structure. This results in robust equalization of the communications channel, which translates to superior bit error rate (BER) performance over the widest variety of worst-case cabling scenarios. The all-digital equalizer automatically adapts to changing conditions.

Echo and Crosstalk Cancellers

Since the four twisted pairs are bundled together and not insulated from each other in Gigabit Ethernet, each of the transmitted signals is coupled onto the three other cables and is seen at the receiver as near-end crosstalk (NEXT). A hybrid circuit is used to transmit and receive simultaneously on each pair. If the transmitter is not perfectly matched to the line, a signal component will be reflected back as an echo. Reflections can also occur at other connectors or cable imperfections. The ET1011C cancels echo and NEXT by subtracting an estimate of these signals from the equalizer output.

Baseline Wander Correction

A known issue for 1000Base-T and 100Base-TX is that the transformer attenuates at low frequencies. As a result, when a large number of symbols of the same sign are transmitted consecutively, the signal at the receiver gradually dies away. This effect is called baseline wander. By employing a circuit that continuously monitors and compensates for this effect, the probability of encountering a receive symbol error is reduced.

Autonegotiation

Autonegotiation is implemented in accordance with *IEEE* 802.3. The device supports 10Base-T, 100Base-TX, and 1000Base-T and can autonegotiate between them in either half- or full-duplex mode. It can also parallel detect 10Base-T or 100Base-TX. If autonegotiation is disabled, a 10Base-T or 100Base-TX link can be manually selected via the *IEEE* MII registers.

Pair Skew Correction

In Gigabit Ethernet, pair skew (timing differences between pairs of cable) can result from differences in length or manufacturing variations between the four individual twisted-pair cables. The ET1011C automatically corrects for both integer and fractional symbol timing differences between pairs.

Automatic MDI Crossover

During autonegotiation, the ET1011C automatically detects and sets the required MDI configuration so that the remote transmitter is connected to the local receiver and vice versa. This eliminates the need for crossover cables or crosswired (MDIX) ports. If the remote device also implements automatic MDI crossover, and/or the crossover is implemented in the cable, the crossover algorithm ensures that only one element implements the required crossover.

Polarity Inversion Correction

In addition to automatic MDI crossover that is necessary for autonegotiation, 10Base-T, and 100Base-TX operation, the ET1011C automatically corrects crossover of the additional two pairs used in 1000Base-T. Polarity inversion on all pairs is also corrected. Both of these effects may arise if the cabling has been incorrectly wired.

Carrier Sense (128-Pin TQFP and 84-Pin MLCC Only)

The carrier sense signal (CRS) of the MAC interface is asserted by the ET1011C whenever the receive medium is nonidle. In half-duplex mode, CRS may also be asserted when the transmit medium is nonidle. The CRS may be enabled on transmit in half-duplex mode by writing to the PHY configuration register, address 22, bit 15.

Functional Description (continued)

Link Monitor

1000Base-T

Once 1000Base-T is autonegotiated and the link is established, both link partners continuously monitor their local receiver status. If the master device determines a problem with its receiver, it signals the slave and both devices cease transmitting data but transmit IDLE. If the master retrains its receiver within 750 ms, then normal operation recommences. Otherwise, both devices restart autonegotiation.

If the slave device determines a problem with its receiver, it ceases transmitting and expects the master to transmit the IDLE sequence. If the slave retrains its receiver within 350 ms, normal operation recommences when the master signals that its receiver is ready. If either receiver fails to reacquire, then autonegotiation is restarted.

100Base-TX

In 100Base-TX mode, the ET1011C monitors the link and determines the link quality based on signal energy, mean square error and scrambler lock. If the link quality is deemed insufficient, transmit and receive data are disabled. If the link had been autonegotiated, then control is handed back to autonegotiation. If the link had been manually set, the 100Base-TX receiver is retrained, and the transmitter is set to transmit idle. Once the link quality has been recovered, data transmit and receive are enabled.

10Base-T

In 10Base-T mode, the ET1011C monitors the link and determines the link quality based either on the presence of valid link pulses or valid 10Base-T packets. If the link is deemed to have failed and the link had been autonegotiated, then control is handed back to autonegotiation. If the link had been manually set, the ET1011C continues to try to reestablish the link.

Functional Description (continued)

Loopback Mode

Enabling loopback mode allows in-circuit testing of the ET1011C's digital and analog data path.

The ET1011C provides several options for loopback that test and verify various functional blocks within the PHY. These are digital loopback and analog loopback. Figure 2 is a block diagram that shows the PHY loopback functionality.

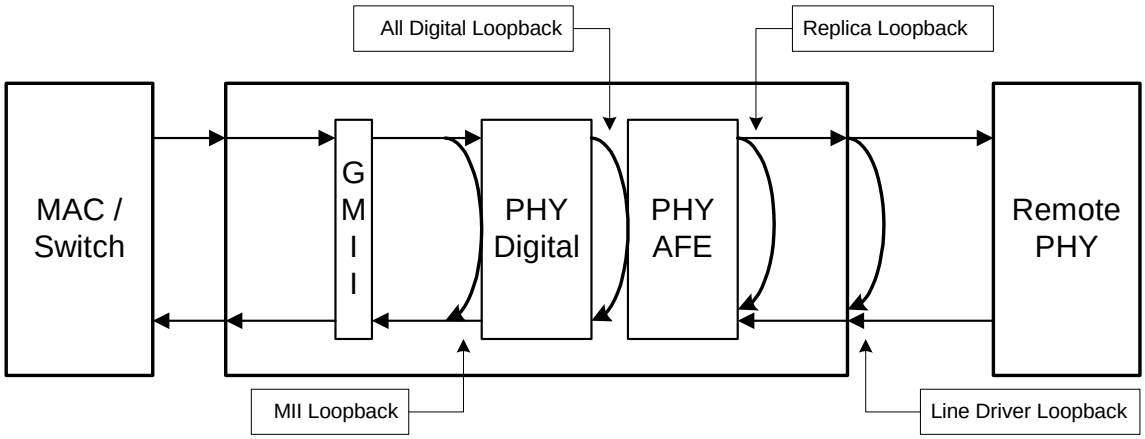

Figure 2. Loopback Functionality

The loopback mode is selected by setting the respective bit in the PHY loopback control register, MII register address 19. The default loopback mode is digital MII loopback. Loopback is enabled by writing to the PHY control register, address 0, bit 14.

Digital Loopback

Digital loopback provides the ability to loop the transmitted data back to the receiver via the digital circuitry. The point at which the signal is looped back is selected using the loopback control register with the following options being provided: MII and all digital. Selecting the MII option gives a simple loopback with minimal latency where the data is looped back directly at the media-independent interface. This loopback is currently set as the default, but it should be noted that it only exercises a small percentage of the PHY circuitry. When the all-digital option is selected, the transmitted data is looped back at the interface between the digital and the analog circuitry, thereby exercising a high percentage of the digital logic. Figure 3 shows a block diagram of digital loopback.

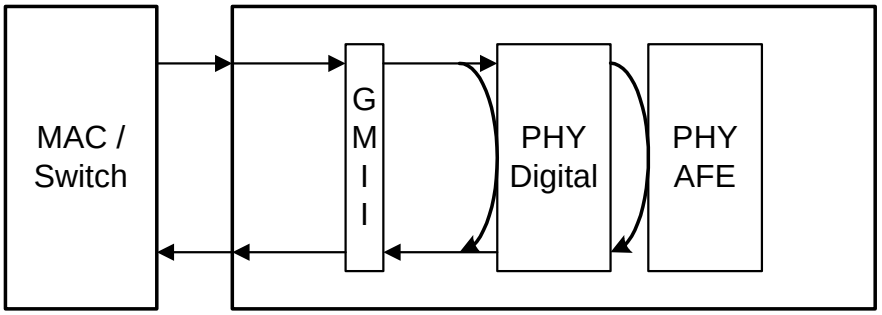

Figure 3. Digital Loopback

Functional Description (continued)

Analog Loopback

Analog loopback provides the ability to loop the transmitted signal back to the receiver within the AFE. The point at which the signal is looped back is selected using the loopback control register with the following options being provided: replica and line driver.

Selecting the replica option causes the transmitted signal to be looped back through the replica generation circuitry of the on-chip hybrid, thereby allowing most of the digital and analog circuitry to be exercised. This loopback mode may be used even when the device is connected to a network because nothing is transmitted to or received from the MDI in this case.

Line driver loopback transmits data to and receives data from the MDI. However, in general, this loopback may not be used when the device is connected to a network because it could cause an unanticipated response from the link partner. Line driver loopback requires 100 Ω terminations to be present on the line side of the transformer for each wire pair. For example, for wire pair A, connect a 100 Ω resistor between the leads (pins 1 and 2) of a short cable plugged into the RJ45. This should also be done for wire pairs B, C, and D. Another way to accomplish this is to connect to a link partner with a short cable and powerdown the link partner. Figure 4 shows a block diagram of both replica and line driver loopbacks.

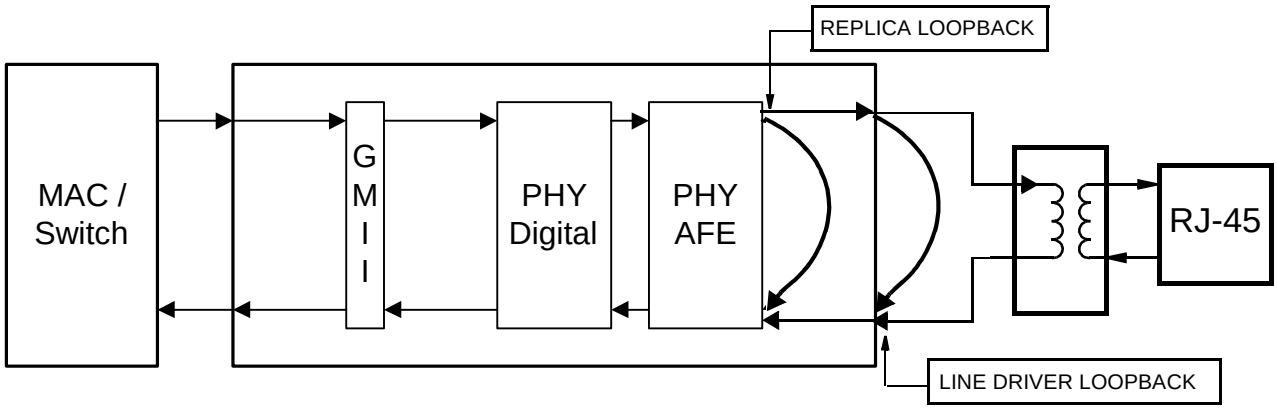

Figure 4. Replica and Line Driver Analog Loopback

External Cable Loopback

External cable loopback loops GMII Tx to GMII Rx via complete digital and analog path and via an external cable. The external cable should have pair A (pins 1 and 2) looped to pair B (pins 3 and 6), and pair C (pins 4 and 5) looped to pair D (pins 7 and 8). This will test all the digital data paths and all the analog circuits. Figure 5 shows a block diagram of external cable loopback

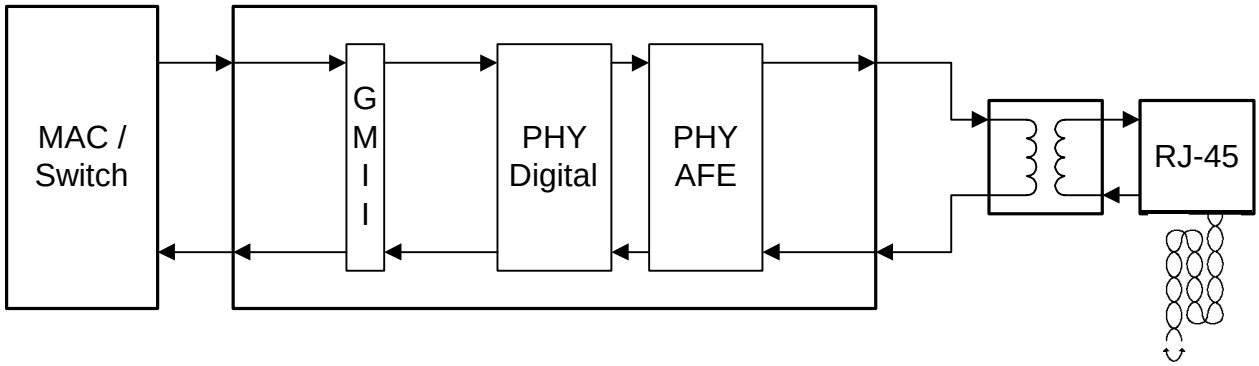

Figure 5. External Cable Loopback

Functional Description (continued)

LEDs

Four status LEDs are provided. These can be used to indicate speed of operation, duplex mode, link status, etc. There is a very high degree of programmability allowed. Hence, the LEDs can be programmed to different status functions from their default value, or they can be controlled directly from the MII register interface. The LED signal pins can also be used for general-purpose I/O if not needed for LED indication.

Regulator Control

The ET1011C has two on-chip regulator controllers. This allows the device to be powered from a single supply, either 3.3 V or 2.5 V. The on-chip regulator control circuits provide output control voltages that can be used to control two external transistors and thus provide regulated 1.0 V and 2.5 V supplies.

Resetting the ET1011C

The ET1011C provides the ability to reset the device by hardware (pin RESET_N) or via software through the management interface. A hardware reset is accomplished by driving the active-low pin RESET_N to 0 volts for a minimum of 20 µs. The configuration pins and the physical address configuration are read during a hardware reset. A hardware reset is required after powerup in order to ensure proper operation.

A software reset is accomplished by setting bit 15 of the control register (MII register address 0, bit 15). The configuration pins and the physical address configuration are not read during software reset.

Low-Power Modes

The ET1011C supports a number of powerdown modes.

Hardware Powerdown Mode

Hardware powerdown is entered when the COMA signal is driven high. In hardware powerdown, all PHY functions (analog and digital) are disabled. During hardware powerdown, SYS_CLK is not available and the MII registers are not accessible.

At exit from hardware powerdown, the ET1011C does the following:

- Initializes all analog circuits including the PLL.
- Initializes all digital logic and state machines.
- Reads and latches the PHY address pins.
- Initializes all MII registers to their default values (H/W configuration pins are reread).

Software Powerdown Mode

Software powerdown is entered when bit 11 of the control register (MII register address 0, bit 11) is set. In software powerdown, all PHY functions except the serial management interface and clock circuitry are disabled. The MII registers can be read or written. If the system clock output is enabled (MII register address 22, bit 4), the 125 MHz system clock will still be available for use by the MAC on pin SYS_CLK.

At exit from software powerdown, the ET1011C does the following:

- Initializes all digital logic and state machines.

Note: At exit from software powerdown, the H/W configuration pins and the PHY address pins are not reread and the MII registers are not reset to their default values. These operations are only done during reset or recovery from hardware powerdown.

Wake-On-LAN Powerdown Mode

ACPI power consumption compliant Wake-On-LAN mode is implemented on the ET1011C by using the *IEEE* standard MII registers to put the PHY into 10Base-T or 100Base-TX modes. Clearing the advertisement of 1000Base-T (MII register address 9, bits 8, 9) and setting the desired 10Base-T and 100Base-TX advertisement (MII register address 4, bits 5—8) activates this feature. This must be followed by an autonegotiation restart via the control register (MII register address 0, bit 9).

Low-Power Energy-Detect (LPED) Mode

When COMA is asserted, low-power energy-detect (LPED) mode is enabled if LPED_EN_N is low. In this mode, the PHY monitors the cable for energy. If energy is detected, the MDINT_N pin is asserted. The PHY exits from LPED mode when COMA is deasserted. An alternate method to enable LPED is also available. When RESET_N and LPED_EN_N are both low (asserted) and SYS_CLK_EN_N is high (deasserted), then the LPED mode is also enabled.

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Pin Information

Pin Diagram, 128-Pin TQFP

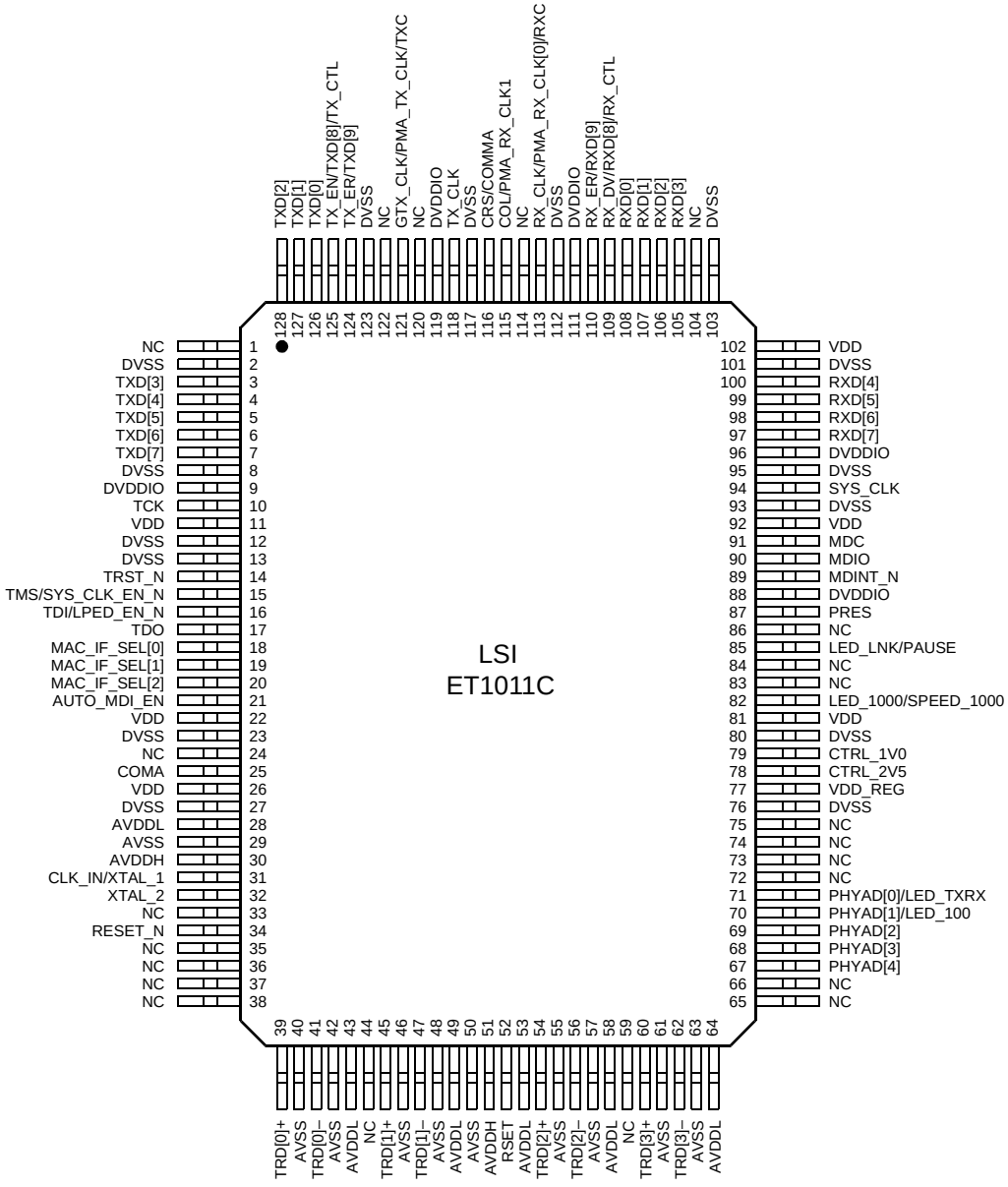


Figure 6. Pin Diagram for ET1011C in 128-Pin TQFP Package (Top View)

Pin Information (continued)

Pin Diagram, 84-Pin MLCC

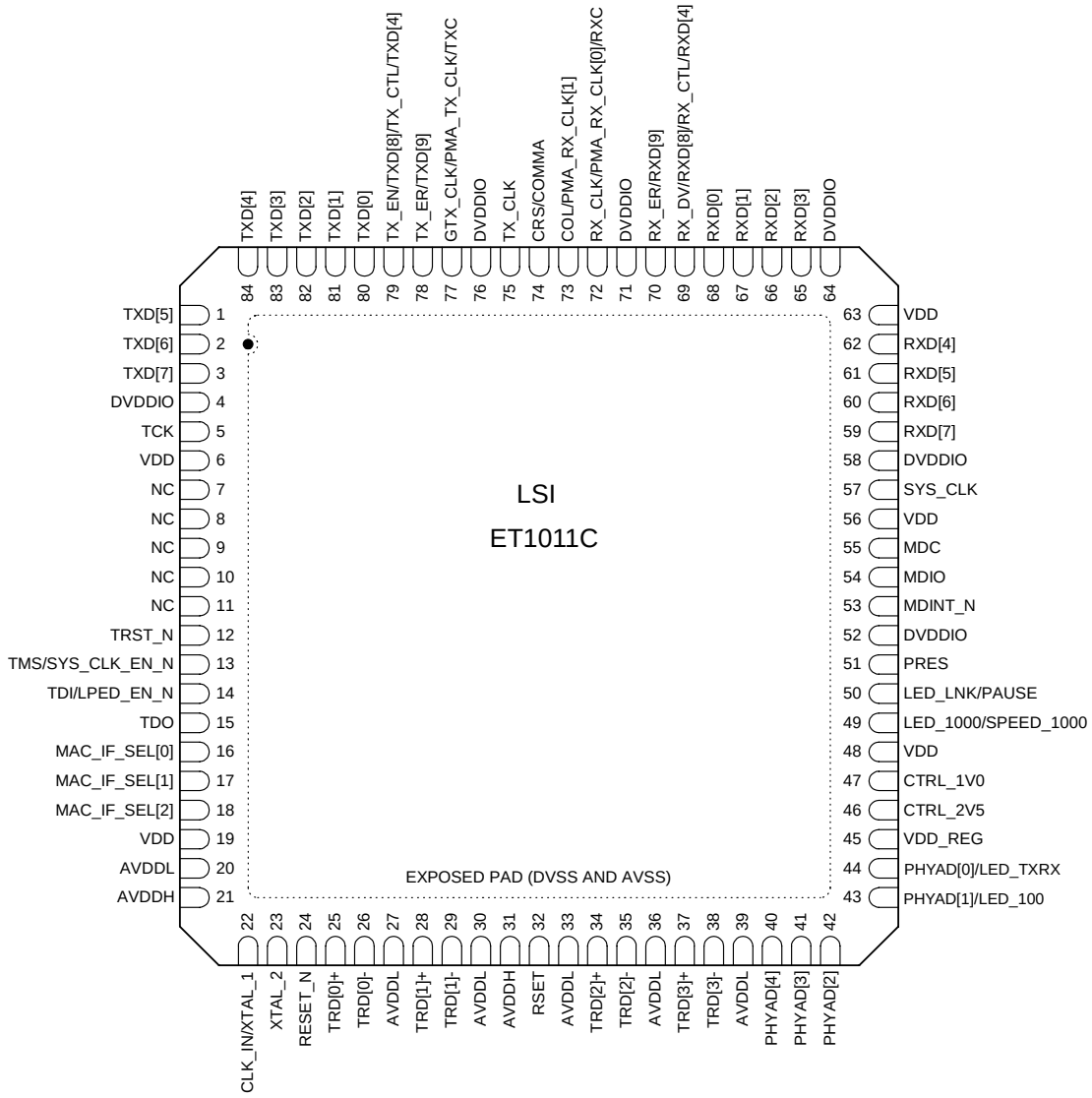


Figure 7. Pin Diagram for ET1011C in 84-Pin MLCC Package (Top View)

Pin Information (continued)

Pin Diagram, 68-Pin MLCC

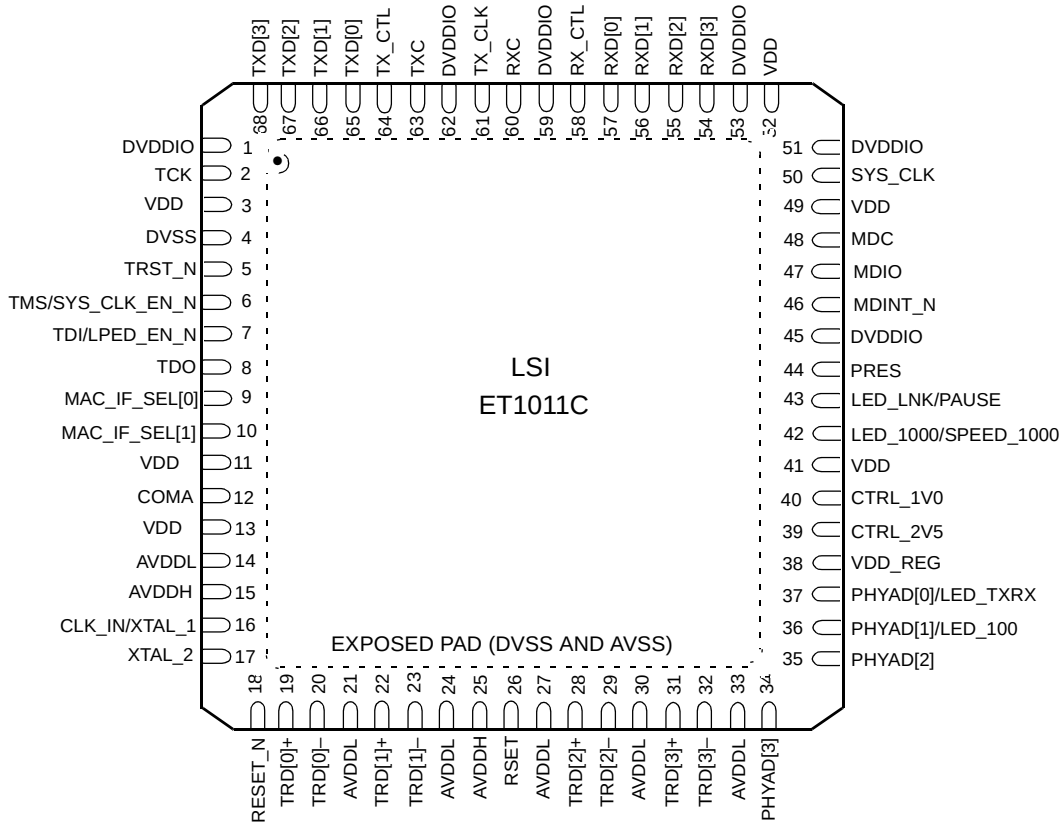


Figure 8. Pin Diagram for ET1011C in 68-Pin MLCC Package (Top View)

Pin Information (continued)

Pin Descriptions, 128-Pin TQFP, 84-Pin MLCC, and 68-Pin MLCC

Table 1. ET1011C Device Signals by Interface, 128-Pin TQFP, 84-Pin and 68-Pin MLCC

Name	Description	Pad Type	Internal Pull-Up/ Pull-Down	3-State	Analog	Pin # 128-Pin TQFP	Pin # 84-Pin MLCC	Pin # 68-Pin MLCC
MAC: GMII—Gigabit Media-Independent Interface (128-Pin TQFP and 84-Pin MLCC Only)								
GTX_CLK	GMII transmit clock	I	—	—	—	121	77	—
TX_ER	Transmit error	I	—	—	—	124	78	—
TX_EN	Transmit enable	I	—	—	—	125	79	—
TXD[7:0]	Transmit data bits	I	—	—	—	7, 6, 5, 4, 3 128, 127, 126	3, 2, 1, 84, 83, 82, 81, 80	—
RX_CLK	Receive clock	O	—	Z	—	113	72	—
RX_ER	Receive error	O	—	Z	—	110	70	—
RX_DV	Receive data valid	O	—	Z	—	109	69	—
RXD[7:0]	Receive data bits	O	—	Z	—	97, 98, 99, 100, 105, 106, 107, 108	59, 60, 61, 62, 65, 66, 67, 68	—
CRS	Carrier sense	O	—	Z	—	116	74	—
COL	Collision detect	O	—	Z	—	115	73	—
MAC: RGMII—Reduced Gigabit Media-Independent Interface								
TXC	RGMII transmit clock	I	—	—	—	121	77	63
TXD[3:0]	Transmit data bits	I	—	—	—	3, 128, 127, 126	83, 82, 81, 80	68, 67, 66, 65
TX_CTL	Transmit control	I	—	—	—	125	79	64
RXC	Receive clock	O	—	Z	—	113	72	60
RXD[3:0]	Receive data bits	O	—	Z	—	105, 106, 107, 108	65, 66, 67, 68	54, 55, 56, 57
RX_CTL	Receive control	O	—	Z	—	109	69	58
MAC: MII—Media-Independent Interface (128-Pin TQFP and 84-Pin MLCC Only)								
TX_CLK	MII transmit clock	O	—	Z	—	118	75	—
TX_ER	Transmit error	I	—	—	—	124	78	—
TX_EN	Transmit enable	I	—	—	—	125	79	—
TXD[3:0]	Transmit data bits	I	—	—	—	3, 128, 127, 126	83, 82, 81, 80	—
RX_CLK	Receive clock	O	—	Z	—	113	72	—
RX_ER	Receive error	O	—	Z	—	110	70	—
RX_DV	Receive data valid	O	—	Z	—	109	69	—
RXD[3:0]	Receive data bits	O	—	Z	—	105, 106, 107, 108	65, 66, 67, 68	—
CRS	Carrier sense	O	—	Z	—	116	74	—
COL	Collision detect	O	—	Z	—	115	73	—

Pin Information (continued)

Pin Descriptions, 128-Pin TQFP, 84-Pin MLCC, and 68-Pin MLCC (continued)

Table 1. ET1011C Device Signals by Interface, 128-Pin TQFP, 84-Pin and 68-Pin MLCC (continued)

Name	Description	Pad Type	Internal Pull-Up/ Pull-Down	3-State	Analog	Pin # 128-Pin TQFP	Pin # 84-Pin MLCC	Pin # 68-Pin MLCC
MAC: TBI—Ten-Bit Interface (128-Pin TQFP and 84-Pin MLCC Only)								
PMA_ TX_CLK	TBI transmit clock	I	—	—	—	121	77	—
TXD[9:0]	Transmit data bits	I	—	—	—	124, 125, 7, 6, 5, 4, 3, 128, 127, 126	78, 79, 3, 2, 1, 84, 83, 82, 81, 80,	—
PMA_RX_CLK[0]	TBI receive clock	O	—	Z	—	113	72	—
RXD[9:0]	Receive data bits	O	—	Z	—	110, 109, 97, 98, 99, 100, 105, 106, 107, 108	70, 69, 59, 60, 61, 62, 65, 66, 67, 68,	—
PMA_RX_ CLK[1]	TBI receive clock	O	—	Z	—	115	73	—
COMMA	Valid comma detect	I	—	—	—	116	74	—
MAC: RTBI—Reduced Ten-Bit Interface								
TXC	RTBI transmit clock	I	—	—	—	121	77	63
TXD[3:0]	Transmit data bits	I	—	—	—	3, 128, 127, 126	83, 82, 81, 80,	68, 67, 66, 65
TX_CTL	Transmit control	I	—	—	—	125	79	64
RXC	RTBI receive clock	O	—	Z	—	113	72	60
RXD[3:0]	Receive data bits	O	—	Z	—	105, 106, 107, 108	65, 66, 67, 68	54, 55, 56, 57
RX_CTL	Receive control	O	—	Z	—	109	69	58
MDI: Transformer Interface								
TRD[0]+	Transmit and receive differential pair	I/O	—	—	A	39	25	19
TRD[0]–						41	26	20
TRD[1]+	Transmit and receive differential pair	I/O	—	—	A	45	28	22
TRD[1]–						47	29	23
TRD[2]+	Transmit and receive differential pair	I/O	—	—	A	54	34	28
TRD[2]–						56	35	29
TRD[3]+	Transmit and receive differential pair	I/O	—	—	A	60	37	31
TRD[3]–						62	38	32
RSET	Analog reference resistor	I/O	—	—	A	52	32	26

Pin Information (continued)

Pin Descriptions, 128-Pin TQFP, 84-Pin MLCC, and 68-Pin MLCC (continued)

Table 1. ET1011C Device Signals by Interface, 128-Pin TQFP, 84-Pin and 68-Pin MLCC (continued)

Name	Description	Pad Type	Internal Pull-Up/ Pull-Down	3-State	Analog	Pin # 128-Pin TQFP	Pin # 84-Pin MLCC	Pin # 68-Pin MLCC
Management Interface								
PHYAD[4:0]	PHY address 4—1	I	Pull-down	—	—	67, 68, 69, 71, 70	40, 41, 42, 43, 44	34, 35, 36, 37 PHYAD [3:0]
	PHY address 0	I	Pull-up	—	—			
MDC	Management interface clock	I	Pull-down	—	—	91	55	48
MDIO	Management data I/O	I/O	Pull-up	—	—	90	54	47
MDINT_N	Management interface interrupt	O	—	—	—	89	53	46
Configuration[1]								
SPEED_1000	1000Base-T speed select	I	Pull-up	—	—	82	49	42
PAUSE	Pause mode	I	Pull-down	—	—	85	50	43
AUTO_MDI_EN	Auto-MDI detection enable	I	Pull-up	—	—	21	—	—
MAC_IF_SEL[0]	MAC interface select 0	I	Pull-down	—	—	18	16	9
MAC_IF_SEL[1]	MAC interface select 1	I	Pull-down	—	—	19	17	10
MAC_IF_SEL[2]	MAC interface select 2	I	Pull-down	—	—	20	18	—
SYS_CLK_EN_N	System clock enable	I	Pull-up	—	—	15	13	6
LPED_EN_N	Low power energy detection enable	I	Pull-up	—	—	16	14	7
PRES	Precision resistor	I	—	—	—	87	51	44

1. Configuration signals are multiplexed with the LED controls. During a reset, the status of the configuration pins are latched and used to set the configuration and later to select the polarity to drive the LEDs.

Pin Information (continued)

Pin Descriptions, 128-Pin TQFP, 84-Pin MLCC, and 68-Pin MLCC (continued)

Table 1. ET1011C Device Signals by Interface, 128-Pin TQFP, 84-Pin and 68-Pin MLCC (continued)

Name	Description	Pad Type	Internal Pull-Up/ Pull-Down	3-State	Analog	Pin # 128-Pin TQFP	Pin # 84-Pin MLCC	Pin # 68-Pin MLCC
LED Interface								
LED_1000	1000Base-T LED	O	Pull-up	—	—	82	49	42
LED_LNK	Link established LED	O	Pull-down	—	—	85	50	43
LED_TXRX	General-purpose LED	I/O	Pull-up	—	—	71	44	37
LED_100	General-purpose LED	I/O	Pull-down	—	—	70	43	36
JTAG								
TCK	Test clock	I	Pull-up	—	—	10	5	2
TRST_N	Test reset	I	Pull-down	—	—	14	12	5
TMS	Test mode select	I	Pull-up	—	—	15	13	6
TDI	Test data input	I	Pull-up	—	—	16	14	7
TDO	Test data output	O	Pull-up	—	—	17	15	8
Clocking and Reset								
CLK_IN	Reference clock input	I/O	—	—	A	31	22	16
XTAL_1	Reference crystal input	I/O	—	—	A	31	22	16
XTAL_2	Reference crystal	I/O	—	—	A	32	23	17
SYS_CLK	System clock	O	—	—	—	94	57	50
RESET_N	Reset	I	—	—	—	34	24	18
COMA	Hardware powerdown	I	Pull-down	—	—	25	—	12
Regulator Control								
CTRL_1V0	Regulator control 1.0 V	O	—	—	A	79	47	40
CTRL_2V5	Regulator control 2.5 V	O	—	—	A	78	46	39

1. Configuration signals are multiplexed with the LED controls. During a reset, the status of the configuration pins are latched and used to set the configuration and later to select the polarity to drive the LEDs.

Pin Information (continued)

Pin Descriptions, 84-Pin MLCC and 68-Pin MCCC (continued)

Table 1. ET1011C Device Signals by Interface, 128-Pin TQFP, 84-Pin and 68-Pin MLCC (continued)

Name	Description	Pad Type	Internal Pull-Up/ Pull-Down	3-State	Analog	Pin # 128-Pin TQFP	Pin # 84-Pin MLCC	Pin # 68-Pin MLCC
Power, Ground, and No Connect								
VDD_REG	Regulator 2.5 V or 3.3 V supply	V_{DD}	—	—	—	77	45	38
DVDDIO	Digital I/O 2.5 V or 3.3 V supply	V_{DD}	—	—	—	9, 88, 96, 111, 119	4, 52, 58, 64, 71, 76	1, 45, 51, 53, 59, 62
VDD	Digital core 1.0 V supply	V_{DD}	—	—	—	11, 22, 26, 81, 92, 102	6, 19, 48, 56, 63	3, 11, 13, 41, 49, 52
DVSS[2]	Digital ground	V_{SS}	—	—	—	2, 8, 12, 13, 23, 27, 76, 80, 93, 95, 101, 103, 112, 117, 123	—	4
AVDDH	Analog power 2.5 V	V_{DD}	—	—	—	30, 51	21, 31	15, 25
AVDDL	Analog power 1.0 V	V_{DD}	—	—	—	28, 43, 49, 53, 58, 64	20, 27, 30, 33, 36, 39	14, 21, 24, 27, 30, 33
AVSS[2]	Analog ground	V_{SS}	—	—	—	29, 40, 42, 46, 48, 50, 55, 57, 61, 63	—	—
NC	Reserved—do not connect	—	—	—	—	1, 24, 33, 35, 36, 37, 38, 44, 59, 65, 66, 72, 73, 74, 75, 104, 114, 120, 122	7, 8, 9, 10, 11	—

1. Configuration signals are multiplexed with the LED controls. During a reset, the status of the configuration pins are latched and used to set the configuration and later to select the polarity to drive the LEDs.
2. All AVSS and DVSS pins share a common ground pin (pad) in the center of the device.

Pin Information (continued)

Pin Descriptions, 128-Pin TQFP, 84-Pin MLCC, and 68-Pin MLCC (continued)

Table 2. Multiplexed Signals on the ET1011C

Default	Pin # 128-Pin TQFP	Pin # 84-Pin MLCC	Pin # 68-Pin MLCC	Alternate
COL	115	73	—	COL[1, 6]
				PMA_RX_CLK[1][2]
CRS	116	74	—	CRS[1, 6]
				COMMA[2]
GTX_CLK	121	77	—	GTX_CLK[1]
			—	PMA_TX_CLK[2]
			63	TXC[3, 4]
LED_LNK	85	50	43	LED_LNK
				PAUSE[5]
LED_1000	82	49	42	LED_1000
				SPEED_1000[5]
LED_TXRX	71	44	37	LED_TXRX
				PHYAD[0][5]
LED_100	70	43	36	LED_100
				PHYAD[1][5]
RX_CLK	113	72	—	RX_CLK[1, 6]
			—	PMA_RX_CLK[0][2]
			60	RXC[3, 4]
RX_ER	110	70	—	RX_ER[1, 6]
				RXD[9][2]
RX_DV	109	69	—	RX_DV[1, 6]
			—	RXD[8][2]
			58	RX_CTL[3, 4]
TDI	16	14	7	TDI
				LPED_EN_N[5]
TMS	15	13	6	TMS
				SYS_CLK_EN_N[5]
TX_ER	124	78	—	TX_ER[1, 6]
				TXD[9][2]
TX_EN	125	79	—	TX_EN[1, 6]
			—	TXD[8][2]
			64	TX_CTL[3, 4]
XTAL_1	31	22	16	XTAL_1
				CLK_IN

1. GMII signal.
2. TBI signal.
3. RGMII signal.
4. RTBI signal.
5. Reset/configuration signal.
6. MII signal.

Hardware Interfaces

The following hardware interfaces are included on the ET1011C Gigabit Ethernet transceiver:

- MAC interfaces:
  - — GMII (128-pin TQFP/84-pin MLCC only)
  - — RGMII
  - — MII (128-pin TQFP/84-pin MLCC only)
  - — TBI (128-pin TQFP/84-pin MLCC only)
  - — RTBI
- Media-dependent interface
- Management interface
- Configuration interface
- LED interface
- Clock and reset signals
- JTAG interface
- Regulator control
- Power and ground signals

Several of the pins of the MAC interface are multiplexed, but they are designed to be interchangeable so that the device can change the MAC interface once the transmission capabilities (1000Base-T, 100Base-TX, and 10Base-T) are established.

The following diagram shows the various interfaces on each ET1011C and how they connect to the MAC and other support devices in a typical application.

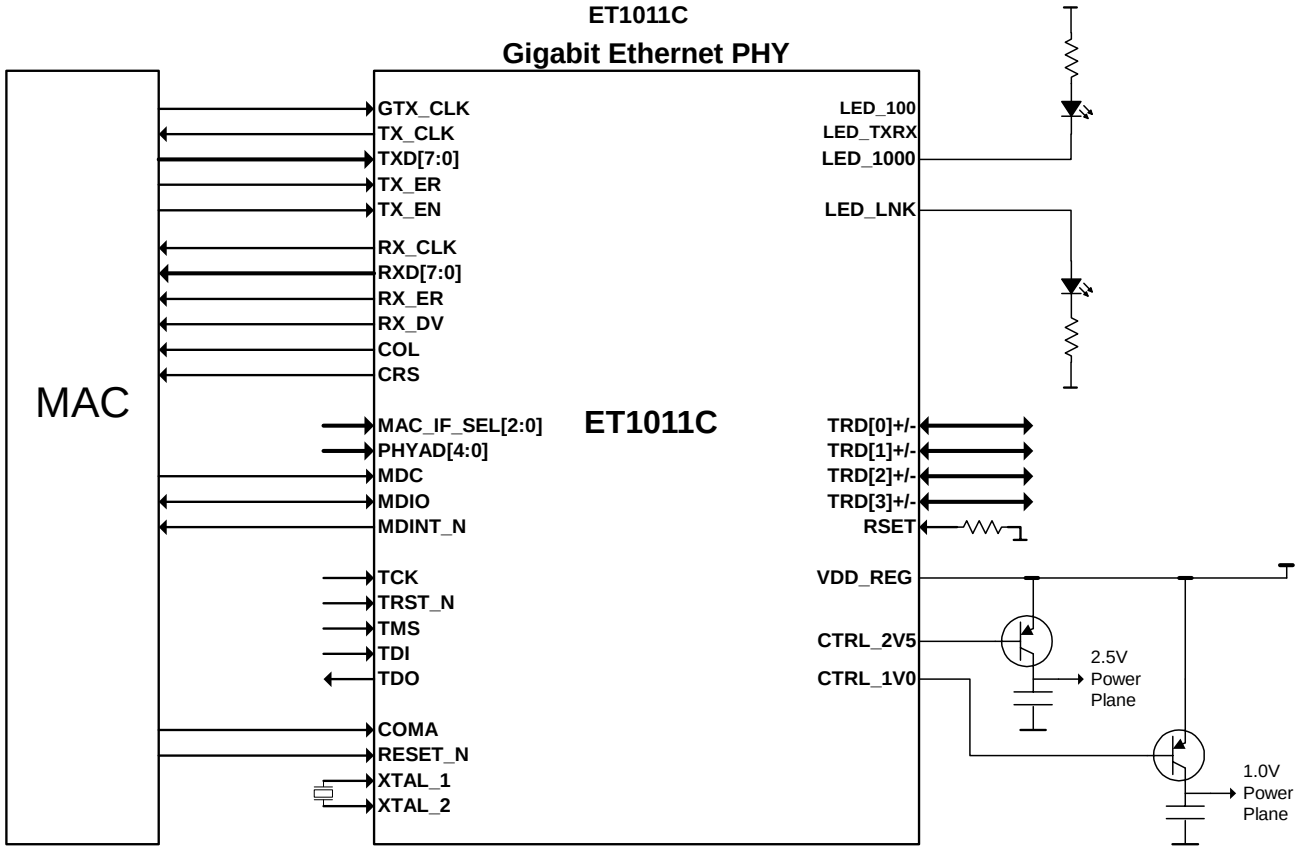


Figure 9. ET1011C Gigabit Ethernet Card Block Diagram

Hardware Interfaces (continued)

MAC Interface

The ET1011C supports RGMII, GMII, MII, RTBI, and TBI interfaces to the MAC. The MAC interface mode is selected via the hardware configuration pins, MAC_IF_SEL[2:0].

Gigabit Media-Independent Interface (GMII) (128-Pin TQFP and 84-Pin MLCC Only)

The GMII is fully compliant with *IEEE* 802.3 clause 35. The GMII interface mode is selected by setting the hardware configuration pins MAC_IF_SEL[2:0] = 000.

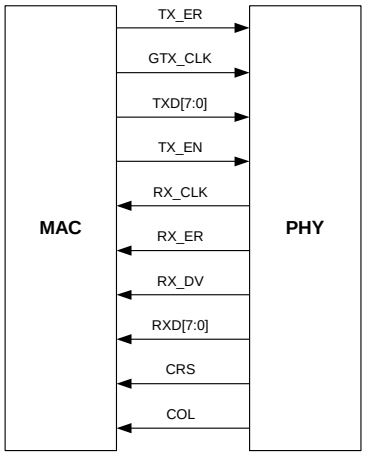


Figure 10. GMII MAC-PHY Signals

Table 3. GMII Signal Description (1000Base-T Mode) (128-Pin TQFP and 84-Pin MLCC only)

Pin Name	Pin # 128-Pin TQFP	Pin # 84-Pin MLCC	Pin Description	Functional Description
GTX_CLK	121	77	Transmit clock	The MAC drives this 125 MHz clock signal that is held low during autonegotiation or when operating in modes other than 1000Base-T.
TX_ER	124	78	Transmit error	The MAC drives this signal high to indicate a transmit coding error.
TX_EN	125	79	Transmit enable	The MAC drives this signal high to indicate that data is available on the transmit data bus.
TXD[7:0]	7, 6, 5, 4, 3, 128, 127, 126	3, 2, 1, 84, 83, 82, 81, 80	Transmit data bits 7—0	The MAC transmits data synchronized with GTX_CLK to the ET1011C for transmission on the media-dependent (transformer) interface.
RX_CLK	113	72	Receive clock	The ET1011C generates a 125 MHz clock to synchronize receive data.
RX_ER	110	70	Receive error	The ET1011C drives RX_ER to indicate that an error was detected in the frame that was received and is being transmitted to the MAC.
RX_DV	109	69	Receive data valid	The ET1011C drives RX_DV to indicate that it is sending recovered and decoded data to the MAC.
RXD[7:0]	97, 98, 99, 100, 105, 106, 107, 108	59, 60, 61, 62, 65, 66, 67, 68	Receive data	The ET1011C transmits data that is synchronized with RX_CLK to the MAC.
CRS	116	74	Carrier sense	The carrier sense signal (CRS) of the MAC interface is asserted by the ET1011C whenever the receive medium is nonidle. In half-duplex mode, CRS may also be asserted when the transmit medium is nonidle. The CRS may be enabled on transmit in half-duplex mode by writing to the PHY configuration register, address 22, bit 15.
COL	115	73	Collision detect	In 10Base-T, 100Base-TX, and 1000Base-T half-duplex modes, COL is asserted when both transmit and receive media are nonidle.

Hardware Interfaces (continued)

Reduced Gigabit Media-Independent Interface (RGMII)

The RGMII interface is fully compliant with the RGMII Rev. 1.3 specification. The RGMII interface mode is selected by setting the hardware configuration pins MAC_IF_SEL[2:0] = 100 or 110. (See Table 10 on page 30 for further information on MAC_IF_SEL pin operation.)

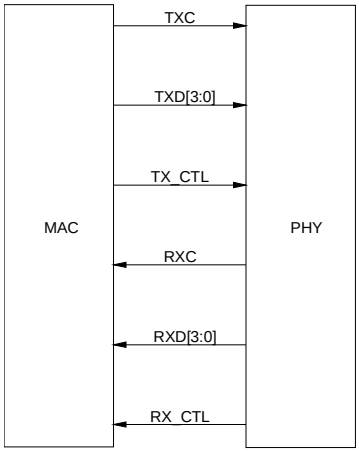


Figure 11. RGMII MAC-PHY Signals

Table 4. RGMII Signal Description (1000Base-T Mode)

Pin Name	Pin # 128-Pin TQFP	Pin # 84-Pin MLCC	Pin # 68-Pin MLCC	Pin Description	Functional Description
TXC	121	77	63	Transmit clock	The MAC drives this 125 MHz clock signal that is held low during autonegotiation. To obtain the 1 Gbit transmission rate, the MAC uses both the positive and negative clock transitions.
TXD[3:0]	3, 128, 127, 126	83, 82, 81, 80	68, 67, 66, 65	Transmit data bits	The MAC transmits data synchronized with TXC to the ET1011C for transmission on the media-dependent (transformer) interface. The MAC transmits bits 3:0 on a positive transition of TXC and bits 7:4 on a negative transition of TXC.
TX_CTL	125	79	64	Transmit control	The MAC transmits control signals across this line (TX_ER and TX_EN). The MAC transmits TX_EN[1] on a positive transition of TXC and TX_EN and TX_ER[1] on the negative transition of TXC.
RXC	113	72	60	Receive clock	The ET1011C generates a 125 MHz clock to synchronize receive data. To obtain the 1 gigabit transmission rate, the ET1011C uses both the positive and negative clock transitions.
RXD[3:0]	105, 106, 107, 108	65, 66, 67, 68	54, 55, 56, 57	Receive data	The ET1011C transmits data that is synchronized with RX_CLK to the MAC. The ET1011C transmits bits 3:0 on a positive transition of RXC and bits 7:4 on the negative transition of RXC.
RX_CTL	109	69	58	Receive control	The ET1011C transmits control signals across this line (RX_ER and RX_EN). The ET1011C transmits RX_DV[1] on a positive transition of RXC and RX_EN[1] and RX_ER[1] on the negative transition of TXC.

1. Reference the GMII interface for description of the following parameters: TX_EN, TX_ER, RX_DV, RX_EN, and RX_ER.

Hardware Interfaces (continued)

Media-Independent Interface (128-Pin TQFP and 84-Pin MLCC Only)

The MII is fully compliant with *IEEE* 802.3 clause 22. The MII interface mode is selected by setting the hardware configuration pins MAC_IF_SEL[2:0] = 000.

In 100Base-TX and 10Base-T mode, the RXD[7:4] pins are driven low by the ET1011C and the TXD[7:4] pins are ignored. They should not be left floating but should be set either high or low. In the MII interface mode, the GTX_CLK pin may be held low.

An alternative to the standard MII is provided when operating in 10Base-T or 100Base-TX mode by setting hardware configuration pins MAC_IF_SEL[2:0] = 010. In this alternative interface, the MAC provides a reference clock at 2.5 MHz or 25 MHz at the GTX_CLK pin. The ET1011C then uses a FIFO to resynchronize data presented synchronously with this reference clock.

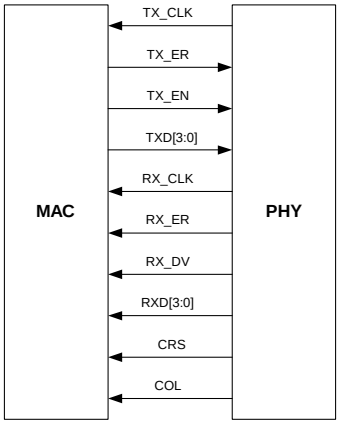


Figure 12. MII Signals

Table 5. MII Interface (100Base-TX and 10Base-T) (128-Pin TQFP and 84-Pin MLCC Only)

Pin Name	Pin # 128-Pin TQFP	Pin # 84-Pin MLCC	Pin Description	Functional Description
TX_CLK	118	75	Transmit clock	In 100Base-TX mode, the ET1011C generates 25 MHz reference clocks and in 10Base-T mode provides 2.5 MHz reference clocks. MAC_IF_SEL[2:0] = 000—this is default behavior.
GTX_CLK	121	77	Alternate transmit clock	In 100Base-TX mode, the MAC generates the 25 MHz reference clock and in 10Base-T mode provides a 2.5 MHz reference clock. MAC_IF_SEL[2:0] = 010.
TX_ER	124	78	Transmit error	The MAC drives this signal high to indicate a transmit coding error.
TX_EN	125	79	Transmit enable	The MAC drives this signal high to indicate that data is available on the transmit data bus.
TXD[3:0]	3, 128, 127, 126	83, 82, 81, 80	Transmit data bits	The MAC transmits data synchronized with TX_CLK to the ET1011C for transmission on the media-dependent (transformer) interface.
RX_CLK	113	72	Receive clock	In 100Base-TX mode, the ET1011C generates 25 MHz reference clocks and in 10Base-T mode provides 2.5 MHz reference clocks.
RX_ER	110	70	Receive error	The ET1011C drives RX_ER to indicate that an error was detected in the frame that was received and is being transmitted to the MAC.
RX_DV	109	69	Receive data valid	The ET1011C drives RX_DV to indicate that it is sending recovered and decoded data to the MAC.
RXD[3:0]	105, 106, 107, 108	65, 66, 67, 68	Receive data bits	The ET1011C transmits data synchronized with RX_CLK to the MAC.
CRS	116	74	Carrier sense	The carrier sense signal (CRS) of the MAC interface is asserted by the ET1011C whenever the receive medium is nonidle. In half-duplex mode, CRS may also be asserted when the transmit medium is nonidle. The CRS may be enabled on transmit in half-duplex mode by writing to the PHY configuration register, address 22, bit 15.
COL	115	73	Collision detect	In 10Base-T, 100Base-TX, and 1000Base-T half-duplex modes, COL is asserted when both transmit and receive media are nonidle.

Hardware Interfaces (continued)

Ten-Bit Interface (TBI) (128-Pin TQFP and 84-Pin MLCC Only)

The TBI is fully compliant with *IEEE* 802.3 clause 36. It may be used as an alternative to the GMII in 1000Base-T mode. The TBI mode is selected by setting the hardware configuration pins MAC_IF_SEL[2:0] = 001.

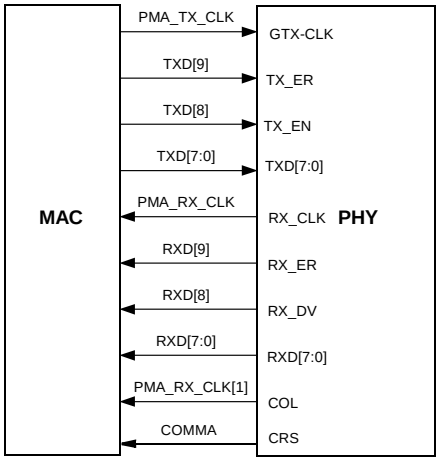


Figure 13. Ten-Bit Interface

Table 6. Ten-Bit Interface (1000Base-T) (128-Pin TQFP and 84-Pin MLCC Only)

Pin Name	Pin # 128-Pin TQFP	Pin # 84-Pin MLCC	Pin Description	Functional Description
PMA_TX _CLK	121	77	TBI transmit clock	The MAC drives this 125 MHz clock signal and should be held low during autonegotiation or when operating in modes other than 1000Base-T.
TXD[9:0]	124, 125, 7, 6, 5, 4, 3, 128, 127, 126	78, 79, 3, 2, 1, 84, 83, 82, 81, 80	Transmit data bits	The MAC transmits data synchronized with PMA_TX_CLK to the ET1011C for transmission on the media-dependent (transformer) interface.
PMA_RX _CLK[0]	113	72	Receive clock	The ET1011C generates a 62.5 MHz clock to synchronize receive data for the odd code group. This signal is 180 degrees out of phase from PMA_RX_CLK[1].
RXD[9:0]	110, 109, 97, 98, 99, 100, 105, 106, 107, 108	70, 69, 59, 60, 61, 62, 65, 66, 67, 68	Receive data bits	The ET1011C transmits data that is synchronized with PMA_ RX_CLK[0] to the MAC.
PMA_RX _CLK[1]	115	73	Receive clock	The ET1011C generates a 62.5 MHz clock to synchronize receive data for the even code group. This signal is 180 degrees out of phase from PMA_RX_CLK[0].
COMMA	116	74	Comma signal	This signal indicates that COMMA has been detected.

Hardware Interfaces (continued)

Reduced Ten-Bit Interface (RTBI)

The RTBI is fully compliant with RGMII rev 1.3 specification. The RTBI mode is selected by setting the hardware configuration pins MAC_IF_SEL[2:0] = 101 or 111. (See Table 10 on page 30 for further information on MAC_IF_SEL pin operation.)

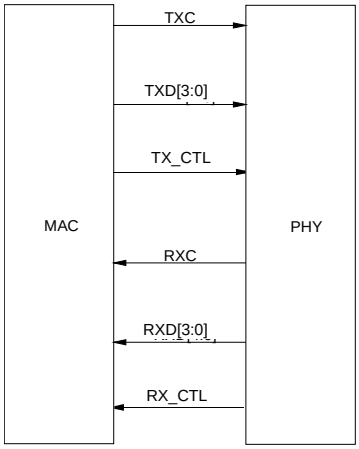


Figure 14. Reduced Ten-Bit Interface

Table 7. RTBI Signal Description (1000Base-T Mode)

Pin Name	Pin # 128-Pin TQFP	Pin # 84-Pin MLCC	Pin # 68-Pin MLCC	Pin Description	Functional Description
TXC	121	77	63	Transmit clock	The MAC drives this 125 MHz clock signal that is held low during autonegotiation.
TXD[3:0]	3, 128, 127, 126	83, 82, 81, 80	68, 67, 66, 65	Transmit data bits	The MAC transmits data synchronized with TXC to the ET1011C for transmission on the media-dependent (transformer) interface. The MAC transmits bits 3:0 on a positive transition of TXC and bits 8:5 on a negative transition of TXC.
TX_CTL	125	79	64	Transmit control	The MAC transmits bit 5 and bit 10 synchronized with TXC to the ET1011C for transmission on the media-dependent (transformer) interface. The MAC transmits bit 5 on a positive transition of TXC and bit 10 on the negative transition of TXC.
RXC	113	72	60	Receive clock	The ET1011C generates a 125 MHz clock to synchronize receive data.
RXD[3:0]	105, 106, 107, 108	65, 66, 67, 68	54, 55, 56, 57	Receive data	The ET1011C transmits data that is synchronized with RXC to the MAC. The ET1011C transmits bits 3:0 on a positive transition of RXC and bits 8:5 on the negative transition of RXC.
RX_CTL	109	69	58	Receive control	The ET1011C transmits bit 5 and bit 10 synchronized with RXC to the MAC. The ET1011C transmits bit 5 on a positive transition of RXC and bit 10 on the negative transition of RXC.

Hardware Interfaces (continued)

Management Interface

Serial Management Interface

The MII management interface (MI) provides a simple, two-wire serial interface between the MAC and the PHY to allow access to control and status information in the internal registers of the ET1011C. The interface is compliant with *IEEE* 802.3 clause 22 and is compatible with the clause 45.3, enabling the two systems to co-exist on the same MDIO bus.

Management Frame Structure

Frames transmitted on the MI have the following structure.

Table 8. Management Frame Structure

	PRE	ST	OP	PHYAD	REGAD	TA	DATA	IDLE
Read	1. . . 1	01	10	aaaaa	rrrrr	ZO	d . . . d	Z
Write	1 . . . 1	01	01	aaaaa	rrrrr	10	d . . . d	Z

- **PRE** (preamble): At the beginning of each transaction, the MAC may send a sequence of 32 contiguous logic one bits on MDIO with 32 corresponding cycles on MDC to provide the PHY with a pattern that it can use to establish synchronization. The ET1011C supports MF preamble suppression, and thus the MAC may initiate management frames with the ST (start of frame) pattern.
- **ST** (start of frame): The start of frame is indicated by a <01> pattern. This pattern ensures transitions from the default logic one line state to zero and back to one. When a clause 45 start of frame <00> is received, the frame is ignored.
- **OP** (operation code): The operation code for a read transaction is <10>, while the operation code for a write transaction is <01>.
- **PHYAD** (PHY address): The PHY address is 5 bits. The first PHY address bit transmitted and received is the MSB of the address. Only the PHY that is addressed will respond to the MI operation.
- **REGAD** (register address): The register address is 5 bits. The first register address bit transmitted and received is the MSB of the address.
- **TA** (turnaround): The turnaround time is a 2-bit time spacing between the register address field and the data field of a management frame to avoid contention during a read transaction. For a read transaction, the PHY remains in a high-impedance state for the first bit time of the turnaround and drives a zero bit during the second bit time of the turnaround. During a write transaction, the PHY expects a one for the first bit time of the turnaround and a zero for the second bit time of the turnaround.
- **DATA** (data): The data field is 16 bits. The first data bit transmitted and received is the MSB of the register being addressed.
- **IDLE** (idle condition): The IDLE condition on MDIO is a high-impedance state, and the ET1011C internal pull-up resistor will pull the MDIO line to logic one.

Hardware Interfaces (continued)

Table 9. Management Interface

Pin Name	Pin # 128-Pin TQFP	Pin # 84-Pin MLCC	Pin # 68-Pin MLCC	Pin Description	Functional Description
PHYAD [4:0]	67, 68, 69, 70, 71	40, 41, 42, 43, 44	34, 35, 36, 37 (PHYAD [3:0])	PHY Address	The physical address of the ET1011C is configured at reset by the current state of the PHYAD[4:0] pins. Once these pins have been latched in at reset, the ET1011C is accessible via the management interface at the configured address. The default address is set to 1 by internal pull-up/downs. These may be overridden by external pull-up/downs. The valid range is 0 to 31[1].
MDC	91	55	48	Management Interface Clock	The management data clock (MDC) is a reference for the data signal and is generated by the MAC. It should be turned off when the MI is not being used. This pin has an internal pull-down resistor. MDC is nominally 2.5 MHz, and can work up to a maximum of 12.5 MHz.
MDIO	90	54	47	Management Data I/O	The management data input/output (MDIO) is a bidirectional data signal between the MAC and one or more PHYs. MDIO is a 3-state pin that allows either the MAC or the selected PHY to drive this signal. This pin has an internal pull-up resistor. An external pull-up resistor should also be used, the exact value depending on the number of PHYs sharing the MDIO signal. Data signals written by the MAC are sampled by the PHY synchronously with respect to the MDC. Data signals written by the PHY are generated synchronously with respect to the MDC. This pin requires an external pull-up (1 kΩ to 10 kΩ).
MDINT_N	89	53	46	Management Interface Interrupt	This pin is active-low and indicates an unmasked management interrupt. This pin requires an external pull-up resistor (1 kΩ to 4.7 kΩ). Pin is open drain.

1. PHYAD description applies to the 84-MLCC only. For the 68-MLCC, the valid range will be 0—15.

Management Interrupt

The ET1011C is capable of generating hardware interrupts on pin MDINT_N in response to a variety of user-selectable conditions. MDINT_N is an open-drain, active-low signal that can be wire-ORed with several other ET1011C devices. A single 2.2 kΩ pull-up resistor is recommended for this wire-OR configuration.

When an interrupt occurs, the system can poll the status of the interrupt status register on each device to determine the origin of the interrupt. There are nine conditions that can be selected to generate an interrupt:

- Autonegotiation status change
- Autonegotiation page received
- FIFO overflow/underflow
- Link status change
- CRC errors
- Full error counter
- Local/remote rx status change
- Automatic speed downshift occurred
- MDIO synchronization lost

The ET1011C is configured to generate an interrupt based on any of these conditions by use of the interrupt mask register (MII register 24). By setting the corresponding bit in the interrupt mask register for the desired condition, the ET1011C will generate the desired interrupt. The ET1011C can be polled on the status of an activated interrupt condition by accessing MII register interrupt status register (MII register 25). If this condition has occurred, the corresponding bit in the interrupt status register will be set. The interrupt status register is self-clearing on a read operation.

Hardware Interfaces (continued)

Configuration Interface

The hardware configuration pins listed in Table 10 initialize the ET1011C at power-on and reset. The configuration is latched during initialization and stored. These pins set the default value of their corresponding MII register bits.

Some configuration inputs are shared with LED pins. The hardware configuration and LED pins are read on initial powerup of the ET1011C, during a hardware reset and during recovery from hardware powerdown. The logic value at the pin is sensed and latched. After RESET_N has been deasserted (raised high), the shared configuration pins become outputs that are used to drive LEDs. (For details on sharing LED and configuration pins, refer to the application note, *TruePHY ET1011 Gigabit Ethernet PHY Design and Layout Guide*.)

Table 10. Configuration Signals

Pin Name	Pin # 128-Pin TQFP	Pin # 84-Pin MLCC	Pin # 68-Pin MLCC	Pin Description	Functional Description
SPEED_1000	82	49	42	Speed 1000	The SPEED_1000 configuration pin sets the default advertised speed. The deassertion of SPEED_1000 disables advertisement of the 1000Base-T to the remote end. The default is to advertise all three speeds.
PAUSE	85	50	43	Pause	This input sets the pause mode. If PAUSE is asserted, full-duplex pause and asymmetric pause operation are advertised. 0 = Don't advertise pause (default). 1 = Advertise full-duplex pause and asymmetric pause.
SYS_CLK_EN_N	15	13	6	SYS_CLK Enable	Enables the system clock. If SYS_CLK_EN_N is asserted when RESET_N is low, SYS_CLK will be enabled and will continue to be generated while RESET_N is low. If SYS_CLK_EN_N is not asserted when RESET_N is low, then SYS_CLK is disabled. 0 = SYS_CLK enabled. 1 = SYS_CLK disabled (default).
LPED_EN_N	16	14	7	Low Power Energy Detection Enable	LPED_EN_N enables the low-power energy-detect (LPED) mode when COMA is asserted (See page 11 for alternate method) When the PHY is in LPED mode, it can wake the MAC/controller (instead of *Magic Packet*) by asserting the MDINT_N pin to indicate the presence of cable energy. 0 = Low-power energy-detect mode enable. 1 = Low-power energy-detect mode disabled (default).
PRES	87	51	44	Precision Resistor	Connect a 1.0 kΩ precision resistor to ground to set termination for all digital I/Os.

Hardware Interfaces (continued)

Table 10. Configuration Signals (continued)

Pin Name	Pin # 128-Pin TQFP	Pin # 84-Pin MLCC	Pin # 68-Pin MLCC	Pin Description	Functional Description
MAC_IF_ SEL[2:0]	20 19 18	18 17 16	— 10 9 (MAC_IF_ SEL[1:0] (See Note 1.)	MAC Inter-face Mode	This input selects the desired MAC interface mode. Configure the MAC during reset as follows: 000 = GMII/MII (84-Pin MLCC default). 001 = TBI. 010 = GMII/MII (clocked by GTX_CLK instead of TX_CLK). 011 = Reserved. 100 = RGMII/RMII (RXC DLL delay; 68-MLCC default)[1]. 101 = RTBI (RXC DLL delay)[1]. 110 = RGMII/RMII (RXC and TXC DLL delay)[1]. 111 = RTBI (RXC and TXC DLL delay)[1].

1. In the 68-MLCC, MAC_IF_SEL 2 (= 1) will be set internally. Also, for all package types:
   — MAC_IF_SEL **pins** = 100 will set MAC interface mode select **bits** in register 22.2:0 = **110**; alternative RGMII TXC DLL Delay bit 23.6 = 1.
   — MAC_IF_SEL **pins** = 101 will set MAC interface mode select **bits** in register 22.2:0 = **111**; alternative RGMII TXC DLL Delay bit 23.6 = 1.
   — MAC_IF_SEL **pins** = 110 will set MAC interface mode select **bits** in register 22.2:0 = 110; alternative RGMII TXC DLL Delay bit 23.6 = 0.
   — MAC_IF_SEL **pins** = 111 will set MAC interface mode select **bits** in register 22.2:0 = 111; alternative RGMII TXC DLL Delay bit 23.6 = 0.

Hardware Interfaces (continued)

LEDs Interface

The ET1011C is capable of sinking or sourcing current to drive LEDs. These LEDs are used to provide link status information to the user. The ET1011C is capable of automatically sensing the polarity of the LEDs. The device determines the active sense of the LED based upon the input that is latched during configuration. Thus, if logic 1 is read, the device will drive the pin to ground to activate the LED; otherwise, it will drive the pin to supply to activate the LED.

The LEDs can be programmed to stretch out events to either 28, 60, or 100 ms. This makes very short events more visible to the user. All LEDs can be programmed to be on, off, or blink instead of the default status function. This is useful for alternative function indication under host processor control: for example, a system error during power-on self-check. All LEDs can be programmed to indicate one of thirteen different status functions instead of the default status function:

- 1000Base-T
- 100Base-TX
- 10Base-T
- 1000Base-T (on) and 100Base-TX (blink)
- Link established
- Transmit activity
- Receive activity
- Transmit or receive activity
- Full duplex
- Collision
- Link established (on) and activity (blink)
- Link established (on) and receive activity (blink)
- Full duplex (on) and collision (blink)

The LED drivers can be configured by use of LED control register 1, LED control register 2, and LED control register 3 (MII registers 27—29).

Table 11. LED

Pin Name	Pin # 128-Pin TQFP	Pin # 84-Pin MLCC	Pin # 68-Pin MLCC	Pin Description	Functional Description
LED_1000	82	49	42	1000Base-T LED	This LED indicates that the device is operating in 1000Base-T mode. Setting can be overridden.
LED_LNK	85	50	43	Link Established LED	This LED indicates that the link is established. Setting can be overridden.
LED_TXRX	71	44	37	General-Purpose LEDs	Set to be off by default.
LED_100	70	43	36		

Hardware Interfaces (continued)

Media-Dependent Interface: Transformer Interface

Table 12. Transformer Interface Signals

Pin Name	Pin # 128-Pin TQFP	Pin # 84-Pin MLCC	Pin # 68-Pin MLCC	Pin Description	Functional Description
TRD[0]+ TRD[0]–	39 41	25 26	19 20	Transmit and Receive Differential Pair 0	Connect this signal pair through a transformer to the media-dependent interface. In 1000Base-T mode, transmit and receive occur simultaneously at TRD[0]±. In 10Base-T and 100Base-TX modes, TRD[0]± are used to transmit when operating in the MDI configuration and to receive when operating in the MDI-X configuration. The PHY automatically determines the appropriate MDI/MDI-X configuration.
TRD[1]+ TRD[1]–	45 47	28 29	22 23	Transmit/ Receive Differential Pair 1	Connect this signal pair through a transformer to the media-dependent interface. In 1000Base-T mode, transmit and receive occurs simultaneously at TRD[1]±. In 10Base-T and 100Base-TX modes, TRD[1]± are used to receive when operating in the MDI configuration and to transmit when operating in the MDI-X configuration. The PHY automatically determines the appropriate MDI/MDI-X configuration.
TRD[2]+ TRD[2]–	54 56	34 35	28 29	Transmit/ Receive Differential Pair 2	Connect this signal pair through a transformer to the media-dependent interface. In 1000Base-T mode, transmit and receive occurs simultaneously at TRD[2]±. In 10Base-T and 100Base-TX modes, TRD[2]± are unused.
TRD[3]+ TRD[3]–	60 62	37 38	31 32	Transmit/ Receive Differential Pair 3	Connect this signal pair through a transformer to the media-dependent interface. In 1000Base-T mode, transmit and receive occurs simultaneously at TRD[3]±. In 10Base-T and 100Base-TX modes, TRD[3]± are unused.
RSET	52	32	26	Analog Reference Resistor	RSET sets an absolute value reference current for the transmitter. Connect this signal to analog ground through a precision 6.34 kΩ 1% resistor.

Hardware Interfaces (continued)

Clocking and Reset

Table 13. Clocking and Reset

Pin Name	Pin # 128-Pin TQFP	Pin # 84-Pin MLCC	Pin # 68-Pin MLCC	Pin Description	Functional Description
CLK_IN	31	22	16	Reference Clock Input	Connect this signal to a 25 MHz clock input (CLK_IN) or a 25 MHz ± 50 ppm tolerance crystal (XTAL_1).
XTAL_1	31	22	16	Reference Crystal Input	
XTAL_2	32	23	17	Reference Crystal Input	Connect this signal to a 25 MHz ± 50 ppm tolerance crystal. Float this signal if an external clock is used (CLK_IN).
SYS_CLK	94	57	50	System Clock	Use this signal to supply a 125 MHz clock to the MAC. By default, the SYS_CLK output is disabled. The SYS_CLK output can be enabled by asserting the SYS_CLK_EN_N pin or via the management interface.
RESET_N	34	24	18	Reset	Drive RESET_N low for 20 µs to initiate a hardware reset. The ET1011C completes all reset operations within 5 ms of this signal returning to a high state. The configuration pins and the physical address configuration are read during a hardware reset.
COMA	25	—	12	Hardware Powerdown	Drive COMA high to initiate a hardware powerdown. The ET1011C completes all reset operations within 5 ms of this signal returning to a low state. All hardware functions are disabled during a hardware powerdown. The configuration pins and the physical address configuration are read during a hardware powerdown.

Hardware Interfaces (continued)

JTAG

The ET1011C has a standard *IEEE* 1149.1 JTAG test interface. The interface provides extensive test and diagnostics capability. It contains internal circuitry that allows the device to be controlled through the JTAG port to provide on-chip, in-circuit emulation.

The JTAG interface is a bidirectional serial interface with its own reset strobe (TRST_N). The reset strobe can be used independently to reset the JTAG state machine but must be used during a power-on reset (see Reset Timing on page 78).

Table 14. JTAG Test Interface

Pin Name	Pin # 128-Pin TQFP	Pin # 84-Pin MLCC	Pin # 68-Pin MLCC	Pin Description	Functional Description
TDI	16	14	7	Test Data Input	This signal is the JTAG serial input. All instructions and scanned data are input using this pin. This pin has an internal pull-up resistor.
TDO	17	15	8	Test Data Output	This signal is the JTAG serial output. Scanned data and status bits are output using this pin. This pin has an internal pull-up resistor.
TCK	10	5	2	Test Clock	This signal is the JTAG serial shift clock. It clocks all of the data that passes through the port on TDI and TDO. This pin has an internal pull-up resistor.
TMS	15	13	6	Test Mode Select	This signal is the JTAG test mode control. This pin has an internal pull-up resistor.
TRST_N	14	12	5	Test Reset (JTAG Reset)	This signal is active-low and causes the JTAG TAP controller to enter the reset state. This pin has an internal pull-down resistor.

Regulator Control

The ET1011C has two on-chip regulator controllers. This allows the device to be powered from a single supply, either 3.3 V or 2.5 V. The on-chip regulator control circuits provide output control voltages that can be used to control two external transistors and thus provide regulated 1.0 V and 2.5 V supplies.

Table 15. Regulator Control Interface

Pin Name	Pin # 128-Pin TQFP	Pin # 84-Pin MLCC	Pin # 68-Pin MLCC	Pin Description	Functional Description
CTRL_1V0	79	47	40	Regulator Control for 1.0 V	This is the regulator output control voltage for the 1.0 V supply. It is used to control an external transistor and thus provide a regulated 1.0 V supply.
CTRL_2V5	78	46	39	Regulator Control for 2.5 V	This is the regulator output control voltage for the 2.5 V supply. It is used to control an external transistor and thus provide a regulated 2.5 V supply.

Hardware Interfaces (continued)

Regulator Control (continued)

The ET1011C digital and analog core operates at 1.0 V. The analog I/O operates at 2.5 V. The digital I/O can operate at either 3.3 V or 2.5 V. The GMII interface operates at 3.3 V and the RGMII interface operates at 2.5 V. The on-chip regulator control allows the device to be operated from a wide variety of external supply combinations. When more than one external supply is available, one or both of the regulator control circuits may be left unused. Table 16 lists example combinations of available external supplies and shows how the on-chip regulator control may be used to provide the required supplies.

Table 16. Supply Voltage Combinations

Available External Supplies	AVDDL	DVDD	AVDDH	VDD_REG[1]	Description
3.3 V only	1.0	1.0	2.5	3.3	Digital I/O can be either 3.3 V or 2.5 V. Regulator control is used to provide 1.0 V and 2.5 V.
2.5 V only	1.0	1.0	2.5	2.5	Digital I/O is 2.5 V. Regulator control is used to provide 1.0 V.
3.3 V and 1.0 V	1.0	1.0	2.5	3.3	Digital I/O can be either 3.3 V or 2.5 V. Regulator control is used to provide 2.5 V.
2.5 V and 1.0 V	1.0	1.0	2.5	2.5	Digital I/O is 2.5 V. Regulator controls are not connected.
3.3 V and 2.5 V	1.0	1.0	2.5	3.3	Digital I/O can be either 3.3 V or 2.5 V. Regulator control is used to provide 1.0 V.
3.3 V, 2.5 V, and 1.0 V	1.0	1.0	2.5	3.3 or 2.5	Digital I/O can be either 3.3 V or 2.5 V. Regulator controls are not connected.

1. Even if the regulator controls are not connected, VDD_REG must be powered.

Power, Ground, and No Connect

Table 17. Power, Ground, and No Connect

Pin Name	Pin Description	Functional Description
VDD_REG	V_{DD}	Regulator 2.5 V or 3.3 V supply.
DVDDIO	V_{DD}	Digital I/O 3.3 V or 2.5 V supply.
DVDD	V_{DD}	Digital core 1.0 V supply.
DVSS	V_{SS}	Digital ground[1].
AVDDH	V_{DD}	Analog power 2.5 V.
AVDDL	V_{DD}	Analog power 1.0 V.
AVSS	V_{SS}	Analog ground[1].
NC	No Connect	Reserved—do not connect.

1. For 84-pin MLCC and 68-pin MLCC, all AVSS and DVSS pins share a common ground pin (exposed pad) in the center of the device.

Cable Diagnostics

The ET1011C has on-chip cable diagnostics. The cable analysis uses two distinct methods for evaluating the cable: link analysis and time domain reflectometry (TDR) analysis. This analysis can be used to detect cable impairments that may be preventing a gigabit link or affecting performance.

When there is a link active, the link analysis can detect cable length, link quality, pair skew, pair swaps (MDI/MDI-X configuration), and polarity reversal. When there is no link, TDR can detect cable faults (open circuit, short circuit), distance to the fault, pair fault is on, cable length, pair skew, and excessive crosstalk. Table 18 summarizes the specifications of the cable diagnostic functions.

Table 18. Cable Diagnostic Functions

Feature	Description	10	100	1000	Term	Unterm	Analysis
Detection of Cable Fault on Any Pair	Cable open	—	—	—	✓	✓	Line Probing
	Cable short	—	—	—	✓	✓	
	Indicate distance to fault	—	—	—	±2 m	±2 m	
	Pair swaps	✓	✓	✓[1]	—	—	Link Analysis
Detect Polarity Reversal	—	✓	—[2]	✓	—	—	Link Analysis
Good Cable with Link	Indicate length	—	±10 m	±10 m	—	—	Link Analysis
Good Cable Without Link	Indicate length	—	—	—	±5 m[3]	±2 m	Line Probing
Pair Skew with Link	Detect excessive, >50 ns	—	—	✓	—	—	Link Analysis
Pair Skew Without Link	Detect excessive, >50 ns	—	—	—	✓[3]	✓	Line Probing
Excessive Crosstalk	Cable quality or split pairs	—	—	—	✓	✓	Line Probing

1. Pair swaps on C and D as well as pairs A and B are reported.
2. Polarity reversal in 100Base-TX is not detected because MLT-3 signaling is polarity insensitive.
3. If the magnitude of the peak reflection is greater than 15% of an open circuit.

Register Description

Register Address Map

Table 19. Register Address Map

Address	Description
0	Control register.
1	Status register.
2	PHY identifier register 1.
3	PHY identifier register 2.
4	Autonegotiation advertisement register.
5	Autonegotiation link partner ability register.
6	Autonegotiation expansion register.
7	Autonegotiation next page transmit register.
8	Link partner next page register.
9	1000Base-T control register.
10	1000Base-T status register.
11—14	Reserved.
15	Extended status register.
16—17	Reserved.
18	PHY control register 2.
19	Loopback control register.
20	RX error counter register.
21	Management interface (MI) control register.
22	PHY configuration register.
23	PHY control register.
24	Interrupt mask register.
25	Interrupt status register.
26	PHY status register.
27	LED control register 1.
28	LED control register 2.
29	LED control register 3.
30	Diagnostics control register.
31	Diagnostics status register (TDR mode).

Table 20. Register Type Definition

Type	Description
LL	Latching low.
LH	Latching high.
R/W	Read write. Register can be read or written.
RO	Read only. Register is read only. Writes to register are ignored.
SC	Self-clearing. Register is self-clearing; if a one is written, the register will automatically clear to zero after the function is completed.

Register Description (continued)

Register Functions/Settings

Table 21. Control Register—Address 0

Control Register					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15	Reset	1 = PHY reset. 0 = Normal operation.	R/W SC	0	1
14	Loopback	1 = Enable loopback. 0 = Disable loopback.	R/W	0	2
13	Speed Selection (LSB)	Bit 6,13. 11 = Reserved. 10 = 1000 Mbits/s. 01 = 100 Mbits/s. 00 = 10 Mbits/s.	R/W	SPEED_1000	3
12	Autonegotiation Enable	1 = Enable autonegotiation process. 0 = Disable autonegotiation process.	R/W	1	4
11	Powerdown	1 = Powerdown. 0 = Normal operation.	R/W	0	—
10	Isolate	1 = Isolate PHY from MII. 0 = Normal operation.	R/W	0	5
9	Restart Autonegotiation	1 = Restart autonegotiation process. 0 = Normal operation.	R/W SC	0	—
8	Duplex Mode	1 = Full duplex. 0 = Half duplex.	R/W	1	6
7	Collision Test	1 = Enable collision test. 0 = Disable collision test.	R/W	0	7
6	Speed Selection (MSB)	See bit 13.	R/W	See bit 13.	3
5:0	Reserved	—	RO	0	—

1. The reset bit is automatically cleared upon completion of the reset sequence. This bit is set to 1 during reset.
2. This is the master enable for digital and analog loopback as defined by the standard. The exact type of loopback is determined by the loopback control register (address 19).
3. The speed selection address 0 bits 13 and 6 may be used to configure the link manually. Setting these bits has no effect unless address 0 bit 12 is clear.
4. When this bit is cleared, the link configuration is determined manually.
5. Setting this bit isolates the PHY from the MII, GMII, or RGMII interfaces.
6. This bit may be used to configure the link manually. Setting this bit has no effect unless address 0 bit 12 is clear.
7. Enables *IEEE* 22.2.4.1.9 collision test.

Register Description (continued)

Register Functions/Settings (continued)

Table 22. Status Register—Address 1

Status Register					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15	100Base-T4	0 = Not 100Base-T4 capable.	RO	0	1
14	100Base-X Full Duplex	1 = 100Base-X full-duplex capable. 0 = Not 100Base-X full-duplex capable.	RO	1	—
13	100Base-X Half Duplex	1 = 100Base-X half-duplex capable. 0 = Not 100Base-X half-duplex capable.	RO	1	—
12	10Base-T Full Duplex	1 = 10Base-T full-duplex capable. 0 = Not 10Base-T full-duplex capable.	RO	1	—
11	10Base-T Half Duplex	1 = 10Base-T half-duplex capable. 0 = Not 10Base-T half-duplex capable.	RO	1	—
10	100Base-T2 Full Duplex	0 = Not 100Base-T2 full-duplex capable.	RO	0	—
9	100Base-T2 Half Duplex	0 = Not 100Base-T2 half-duplex capable.	RO	0	—
8	Extended Status	1 = Extended status information in register 0Fh.	RO	1	—
7	Reserved	—	RO	—	—
6	MF Preamble Suppression	1 = Preamble suppressed management frames accepted.	RO	1	—
5	Autonegotiation Complete	1 = Autonegotiation process complete. 0 = Autonegotiation process not complete.	RO	0	2
4	Remote Fault	1 = Remote fault detected. 0 = No remote fault detected.	RO LH	0	3
3	Autonegotiation Ability	1 = Autonegotiation capable. 0 = Not autonegotiation capable.	RO	1	—
2	Link Status	1 = Link is up. 0 = Link is down.	RO LL	0	4
1	Jabber Detect	1 = Jabber condition detected. 0 = No jabber condition detected.	RO LH	0	—
0	Extended Capability	1 = Extended register capabilities.	RO	1	5

1. The ET1011C does not support 100Base-T4 or 100Base-T2; therefore, these register bits will always be set to zero.
2. Upon completion of autonegotiation, this bit becomes set.
3. This bit indicates that a remote fault has been detected. Once set, it remains set until it is cleared by reading register 1 via the management interface or by PHY reset.
4. This bit indicates that a valid link has been established. Once cleared due to link failure, this bit will remain cleared until register 1 is read via the management interface.
5. Indicates that the PHY provides an extended set of capabilities that may be accessed through the extended register set. For a PHY that incorporates a GMII/RGMII, the extended register set consists of all management registers except registers 0, 1, and 15.

Register Description (continued)

Register Functions/Settings (continued)

Table 23. PHY Identifier Register 1—Address 2

PHY Identifier Register 1					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15:0	PHY Identifier Bits 3:18	Organizationally unique identifier (OUI), bits 3:18.	RO	0x0282	1

Table 24. PHY Identifier Register 2—Address 3

PHY Identifier Register 2					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15:10	PHY Identifier Bits 19:24	Organizationally unique identifier (OUI), bits 19:24.	RO	111100	1
9:4	Model Number	Model number = 1.	RO	000001	—
3:0	Revision Number	Revision number = 4.	RO	0100	—

1. The LSI OUI is 00-05-3D.

Register Description (continued)

Register Functions/Settings (continued)

Table 25. Autonegotiation Advertisement Register—Address 4

Autonegotiation Advertisement Register 1					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15	Next Page	1 = Advertise next page ability supported. 0 = Advertise next page ability not supported.	R/W	0	—
14	Reserved	—	RO	0	—
13	Remote Fault	1 = Advertise remote fault detected. 0 = Advertise no remote fault detected.	R/W	0	—
12	Reserved	—	RO	0	—
11	Asymmetric Pause	1 = Advertise asymmetric pause ability. 0 = Advertise no asymmetric pause ability.	R/W	PAUSE	1
10	Pause Capable	1 = Capable of full-duplex pause operation. 0 = Not capable of pause operation.	R/W	PAUSE	1
9	100Base-T4 Capability	1 = 100Base-T4 capable. 0 = Not 100Base-T4 capable.	R/W	0	2
8	100Base-TX Full-Duplex Capable	1 = 100Base-TX full-duplex capable. 0 = Not 100Base-TX full-duplex capable.	R/W	1	—
7	100Base-TX Half-Duplex Capable	1 = 100Base-TX half-duplex capable. 0 = Not 100Base-TX half-duplex capable.	R/W	1	—
6	10Base-T Full-Duplex Capable	1 = 10Base-T full-duplex capable. 0 = Not 10Base-T full-duplex capable.	R/W	1	—
5	10Base-T Half-Duplex Capable	1 = 10Base-T half-duplex capable. 0 = Not 10Base-T half-duplex capable.	R/W	1	—
4:0	Selector Field	00001 = *IEEE* 802.3 CSMA/CD.	R/W	00001	—

1. Value read from PAUSE on reset.
2. The ET1011C does not support 100Base-T4, so the default value of this register bit is zero.

Note: Any write to this register prior to the completion of autonegotiation is followed by a restart of autonegotiation. Also note that this register is not updated following autonegotiation.

Register Description (continued)

Register Functions/Settings (continued)

Table 26. Autonegotiation Link Partner Ability Register—Address 5

Autonegotiation Link Partner Ability Register					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15	Next page	1 = Link partner has next page ability. 0 = Link partner does not have next page ability.	RO	0	—
14	Acknowledge	1 = Link partner has received link code word. 0 = Link partner has not received link code word.	RO	0	—
13	Remote Fault	1 = Link partner has detected remote fault. 0 = Link partner has not detected remote fault.	RO	0	—
12	Reserved	—	RO	0	—
11	Asymmetric Pause	1 = Link partner desired asymmetric pause. 0 = Link partner does not desire asymmetric pause.	RO	0	—
10	Pause Capable	1 = Link partner capable of full-duplex pause operation. 0 = Link partner is not capable of pause operation.	RO	0	—
9	100Base-T4 Capability	1 = Link partner is 100Base-T4 capable. 0 = Link partner is not 100Base-T4 capable.	RO	0	—
8	100Base-TX Full-Duplex Capable	1 = Link partner is 100Base-TX full-duplex capable. 0 = Link partner is not 100Base-TX full-duplex capable.	RO	0	—
7	100Base-TX Half-Duplex Capable	1 = Link partner is 100Base-TX half-duplex capable. 0 = Link partner is not 100Base-TX half-duplex capable.	RO	0	—
6	10Base-T Full-Duplex Capable	1 = Link partner is 10Base-T full-duplex capable. 0 = Link partner is not 10Base-T full-duplex capable.	RO	0	—
5	10Base-T Half-Duplex Capable	1 = Link partner is 10Base-T half-duplex capable. 0 = Link partner is not 10Base-T half-duplex capable.	RO	0	—
4:0	Protocol Selector Field	Link partner protocol selector field.	RO	0	—

Register Description (continued)

Register Functions/Settings (continued)

Table 27. Autonegotiation Expansion Register—Address 6

Autonegotiation Expansion Register					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15:5	Reserved	—	RO	—	—
4	Parallel Detection Fault	1 = Parallel link fault detected. 0 = Parallel link fault not detected.	RO LH	0	—
3	Link Partner Next Page Ability	1 = Link partner has next page capability. 0 = Link partner does not have next page capability.	RO	0	—
2	Next Page Capability	1 = Local device has next page capability. 0 = Local device does not have next page capability.	RO LH	1	—
1	Page Received	1 = New page has been received from link partner. 0 = New page has not been received.	RO LH	0	—
0	Link Partner Autonegotiation Ability	1 = Link partner has autonegotiation capability. 0 = Link partner does not have autonegotiation capability.	RO	0	—

Table 28. Autonegotiation Next Page Transmit Register—Address 7

Autonegotiation Next Page Transmit Register					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15	Next Page	1 = Additional next pages follow. 0 = Sending last next page.	R/W	0	—
14	Reserved	—	RO	0	—
13	Message Page	1 = Formatted page. 0 = Unformatted page.	R/W	1	—
12	Acknowledge 2	1 = Complies with message. 0 = Cannot comply with message.	R/W	0	—
11	Toggle	1 = Previous value of transmitted link code word was logic zero. 0 = Previous value of transmitted link code word was logic one.	RO	0	—
10:0	Message/ Unformatted Code Field	Next page message code or unformatted data.	R/W	1	—

Register Description (continued)

Register Functions/Settings (continued)

Table 29. Link Partner Next Page Register—Address 8

Link Partner Next Page Register					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15	Next Page	1 = Additional next pages follow. 0 = Sending last next page.	RO	0	—
14	Acknowledge	1 = Acknowledge. 0 = No acknowledge.	RO	0	—
13	Message Page	1 = Formatted page. 0 = Unformatted page.	R/W	0	—
12	Acknowledge 2	1 = Complies with message. 0 = Cannot comply with message.	R/W	0	—
11	Toggle	1 = Previous value of transmitted link code word was logic zero. 0 = Previous value of transmitted link code word was logic one.	RO	0	—
10:0	Message/ Unformatted Code Field	Next page message code or unformatted data.	R/W	0	—

Register Description (continued)

Register Functions/Settings (continued)

Table 30. 1000 Base-T Control Register—Address 9

1000Base-T Control Register					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15:13	Test Mode	000 = Normal mode. 001 = Test mode 1—transmit waveform test. 010 = Test mode 2—master transmit jitter test. 011 = Test mode 3—slave transmit jitter test (slave mode). 100 = Test mode 4—transmit distortion test. 101, 110, 111 = Reserved.	R/W	000	—
12	Master/Slave Configuration Enable	1 = Enable master/slave configuration. 0 = Automatic master/slave configuration.	R/W	0	—
11	Master/Slave Configuration Value	1 = Configure PHY as master. 0 = Configure PHY as slave.	R/W	0	1
10	Port Type	1 = Prefer multiport device (master). 0 = Prefer single-port device (slave).	R/W	0	—
9	Advertise 1000Base-T Full-duplex Capability	1 = Advertise 1000Base-T full-duplex capability. 0 = Advertise no 1000Base-T full-duplex capability.	R/W	SPEED_1000	2
8	Advertise 1000Base-T Half-duplex Capability	1 = Advertise 1000Base-T half-duplex capability. 0 = Advertise no 1000Base-T half-duplex capability.	R/W	SPEED_1000	2
7:0	Reserved	—	RO	—	—

1. Setting this bit has no effect unless address 9, bit 12 is set.
2. Value read from SPEED_1000 pin at reset.

Note: Logically, bits 12:8 can be regarded as an extension of the technology ability field of register 4.

Register Description (continued)

Register Functions/Settings (continued)

Table 31. 1000Base-T Status Register—Address 10

1000Base-T Status Register					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15	Master/ Slave Configu-ration Fault	1 = Master/slave configuration fault detected. 0 = No master/slave configuration fault detected.	RO, LH, SC	0	1
14	Master/Slave Configuration Resolution	1 = Local PHY resolved to master. 0 = Local PHY resolved to slave.	RO	0	2
13	Local Receiver Status	1 = Local receiver okay. 0 = Local receiver not okay.	RO	0	—
12	Remote Receiver Status	1 = Remote receiver okay. 0 = Remote receiver not okay.	RO	0	—
11	Link Partner 1000Base-T Full-duplex Capability	1 = Link partner is capable of 1000Base-T full duplex. 0 = Link partner not 1000Base-T full-duplex capable.	RO	0	3
10	Link Partner 1000Base-T Half-duplex Capability	1 = Link partner is 1000Base-T half-duplex capable. 0 = Link partner not 1000Base-T half-duplex capable.	RO	0	3
9:8	Reserved	—	RO		—
7:0	Idle Error Count	MSB of idle error count.	RO	0	4

1. Once set, this bit remains set until cleared by the following actions:
   - Read of register 10 via the management interface.
   - Reset.
   - Completion of autonegotiation.
   - Enable of autonegotiation.
2. This bit is not valid when bit 15 is set.
3. Note that logically, bits 11:10 may be regarded as an extension of the technology ability field of register 5.
4. These bits contain a cumulative count of the errors detected when the receiver is receiving idles and both local and remote receiver status are OK. The count is held at 255 in the event of overflow and is reset to zero by reading register 10 via the management interface or by reset.

Register Description

Register Functions/Settings (continued)

Table 32. Reserved Registers—Addresses 11—14

Reserved Registers					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15:0	Reserved	—	—	—	—

Table 33. Extended Status Register—Address 15

Extended Status Register					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15	1000Base-X Full-duplex	0 = Not 1000Base-X full-duplex capable.	RO	0	—
14	1000Base-X Half-duplex	0 = Not 1000Base-X half-duplex capable.	RO	0	—
13	1000Base-T Full-duplex	1 = 1000Base-T full-duplex capable. 0 = Not 1000Base-T full-duplex capable.	RO	1	1
12	1000Base-T Half-duplex	1 = 1000Base-T half-duplex capable. 0 = Not 1000Base-T half-duplex capable.	RO	1	—
11:0	Reserved	—	RO	0	—

1. Value is a result of (SPEED_1000) pin at reset.

Table 34. Reserved Registers—Addresses 16—17

Reserved Registers					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15:0	Reserved	—	—	—	—

Register Description (continued)

Register Functions/Settings (continued)

Table 35. PHY Control Register 2—Address 18

PHY Control Register 2					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15	Reserved	—	—	—	—
14	Count False Carrier Events	1 = Rx error counter counts false carrier events. 0 = Rx error counter does not count false carrier events.	R/W	0	1
13	Count Symbol Errors	1 = Rx error counter counts symbol errors. 0 = Rx error counter counts CRC errors.	R/W	0	1
12:11	Reserved	—	—	—	—
10	Automatic MDI/MDI-X	1 = Enable automatic MDI/MDI-X detection. 0 = Disable automatic MDI/MDI-X detection.	R/W	1	—
9	MDI/MDI-X Configuration	1 = Manual MDI-X configuration. 0 = Manual MDI configuration.	R/W	0	See Table 36.
8:3	Reserved	—	—	—	—
2	Enable Diagnostics	1 = Enable diagnostics. 0 = Disable diagnostics.	R/W	0	2
1:0	Reserved	—	—	—	—

1. Count symbol errors (18.13) and count false carrier events (18.14) control the type of errors that the Rx error counter (20.15:0) counts (settings are shown below). The default is to count CRC errors.

Count False Carrier Events	Count Symbol Errors	Rx Error Counter
1	1	Counts symbol errors and false carrier events.
1	0	Counts CRC errors and false carrier events
0	1	Counts symbol errors.
0	0	Counts CRC errors.

2. This bit enables PHY diagnostics, which include IP phone detection and TDR cable diagnostics. It is not recommended to enable this bit in normal operation (when the link is active). This bit does not need to be set for link analysis cable diagnostics.

Register Description (continued)

Register Functions/Settings (continued)

Bit 9, PHY Control Register 2, manually sets the MDI/MDI-X configuration if automatic MDIX is disabled, as indicated below.

Table 36. MDI/MDI-X Configuration

Automatic MDI/MDI-X	MDI/MDI-X Configuration	MDI/MDI-X Mode
1	X	Automatic MDI/MDI-X detection.
0	0	MDI configuration (NIC/DTE).
0	1	MDI-X configuration (switch).

The mapping of the transmitter and receiver to pins for MDI and MDI-X configuration for 10Base-T, 100Base-TX, and 1000Base-T is shown below. Note that even in manual MDI/MDI-X configuration, the PHY automatically detects and corrects for C and D pair swaps.

Table 37. MDI/MDI-X Pin Mapping

Pin	MDI Pin Mapping			MDI-X Pin Mapping		
	10Base-T	100Base-TX	1000Base-T	10Base-T	100Base-TX	1000Base-T
TRD[0]+/–	Transmit +/–	Transmit +/–	Transmit A+/– Receive B+/–	Receive +/–	Receive +/–	Transmit B+/– Receive A+/–
TRD[1]+/–	Receive +/–	Receive +/–	Transmit B+/– Receive A+/–	Transmit +/–	Transmit +/–	Transmit A+/– Receive B+/–
TRD[2]+/–	—	—	Transmit C+/– Receive D+/–	—	—	Transmit D+/– Receive C+/–
TRD[3]+/–	—	—	Transmit D+/– Receive C+/–	—	—	Transmit C+/– Receive D+/–

Register Description (continued)

Register Functions/Settings (continued)

Table 38. Loopback Control Register—Address 19

Loopback Control Register					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15	MII	1 = MII loopback selected. 0 = MII loopback not selected.	R/W	1	—
14:13	Reserved	—	—	—	—
12	All Digital	1 = All digital loopback selected. 0 = All digital loopback not selected.	R/W	0	—
11	Replica	1 = Replica loopback selected. 0 = Replica loopback not selected.	R/W	0	1
10	Line Driver	1 = Line driver loopback selected. 0 = Line driver loopback not selected.	R/W	0	—
9:8	Reserved	—	—	—	—
7	External Cable	1 = External cable loopback enabled. 0 = External cable loopback disabled.	R/W	0	—
6:1	Reserved	—	—	—	—
0	Force Link Status	1 = Force link status okay in MII loopback. 2 = Force link status **not** okay in MII loopback.	R/W	0	2

1. Replica loopback is not available in 10Base-T.
2. This bit can be used to force link status okay during MII loopback. In MII loopback, the link status bit will not be set unless force link status is used. In all other loopback modes, the link status bit will be set when the link comes up.

Loopback Mode Settings

The following table shows how the loopback bit (0.14) and the cable diagnostic mode bit (23.13) should be set for each loopback mode. It also indicates whether the loopback mode sets the link status bit and when the PHY is ready to receive data.

Table 39. Loopback Bit (0.14) and Cable Diagnostic Mode Bit (23.13) Settings for Loopback Mode

Loopback	Bit 0.14 Loopback Required	Bit 23.13 = 1 Cable Diagnostic Mode Required	Bit 26.6 Link Status Set	PHY Ready for Data
MII	Yes	No	19.0	After a few ms
All Digital	Yes	Yes	Yes	Link Status
Replica	Yes	Yes	Yes	Link Status
Line Driver	Yes	Yes	Yes	Link Status
Ext Cable	No	Yes	Yes	Link Status

Register Description (continued)

Register Functions/Settings (continued)

Table 40. RX Error Counter Register—Address 20

RX Error Counter Register					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15:0	Rx Error Counter	16-bit Rx error counter.	RO, SC	0	Reference Register 18 (bits 13 and 14) for error type descriptions

Table 41. Management Interface (MI) Control Register—Address 21

Management Interface (MI) Control Register					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15:3	Reserved	—	—	—	—
2	Ignore 10G Frames	1 = Management frames with ST = <00> are ignored. 0 = Management frames with ST = <00> are treated as wrong frames	R/W	1	—
1	Reserved	—	—	—	—
0	Preamble Suppression Enable	1 = MI preamble is ignored. 0 = MI preamble is required.	R/W	1	—

Register Description (continued)

Register Functions/Settings (continued)

Table 42. PHY Configuration Register—Address 22

PHY Configuration Register					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15	CRS Transmit Enable	1 = Enable CRS on transmit in half-duplex mode. 0 = Disable CRS on transmit.	R/W	0	—
14	Reserved	—	—	—	—
13:12	Transmit FIFO depth (1000Base-T)	00 = ±8. 01 = ±16. 10 = ±24. 11 = ±32.	R/W	01	—
11:10	Automatic Speed Downshift Mode	00 = Disable automatic speed downshift. 10 = 100Base-TX downshift enabled. x1 = 100Base-TX and 10Base-T enabled.	R/W	11	1
9	TBI Detect Select	1 = CRS pin outputs comma detect. 0 = CRS pin outputs link status detect	R/W	0	—
8	TBI Rate Select	1 = Output 125 MHz clock on RX_CLK while COL is held low (full rate). 0 = Output even/odd clocks on RX_CLK/COL	R/W	0	—
7	Alternate Next-Page	1 = Enables manual control of 1000Base-T next pages only. 0 = Normal operation of 1000Base-T next page exchange	R/W	0	—
6	Group MDIO Mode Enable	1 = Enable group MDIO mode. 0 = Disable Group MDIO mode.	R/W	0	—
5	Transmit Clock Enable	1 = Enable output of 1000Base-T transmit clock (TX_CLK pin). 0 = Disable output.	R/W	0	—
4	System Clock Enable	1 = Enable output of 125 MHz reference clock (SYS_CLK pin). 0 = Disable output of 125 MHz reference clock.	R/W	$\overline{\text{SYS\_CLK\_EN\_N}}$	2
3	Reserved	—	—	—	—
2:0	MAC Interface Mode Select	000 = GMII/MII. 001 = TBI. 010 = GMII/MII clocked by GTX_CLK instead of TX_CLK. 011 = Reserved. 100 = RGMII (trace delay). 101 = RTBI (trace delay). 110 = RGMII (DLL delay). 111 = RTBI (DLL delay).	R/W	See bit 23.6 (next page) and Note 1, Table 10, page 30.	3

1. If automatic speed downshift is enabled and the PHY fails to autonegotiate at 1000Base-T, the PHY will fall back to attempt connection at 100Base-TX and, subsequently, 10Base-T. This cycle will repeat. If the link is broken at any speed, the PHY will restart this process by reat-tempting connection at the highest possible speed (e.g., 1000Base-T).
2. Value is read from inversion of SYS_CLK_EN_N at reset.
3. For the 68-pin MLCC, only RGMII and RTBI modes/options are supported.

Register Description (continued)

Register Functions/Settings (continued)

Table 43. PHY Control Register—Address 23

PHY Control Register					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15	IP Phone Detected	1 = IP phone detected. 0 = IP phone not detected.	RO	0	1
14	IP Phone Detect Enable	1 = Enable automatic IP phone detect. 0 = Disable automatic IP phone detect.	R/W, SC	0	2
13	Cable Diagnostic Mode	1 = Link analysis mode. 0 = TDR mode.	R/W	1	3
12:11	Automatic Speed Downshift Attempts Before Downshift	00 = 1. 01 = 2. 10 = 3. 11 = 4.	R/W	11	—
10:7	Reserved	—	—	—	—
6	Alternative RGMII TXC DLL Delay	1 = TXC DLL delay in RGMII mode is opposite of RXC. 0 = TXC DLL delay in RGMII mode is same as RXC.	R/W	See Note 1, Table 10, page 30.	4
5	Jabber (10Base-T)	1 = Disable jabber. 0 = Normal operation.	R/W	0	—
4	SQE (10Base-T)	1 = Enable heartbeat. 0 = Disable heartbeat.	R/W	0	—
3	TP_LOOPBACK (10Base-T)	1 = Disable TP loopback during half-duplex. 0 = Normal operation.	R/W	1	—
2	Preamble Generation Enable	1 = Enable preamble generation for 10Base-T. 0 = Disable preamble generation for 10Base-T.	R/W	1	—
1	Reserved	—	—	—	—
0	Force Interrupt	1 = Assert MDINT_N pin. 0 = Deassert MDINT_N pin.	R/W	0	—

1. This bit is only valid when the PHY is in PHY standby mode (26.15 = 1) and after the IP phone detect enable bit (23.14) has been set and has self-cleared to indicate that the IP phone detection algorithm has completed.
2. Setting this bit enables the automatic IP phone detection algorithm and clears the IP phone detected bit (23.15). Diagnostics must be enabled (18.2 = 1), cable diagnostic TDR mode must be selected (23.13 = 0), and the PHY must be in PHY standby mode (26.15 = 1) to do IP phone detection. IP phone detect enable self-clears when the IP phone detection algorithm is complete, the result is then indicated in IP phone detected.
3. This bit sets the cable diagnostics mode. The default is link analysis mode wherein the PHY brings up a link with a remote partner. For analysis of cable faults, the PHY can be put in TDR mode. In TDR mode, the PHY will not respond to link pulses from a remote link partner and will not bring up a link.
4. This bit allows independent control over TXC and RXC DLL delay. Settings are shown below:

RGMII Mode		Delay		Description
22.2:0	**23.6**	**TXC**	**RXC**	
10x	0	0 ns	0 ns	RGMII (trace delay).
11x	0	2 ns	2 ns	RGMII (TXC and RXC DLL delay).
10x	1	2 ns	0 ns	RGMII (TXC DLL delay).
11x	1	0 ns	2 ns	RGMII (RXC DLL delay).

Register Description (continued)

Register Functions/Settings (continued)

Table 44. Interrupt Mask Register—Address 24

Interrupt Mask Register					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15:11	Reserved	—	—	—	—
10	TDR/IP Phone	1 = Interrupt enabled. 0 = Interrupt disabled.	R/W	0	—
9	MDIO Sync Lost	1 = Interrupt enabled. 0 = Interrupt disabled.	R/W	0	—
8	Autonegotiation Status Change	1 = Interrupt enabled. 0 = Interrupt disabled.	R/W	0	—
7	CRC Errors	1 = Interrupt enabled. 0 = Interrupt disabled.	R/W	0	—
6	Next Page Received	1 = Interrupt enabled. 0 = Interrupt disabled.	R/W	0	—
5	Error Counter Full	1 = Interrupt enabled. 0 = Interrupt disabled.	R/W	0	—
4	FIFO Overflow/ Underflow	1 = Interrupt enabled. 0 = Interrupt disabled.	R/W	0	—
3	Receive Status Change	1 = Interrupt enabled. 0 = Interrupt disabled.	R/W	0	—
2	Link Status Change	1 = Interrupt enabled. 0 = Interrupt disabled.	R/W	0	—
1	Automatic Speed Downshift	1 = Interrupt enabled. 0 = Interrupt disabled.	R/W	0	—
0	MDINT_N Enable	1 = MDINT_N enabled[1]. 0 = MDINT_N disabled.	R/W	0	—

1. MDINT_N is asserted (active-low) if MII interrupt pending = 1.

Register Description (continued)

Register Functions/Settings (continued)

Table 45. Interrupt Status Register—Address 25

Interrupt Status Register					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15:11	Reserved	—	—	—	—
10	TDR/IP Phone	1 = Event has completed. 0 = Event has not completed.	RO, LH	0	—
9	MDIO Sync Lost	1 = Event has occurred. 0 = Event has not occurred.	RO, LH	0	1
8	Autonegotiation Status Change	1 = Event has occurred. 0 = Event has not occurred.	RO, LH	0	—
7	CRC Errors	1 = Event has occurred. 0 = Event has not occurred.	RO, LH	0	—
6	Next Page Received	1 = Event has occurred. 0 = Event has not occurred.	RO, LH	0	—
5	Error Counter Full	1 = Event has occurred. 0 = Event has not occurred.	RO, LH	0	—
4	FIFO Overflow/ Underflow	1 = Event has occurred. 0 = Event has not occurred.	RO, LH	0	—
3	Receive Status Change	1 = Event has occurred. 0 = Event has not occurred.	RO, LH	0	—
2	Link Status Change	1 = Event has occurred. 0 = Event has not occurred.	RO, LH	0	—
1	Automatic Speed Downshift	1 = Event has occurred. 0 = Event has not occurred.	RO, LH	0	—
0	MII Interrupt Pending	1 = Interrupt pending. 0 = No interrupt pending.	RO, LH	0	2

1. If the management frame preamble is suppressed (MF preamble suppression, register 0, bit 6), it is possible for the PHY to lose synchronization if there is a glitch at the interface. The PHY can recover if a single frame with a preamble is sent to the PHY. The MDIO sync lost interrupt can be used to detect loss of synchronization and, thus, enable recovery.
2. An event has occurred and the corresponding interrupt mask bit is enabled (set = 1).

Register Description (continued)

Register Functions/Settings (continued)

Table 46. PHY Status Register—Address 26

PHY Status Register					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15	PHY in Standby Mode	1 = PHY in standby mode. 0 = PHY **not** in standby mode.	R0	0	1
14:13	Autonegotiation Fault Status	10 = Master/slave autonegotiation fault. 01 = Parallel detect autonegotiation fault. 00 = No autonegotiation fault.	RO	00	—
12	Autonegotiation Status	1 = Autonegotiation is complete. 0 = Autonegotiation not complete.	RO	0	—
11	MDI-X Status	1 = MDI-X configuration. 0 = MDI configuration.	RO	0	—
10	Polarity Status	1 = Polarity is normal (10Base-T only). 0 = Polarity is inverted (10Base-T only).	RO	1	—
9:8	Speed Status	11 = Undetermined. 10 = 1000Base-T. 01 = 100Base-TX. 00 = 10Base-T.	RO	11	—
7	Duplex Status	1 = Full duplex. 0 = Half duplex.	RO	0	—
6	Link Status	1 = Link is up. 0 = Link is down.	RO	0	—
5	Transmit Status	1 = PHY is transmitting a packet. 0 = PHY is not transmitting a packet.	RO	0	—
4	Receive Status	1 = PHY is receiving a packet. 0 = PHY is not receiving a packet.	RO	0	—
3	Collision Status	1 = Collision is occurring. 0 = Collision not occurring.	RO	0	—
2	Autonegotiation Enabled	1 = Both partners have autonegotiation enabled. 0 = Both partners do not have autonegotiation enabled.	RO	0	—
1	PAUSE Enabled	1 = Link partner advertised PAUSE mode enabled. 0 = Link partner advertised PAUSE mode disabled.	RO	0	—
0	Asymmetric Direction	1 = Link partner advertised direction is symmetric. 0 = Link partner advertised that direction is asymmetric.	RO	0	—

1. This bit indicates that the PHY is in standby mode and is ready to perform IP phone detection or TDR cable diagnostics. The PHY enters standby mode when cable diagnostic TDR mode is selected (23.13 = 0) and the link is dropped. A software reset (0.15) or software power down (0.11) can be used to force the link to drop.

Register Description (continued)

Register Functions/Settings (continued)

Table 47. LED Control Register 1—Address 27

LED Control Register 1					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15	Two-Color Mode LED_1000/LED_100	1 = Two-color mode for LED_1000 and LED_100. 0 = Normal mode for LED_1000 and LED_100.	R/W	0	1
14	Two-Color Mode LED_LINK/LED_TXRX	1 = Two-color mode for LED_LINK and LED_TXRX. 0 = Normal mode for LED_LINK and LED_TXRX.	R/W	0	1
13	LED_TXRX Extended Modes	1 = Extended modes for LED_TXRX. 0 = Standard modes for LED_TXRX.	R/W	0	2
12	LED_LINK Extended Modes	1 = Extended modes for LED_LINK. 0 = Standard modes for LED_LINK.	R/W	0	2
11	LED_100 Extended Modes	1 = Extended modes for LED_100. 0 = Standard modes for LED_100.	R/W	0	2
10	LED_1000 Extended Modes	1 = Extended modes for LED_1000. 0 = Standard modes for LED_1000.	R/W	0	2
9:8	Reserved	—	—	—	—
7:4	LED Blink Pattern Pause	LED blink pattern pause cycles.	R/W	0x0	—
3:2	LED Pulse Duration	00 = Stretch LED events to 28 ms. 01 = Stretch LED events to 60 ms. 10 = Stretch LED events to 100 ms. 11 = Reserved.	R/W	00	—
1	Reserved	—	—	—	—
0	Pulse Stretch 0	1 = Enable pulse stretching of LED functions: transmit activity, receive activity, and collision. 0 = Disable pulse stretching of LED functions: transmit activity, receive activity, and collision.	R/W	1	—

1. If two-color mode is enabled for pair LED_LINK and LED_TXRX, the signal output for LED_LINK is equal to (LED_LINK and $\overline{\text{LED\_TXRX}}$). For the case where LED_LINK and LED_TXRX are not mutually exclusive (e.g., duplex and collision), this mode can simplify the external circuitry because it ensures either LED_LINK or LED_TXRX is on, and not both at the same time. The same rule applies to pair LED_1000 and LED_100.
2. The LED function is programmed using this bit and register 28.

Register Description (continued)

Register Functions/Settings (continued)

Table 48. LED Control Register 2—Address 28

LED Control Register 2					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15:12	LED_TXRX	As per 11:8.	RW	1111	—
11:8	LED_LINK	**Standard modes** 0000 = 1000Base-T. 0001 = 100Base-TX. 0010 = 10Base-T. 0011 = 1000Base-T on, 100Base-TX blink. 0100 = Link established. 0101 = Transmit. 0110 = Receive. 0111 = Transmit or receive activity. 1000 = Full duplex. 1001 = Collision. 1010 = Link established (on) and activity (blink). 1011 = Link established (on) and receive (blink). 1100 = Full duplex (on) and collision (blink). 1101 = Blink. 1110 = On. 1111 = Off. **Extended modes** 0000 = 10Base-T or 100Base-TX. 0001 = Reserved. 0010 = Reserved. 0011 = Reserved. 0100 = 1000Base-T (on) and activity (blink). 0101 = 10Base-T or 100Base-TX (on) and activity (blink). 011x = Reserved.	R/W	0100	—
7:4	LED_100	As per 11:8.	RW	1111	—
3:0	LED_1000	As per 11:8.	R/W	0000	—

Table 49. LED Control Register 3—Address 29

LED Control Register 3					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15:14	LED Blink Pattern Address	Select LED blink pattern register set. 00 = Select register set for LED_LINK. 01 = Select register set for LED_TXRX. 10 = Select register set for LED_1000. 11 = Select register set for LED_100.	R/W	00	—
13:8	LED Blink Pattern Frequency	LED blink pattern clock frequency divide ratio.	R/W	0x1f	1
7:0	LED Blink Pattern	LED blink pattern.	R/W	0x55	1

1. The default pattern is a 512 ms blink.

Register Description (continued)

Register Functions/Settings (continued)

Table 50. Diagnostics Control Register (TDR Mode)—Address 30

Diagnostics Control Register (TDR Mode)					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15:14	TDR Request	11 = Automatic TDR analysis in progress. 10 = Single-pair TDR analysis in progress. 01 = TDR analysis complete, results valid. 00 = TDR analysis complete, results invalid.	R/W	00	1
13:12	TDR Tx Dim	Transmit dimension for single-pair TDR analysis. 00 = TDR transmit on pair A. 01 = TDR transmit on pair B. 10 = TDR transmit on pair C. 11 = TDR transmit on pair D.	R/W	00	2
11:10	TDR Rx Dim	Receive dimension for single-pair TDR analysis. 00 = TDR receive on pair A. 01 = TDR receive on pair B. 10 = TDR receive on pair C. 11 = TDR receive on pair D.	R/W	00	2
9:2	Distance to Fault	Distance to open or short fault.	R/W	0	3, 4
1:0	Reserved	—	—	—	—

1. Automatic TDR analysis is enabled by setting TDR request to {11}. All 10 combinations of pairs are analyzed in sequence, and the results are available in registers 30 and 31. TDR analysis for a single-pair combination can be enabled by setting TDR request to {10}. Diagnostics must be enabled (18.2 = 1), cable diagnostic TDR must be mode selected (23.13 = 0), and the PHY must be in PHY standby mode (26.15 = 1) to perform TDR operations. Bit 15 self-clears when the TDR operation is complete. When TDR is complete, bit 14 indicates whether the results are valid.
2. TDR transmit and receive dimensions are only valid for single-pair TDR analysis. They are ignored for automatic TDR analysis when all 10 pair combinations are analyzed.
3. This is the distance to an open, short, or strong impedance mismatch fault on the chosen pair for single-pair TDR analysis. For automatic TDR analysis, this returns the distance to the last open, short, or strong impedance mismatch fault found. The automatic algorithm searches for faults in the order of short between C and D, B and D, B and C, A and D, A and C, A and B; and faults on pair D, pair C, pair B, and pair A. If there is no fault, the result will be 0xff and should be ignored.
4. The 8-bit integer value can be linearly converted to distance in meters. The value 0x08 (or less) corresponds to a distance of 0 m, and the value 0xfe corresponds to a distance of 200 m (180 m for Cat-3 cable). The following equation can be used to convert the integer value to meters:

   $$\text{distance (m)} = 1.179 \times (x - 8) \times \text{NVP}$$

   Where,
   NVP = normalized velocity of propagation (typically 0.69 for CAT5, CAT5e, and CAT6; 0.62 for CAT3). For CAT5/5e/6 cable, a simple approximation (accurate to 0.1%) is (x – 8) x 13/16.

Register Description (continued)

Register Functions/Settings (continued)

Table 51. Diagnostics Status Register (TDR Mode)—Address 31

Diagnostics Status Register (TDR Mode)					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15:14	TDR Fault Type Pair A (or fault type for single pair combination)	11 = Short found on pair A. 10 = Open found on pair A. 01 = Strong impedance mismatch found on pair A. 00 = Good termination found on pair A.	R/W	00	1
13:12	TDR Fault Type Pair B	11 = Short found on pair B. 10 = Open found on pair B. 01 = Strong impedance mismatch found on pair B. 00 = Good termination found on pair B.	R/W	00	—
11:10	TDR Fault Type Pair C	11 = Short found on pair C. 10 = Open found on pair C. 01 = Strong impedance mismatch found on pair C. 00 = Good termination found on pair C.	R/W	00	—
9:8	TDR Fault Type Pair D	11 = Short found on pair D. 10 = Open found on pair D. 01 = Strong impedance mismatch found on pair D. 00 = Good termination found on pair D.	R/W	00	—
7	Short Between Pairs A and B	1 = Short between pairs A and B. 0 = No short between pairs A and B.	R/W	0	—
6	Short Between Pairs A and C	1 = Short between pairs A and C. 0 = No short between pairs A and C.	R/W	0	—
5	Short Between Pairs A and D	1 = Short between pairs A and D. 0 = No short between pairs A and D.	R/W	0	—
4	Short Between Pairs B and C	1 = Short between pairs B and C. 0 = No short between pairs Band C.	R/W	0	—
3	Short Between Pairs B and D	1 = Short between pairs B and D. 0 = No short between pairs B and D.	R/W	0	—
2	Short Between Pairs C and D	1 = Short between pairs C and D. 0 = No short between pairs C and D.	R/W	0	—
1:0	Reserved	—	—	—	—

1. For automatic TDR analysis, this returns the fault type on pair A. For single-pair TDR analysis, this returns the fault type on the pair combination under test, i.e., as specified in the TDR Tx Dim and Rx Dim (30.13:12 and 30.11:10, respectively).

Register Description (continued)

Register Functions/Settings (continued)

Table 52. Diagnostics Control Register (Link Analysis Mode)—Address 30

Diagnostics Control Register (Link Analysis Mode)					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15:12	Reserved	—	—	—	—
11	Pair Swap on Pairs C and D	1 = Pairs C and D are swapped (1000Base-T only). 0 = Pairs C and D are not swapped (1000Base-T only).	R/W	0	See Table 53.
10:5	Cable Length	Cable length when link is active.	R/W	0	1
4	Polarity on Pair D	1 = Polarity on pair D is normal (1000Base-T only). 0 = Polarity on pair D is inverted (1000Base-T only).	R/W	0	—
3	Polarity on Pair C	1 = Polarity on pair C is normal (1000Base-T only). 0 = Polarity on pair C is inverted (1000Base-T only).	R/W	0	—
2	Polarity on Pair B	1 = Polarity on pair B is normal (1000Base-T only). 0 = Polarity on pair B is inverted (1000Base-T only).	R/W	0	—
1	Polarity on Pair A	1 = Polarity on pair A is normal (1000Base-T only). 0 = Polarity on pair A is inverted (1000Base-T only).	R/W	0	—
0	Excessive Pair Skew	1 = Excessive pair skew (1000Base-T only). 0 = Not excessive pair skew (1000Base-T only).	R/W	0	2

1. This is the cable length estimate when the link is active (maximum of 155 m). The values of 0x00 to 0x1f correspond to 0 m—155 m in 5 m increments. The values of 0x20 to 0x3e are reserved for future use, e.g., cable lengths of 160 m—315 m. The result may be invalid for a 10Base-T link. If the result is invalid, a value of 0x3f is returned.
2. Excessive pair skew is detected by determining that the scrambler has not acquired. It is possible for other scrambler acquisition errors to be mistaken for excessive pair skew.

The following table shows the mapping of the transmitter and receiver for MDI and MDI-X configuration for 1000Base-T when pairs C and D are not swapped and are swapped.

Table 53. MDI/MDI-X Configuration for 1000Base-T with C and D Swapped/Not Swapped

Pin	**Pair C and D Are Not Swapped**		**Pair C and D Are Swapped**	
	MDI Configuration	**MDI-X Configuration**	**MDI Configuration**	**MDI-X Configuration**
TDR_[0:7]_[0]+/–	Transmit A+/– Receive B+/–	Transmit B+/– Receive A+/–	Transmit A+/– Receive B+/–	Transmit B+/– Receive A+/–
TDR_[0:7]_[1]+/–	Transmit B+/– Receive A+/–	Transmit A+/– Receive B+/–	Transmit B+/– Receive A+/–	Transmit A+/– Receive B+/–
TDR_[0:7]_[2]+/–	Transmit C+/– Receive D+/–	Transmit D+/– Receive C+/–	Transmit C+/– Receive C+/–	Transmit D+/– Receive D+/–
TDR_[0:7]_[3]+/–	Transmit D+/– Receive C+/–	Transmit C+/– Receive D+/–	Transmit D+/– Receive D+/–	Transmit C+/– Receive C+/–

Electrical Specifications

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operations sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Table 54. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage (2.5 V analog)	AV_{DDH}	—	4.2	V
Supply Voltage (1.0 V analog)	AV_{DDL}	—	1.2	V
Supply Voltage (3.3 V/2.5 V digital)	DV_{DDIO}	—	4.2	V
Supply Voltage (1.0 V digital)	V_{DD}	—	1.2	V
ESD Protection	V_{ESD}	—	2000	V
Storage Temperature	T_{STORE}	–40	125	°C

Recommended Operating Conditions

Table 55. ET1011C Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (2.5 V analog)	AV_{DDH}	2.38	2.5	2.62	V
Supply Voltage (1.0 V analog)[1]	AV_{DDL}	0.95	1.0 or 1.1	1.15	V
Supply Voltage (3.3 V digital)[2]	DV_{DDIO}	3.14	3.3	3.46	V
Supply Voltage (2.5 V digital)[2]	DV_{DDIO}	2.38	2.5	2.62	V
Supply Voltage (1.0 V digital)[1]	V_{DD}	0.95	1.0 or 1.1	1.15	V
Ambient Operating Temperature—Commercial	T_A	0	—	70	°C
Ambient Operating Temperature—Industrial	T_A	–40	—	85	°C
Maximum Junction Temperature	T_J	0	—	125	°C
Thermal Characteristics, 128 TQFP (JDEC 3 in. x 4.5 in. 4-layer PCB):	 T_{JB} T_{JC} ψ_{JT}	 — — —	 29 33 1	 — — —	°C/W
0 m/s airflow	T_{JA}	—	37	—	
1 m/s airflow	T_{JA}	—	32	—	
2.5 m/s airflow	T_{JA}	—	30	—	
Thermal Characteristics, 84-pin MLCC and 68-pin MLCC (JDEC 3 in. x 4.5 in. 4-layer PCB):	 T_{JB} T_{JC} ψ_{JT}	 — — —	 10 3 1	 — — —	°C/W
0 m/s Airflow	T_{JA}	—	24	—	
1 m/s Airflow	T_{JA}	—	23		
2.5 m/s Airflow	T_{JA}	—	21	—	

1. For the 128-pin TQFP package operating over the industrial temperature range, the maximum voltage is reduced from 1.15 V to 1.05. V. The center tap voltage range is changed to 1.8V only.
2. The part can operate at either 3.3 V (typically for an GMII interface) or 2.5 V (typically for an RGMII interface).

Electrical Specifications (continued)

Device Electrical Characteristics

Device electrical characteristics refer to the behavior of the device under specified conditions imposed on the user for proper operation of the device. Unless otherwise noted, the parameters below are valid for the conditions described in the previous section, Recommended Operating Conditions.

Table 56. Device Characteristics—3.3 V Digital I/O Supply (DV_{DDIO})

Parameter	Symbol	Min	Typ	Max	Unit
Input Low Voltage (GMII input pins)	V_{IL}	–0.3	—	0.8	V
Input Low Voltage (all other digital input pins)	V_{IL}	–0.3	—	0.8	V
Input High Voltage (GMII input pins)	V_{IH}	2.0	—	3.6	V
Input High Voltage (all other digital input pins)	V_{IH}	2.0	—	3.6	V
Output Low Voltage (GMII output pins)	V_{OL}	—	—	0.4	V
Output Low Voltage (all other digital output pins)	V_{OL}	—	—	0.4	V
Output High Voltage (GMII output pins)	V_{OH}	2.4	—	—	V
Output High Voltage (all other digital output pins)	V_{OH}	2.4	—	—	V
Differential Output Voltage (analog MDI pins 1000Base-T)	V_{ODIFF}	0.67	0.75	0.82	V
Differential Output Voltage (analog MDI pins 100Base-TX)	V_{ODIFF}	0.95	1.0	1.05	V
Differential Output Voltage (analog MDI pins 10Base-T)	V_{ODIFF}	2.2	2.5	2.8	V
Bias Voltage	V_{BIAS}	—	1.2	—	V

Table 57. Device Characteristics—2.5 V Digital I/O Supply (DV_{DDIO})

Parameter	Symbol	Min	Typ	Max	Unit
Input Low Voltage (GMII input pins)	V_{IL}	–0.3	—	0.7	V
Input Low Voltage (all other digital input pins)	V_{IL}	–0.3	—	0.7	V
Input High Voltage (GMII input pins)	V_{IH}	1.7	—	2.8	V
Input High Voltage (all other digital input pins)	V_{IH}	1.7	—	2.8	V
Output Low Voltage (GMII output pins)	V_{OL}	—	—	0.4	V
Output Low Voltage (all other digital output pins)	V_{OL}	—	—	0.4	V
Output High Voltage (GMII output pins)	V_{OH}	2.0	—	—	V
Output High Voltage (all other digital output pins)	V_{OH}	2.0	—	—	V
Differential Output Voltage (analog MDI pins 1000Base-T)	V_{ODIFF}	0.67	0.75	0.82	V
Differential Output Voltage (analog MDI pins 100Base-TX)	V_{ODIFF}	0.95	1.0	1.05	V
Differential Output Voltage (analog MDI pins 10Base-T)	V_{ODIFF}	2.2	2.5	2.8	V
Bias Voltage	V_{BIAS}	—	1.2	—	V

Electrical Specifications (continued)

Device Electrical Characteristics (continued)

Table 58. ET1011C Current Consumption GMII 1000Base-T

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage (2.5 V analog)	I_{AVDDH}	Tx/Rx random data	—	59	—	mA
Supply Voltage (1.0 V analog)	I_{AVDDL}	Tx/Rx random data	—	192	—	mA
Supply Voltage (3.3 V digital)	I_{DVDDIO}	Tx/Rx random data	—	42	—	mA
Supply Voltage (1.0 V digital)	I_{VDD}	Tx/Rx random data	—	148	—	mA
Center Tap Voltage (1.8 V analog)	I_{CTAP}	Tx/Rx random data	—	163	—	mA

Table 59. ET1011C Current Consumption GMII 100Base-TX

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage (2.5 V analog)	I_{AVDDH}	Tx/Rx random data	—	20	—	mA
Supply Voltage (1.0 V analog)	I_{AVDDL}	Tx/Rx random data	—	76	—	mA
Supply Voltage (3.3 V digital)	I_{DVDDIO}	Tx/Rx random data	—	27	—	mA
Supply Voltage (1.0 V digital)	I_{VDD}	Tx/Rx random data	—	29	—	mA
Center Tap Voltage (1.8 V analog)	I_{CTAP}	Tx/Rx random data	—	41	—	mA

Table 60. ET1011C Current Consumption GMII 10Base-T

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage (2.5 V analog)	I_{AVDDH}	Tx/Rx random data	—	26	—	mA
Supply Voltage (1.0 V analog)	I_{AVDDL}	Tx/Rx random data	—	76	—	mA
Supply Voltage (3.3 V digital)	I_{DVDDIO}	Tx/Rx random data	—	19	—	mA
Supply Voltage (1.0 V digital)	I_{VDD}	Tx/Rx random data	—	15	—	mA
Center Tap Voltage (1.8 V analog)	I_{CTAP}	Tx/Rx random data	—	57	—	mA

Electrical Specifications (continued)

Device Electrical Characteristics (continued)

Table 61. ET1011C Current Consumption GMII 10Base-T Idle

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage (2.5 V analog)	I_{AVDDH}	Idle	—	26	—	mA
Supply Voltage (1.0 V analog)	I_{AVDDL}	Idle	—	76	—	mA
Supply Voltage (3.3 V digital)	I_{DVDDIO}	Idle	—	15	—	mA
Supply Voltage (1.0 V digital)	I_{VDD}	Idle	—	13	—	mA
Center Tap Voltage (1.8 V analog)	I_{CTAP}	Idle	—	1	—	mA

Table 62. ET1011C Current Consumption RGMII 1000Base-T

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage (2.5 V analog)	I_{AVDDH}	Tx/Rx random data	—	59	—	mA
Supply Voltage (1.0 V analog)	I_{AVDDL}	Tx/Rx random data	—	192	—	mA
Supply Voltage (2.5 V digital)	I_{DVDDIO}	Tx/Rx random data	—	24	—	mA
Supply Voltage (1.0 V digital)	I_{VDD}	Tx/Rx random data	—	148	—	mA
Center Tap Voltage (1.8 V analog)	I_{CTAP}	Tx/Rx random data	—	163	—	mA

Table 63. ET1011C Current Consumption RGMII 100Base-TX

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage (2.5 V analog)	I_{AVDDH}	Tx/Rx random data	—	20	—	mA
Supply Voltage (1.0 V analog)	I_{AVDDL}	Tx/Rx random data	—	76	—	mA
Supply Voltage (2.5 V digital)	I_{DVDDIO}	Tx/Rx random data	—	10	—	mA
Supply Voltage (1.0 V digital)	I_{VDD}	Tx/Rx random data	—	29	—	mA
Center Tap Voltage (1.8 V analog)	I_{CTAP}	Tx/Rx random data	—	41	—	mA

Electrical Specifications (continued)

Device Electrical Characteristics (continued)

Table 64. ET1011C Current Consumption RGMII 10Base-T

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage (2.5 V analog)	I_{AVDDH}	Tx/Rx random data	—	26	—	mA
Supply Voltage (1.0 V analog)	I_{AVDDL}	Tx/Rx random data	—	76	—	mA
Supply Voltage (2.5 V digital)	I_{DVDDIO}	Tx/Rx random data	—	7	—	mA
Supply Voltage (1.0 V digital)	I_{VDD}	Tx/Rx random data	—	15	—	mA
Center Tap Voltage (1.8 V analog)	I_{CTAP}	Tx/Rx random data	—	57	—	mA

Table 65. ET1011C Current Consumption RGMII 10Base-T Idle

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage (2.5 V analog)	I_{AVDDH}	Idle	—	26	—	mA
Supply Voltage (1.0 V analog)	I_{AVDDL}	Idle	—	76	—	mA
Supply Voltage (2.5 V digital)	I_{DVDDIO}	Idle	—	7	—	mA
Supply Voltage (1.0 V digital)	I_{VDD}	Idle	—	13	—	mA
Center Tap Voltage (1.8 V analog)	I_{CTAP}	Idle	—	1	—	mA

Timing Specification

GMII 1000Base-T Transmit Timing (128-Pin TQFP and 84-Pin MLCC Only)

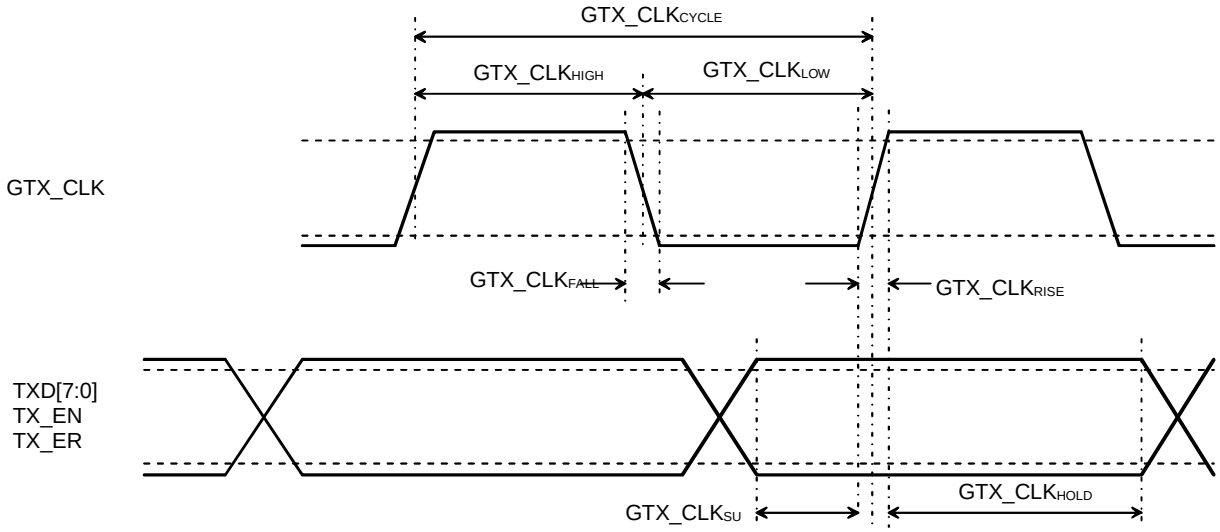


Figure 15. GMII 1000Base-T Transmit Timing

Table 66. GMII 1000Base-T Transmit Timing

Symbol	Parameter	Min	Typ	Max	Unit
GTX_CLK_{CYCLE}	GTX_CLK Cycle Time	7.5	—	8.5	ns
GTX_CLK_{HIGH}	GTX_CLK High Time	2.5	—	—	ns
GTX_CLK_{LOW}	GTX_CLK Low Time	2.5	—	—	ns
GTX_CLK_{RISE}	GTX_CLK Rise Time	—	—	1.0	ns
GTX_CLK_{FALL}	GTX_CLK Fall Time	—	—	1.0	ns
GTX_CLK_{SU}	GMII Input Signal Setup Time to GTX_CLK	2.0	—	—	ns
GTX_CLK_{HOLD}	GMII Input Signal Hold Time to GTX_CLK	0.0	—	—	ns

Timing Specifications (continued)

GMII 1000Base-T Receive Timing (128-Pin TQFP and 84-Pin MLCC Only)

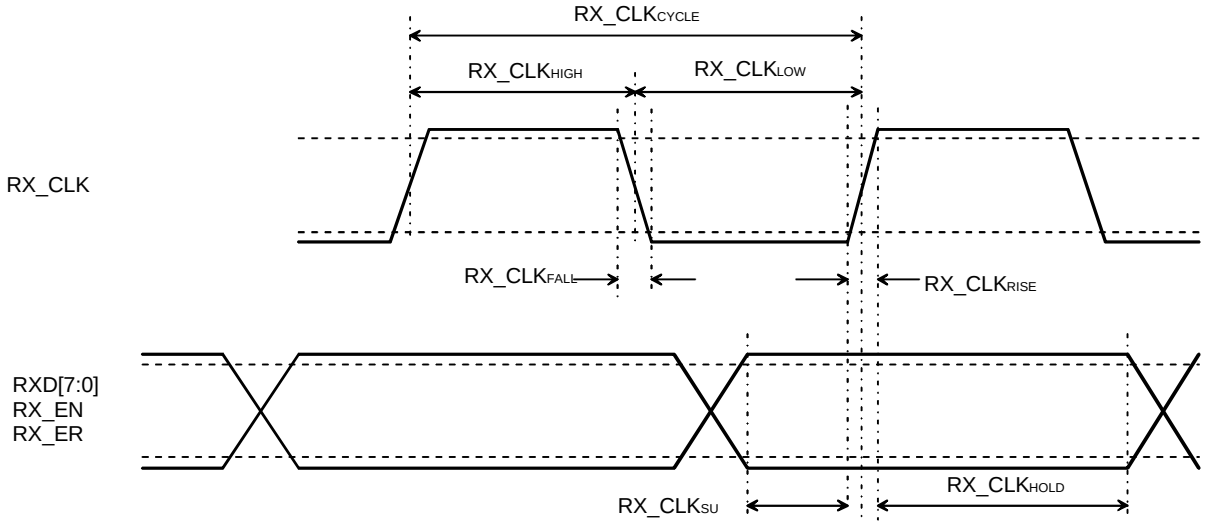


Figure 16. GMII 1000Base-T Receive Timing

Table 67. GMII 1000Base-T Receive Timing

Symbol	Parameter	Min	Typ	Max	Unit
RX_CLKCYCLE	RX_CLK Cycle Time	7.5	8.0	—	ns
RX_CLKHIGH	RX_CLK High Time	2.5	—	—	ns
RX_CLKLOW	RX_CLK Low Time	2.5	—	—	ns
RTX_CLKRISE	RX_CLK Rise Time	—	—	1.0	ns
RX_CLKFALL	RX_CLK Fall Time	—	—	1.0	ns
RX_CLKSU	GMII Output Signal Setup Time to RX_CLK	2.5	—	—	ns
RX_CLKHOLD	GMII Output Signal Hold Time to RX_CLK	0.5	—	—	ns

Timing Specifications (continued)

RGMII 1000Base-T Transmit Timing

Trace Delay

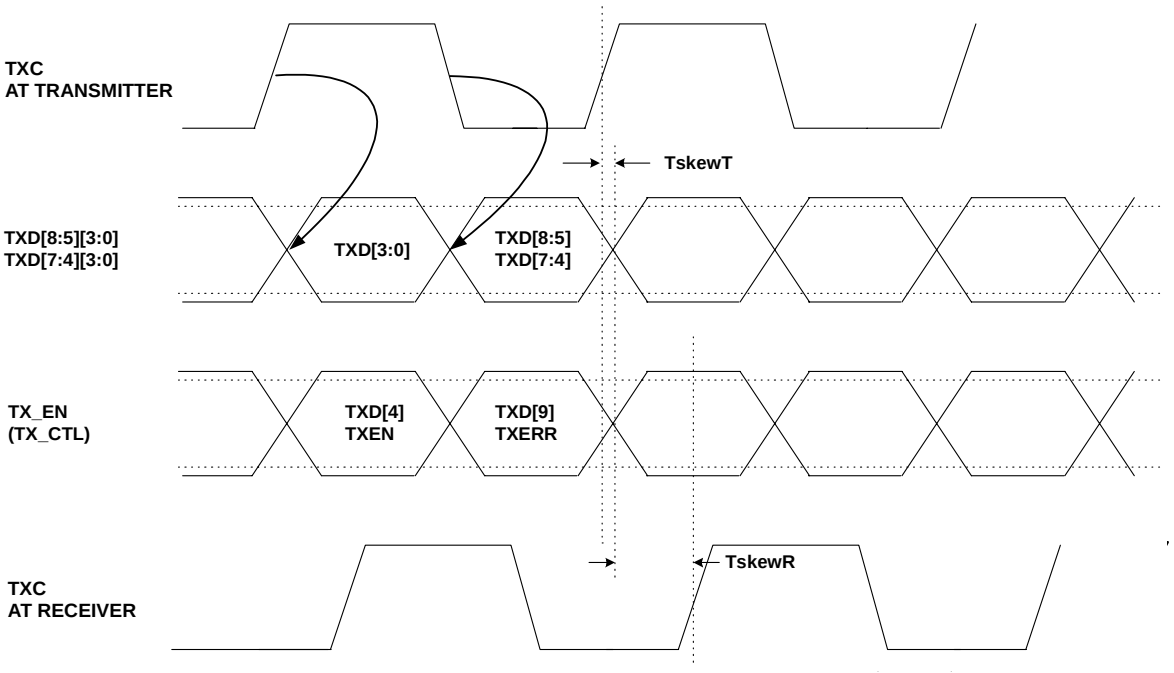


Figure 17. RGMII 1000Base-T Transmit Timing—Trace Delay

Table 68. RGMII 1000Base-T Transmit Timing

Symbol	Parameter	Min	Typ	Max	Unit
TskewT	Data to Clock Output Skew (at transmitter)—Trace Delay[1]	–500	0	500	ps
TskewR	Data to Clock Input Skew (at receiver)—Trace Delay[1]	1	1.8	2.6	ns
Tcyc	Clock Cycle Duration[2]	7.2	8	8.8	ns
Duty_G	Duty Cycle for Gigabit[3]	45	50	55	%
Duty_T	Duty Cycle for 10Base-T/100Base-TX[3]	40	50	60	%
Tr/Tf	Rise/Fall Time (20%—80%)	—	—	0.75	ns

1. This implies that PCB design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns and less than 2.0 ns will be added to the associated clock signal. To enable internal delay, see MII register 22 bits 2:0.
2. For 10Base-T and 100Base-TX, Tcyc scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
3. Duty cycle may be shrunk/stretched during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three Tcyc of the lowest speed transitioned between.

Timing Specifications (continued)

Internal Delay

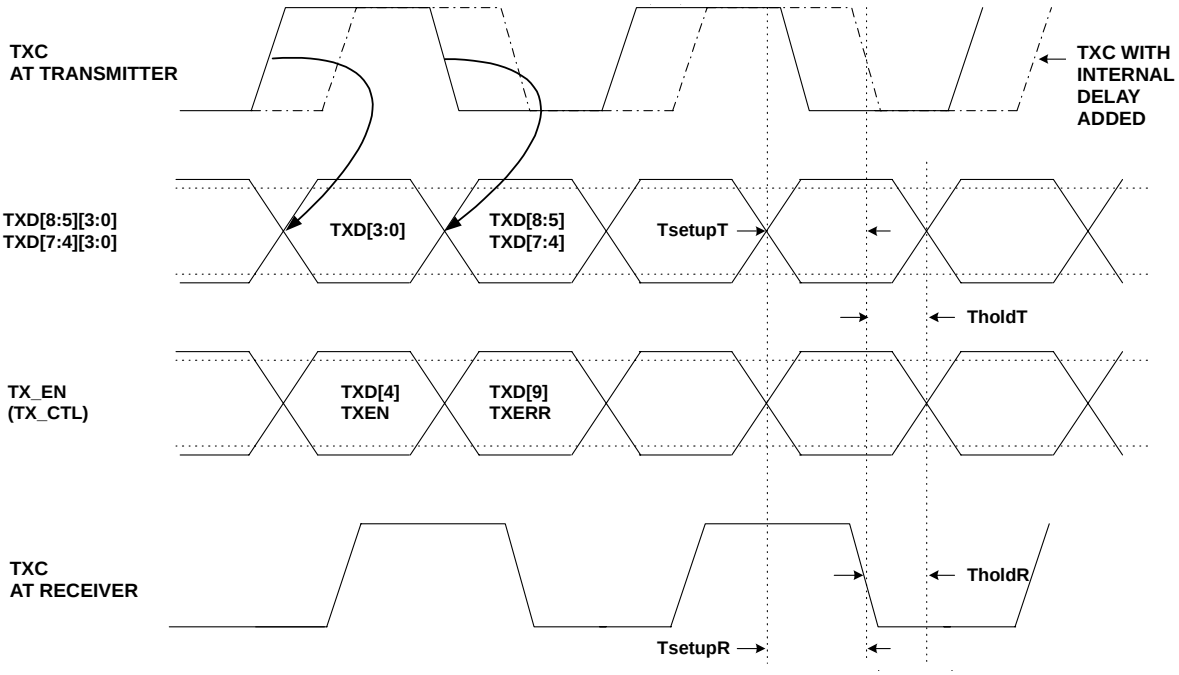


Figure 18. RGMII 1000Base-T Transmit Timing—Internal Delay

Table 69. RGMII 1000Base-T Transmit Timing

Symbol	Parameter	Min	Typ	Max	Unit
TsetupT	Data to Clock Output Setup (at transmitter—integrated delay)[1]	1.2	2.0	—	ns
TholdT	Clock to Data Output Hold (at transmitter—integrated delay)[1]	1.2	2.0	—	ns
TsetupR	Data to Clock Input Setup (at receiver—integrated delay)[1]	1.0	2.0	—	ns
TholdR	Data to Clock Input Hold (at receiver—integrated delay)[1]	1.0	2.0	—	ns
Tcyc	Clock Cycle Duration[2]	7.2	8	8.8	ns
Duty_G	Duty Cycle for Gigabit[3]	45	50	55	%
Duty_T	Duty Cycle for 10Base-T/100Base-TX[3]	40	50	60	%
Tr/Tf	Rise/Fall Time (20%—80%)	—	—	0.75	ns

1. The PHY uses internal delay to compensate by delaying both incoming and outgoing clocks by ~2.0 ns.
2. For 10Base-T and 100Base-TX, Tcyc scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
3. Duty cycle may be shrunk/stretched during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three Tcyc of the lowest speed transitioned between.

Timing Specifications (continued)

RGMII 1000Base-T Receive Timing

Trace Delay

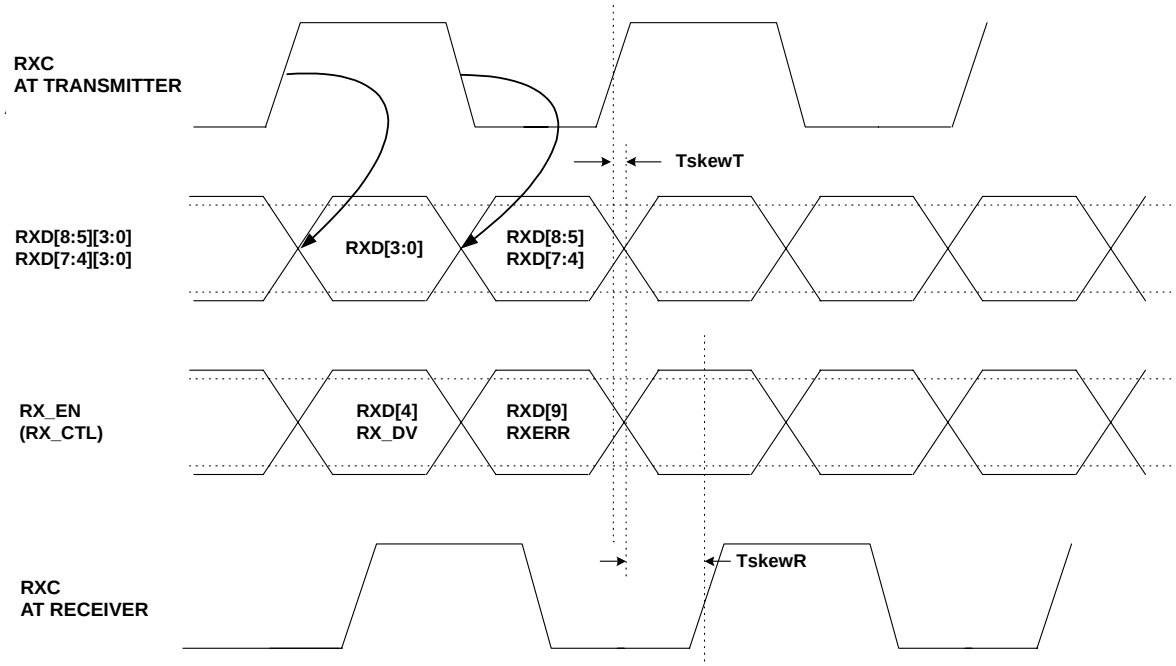


Figure 19. RGMII 1000Base-T Receive Timing—Trace Delay

Table 70. RGMII 1000Base-T Receive Timing

Symbol	Parameter	Min	Typ	Max	Unit
TskewT	Data to Clock Output Skew (at transmitter)—Trace Delay[1]	–500	0	500	ps
TskewR	Data to Clock Input Skew (at receiver)—Trace Delay[1]	1	1.8	2.6	ns
Tcyc	Clock Cycle Duration[2]	7.2	8	8.8	ns
Duty_G	Duty Cycle for Gigabit[3]	45	50	55	%
Duty_T	Duty Cycle for 10Base-T/100Base-TX[3]	40	50	60	%
Tr/Tf	Rise/Fall Time (20%—80%)	—	—	0.75	ns

1. This implies that PCB design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns and less than 2.0 ns will be added to the associated clock signal. To enable internal delay, see MII register 22 bits 2:0.
2. For 10Base-T and 100Base-TX, Tcyc scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
3. Duty cycle may be shrunk/stretched during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three Tcyc of the lowest speed transitioned between.

Timing Specifications (continued)

Internal Delay

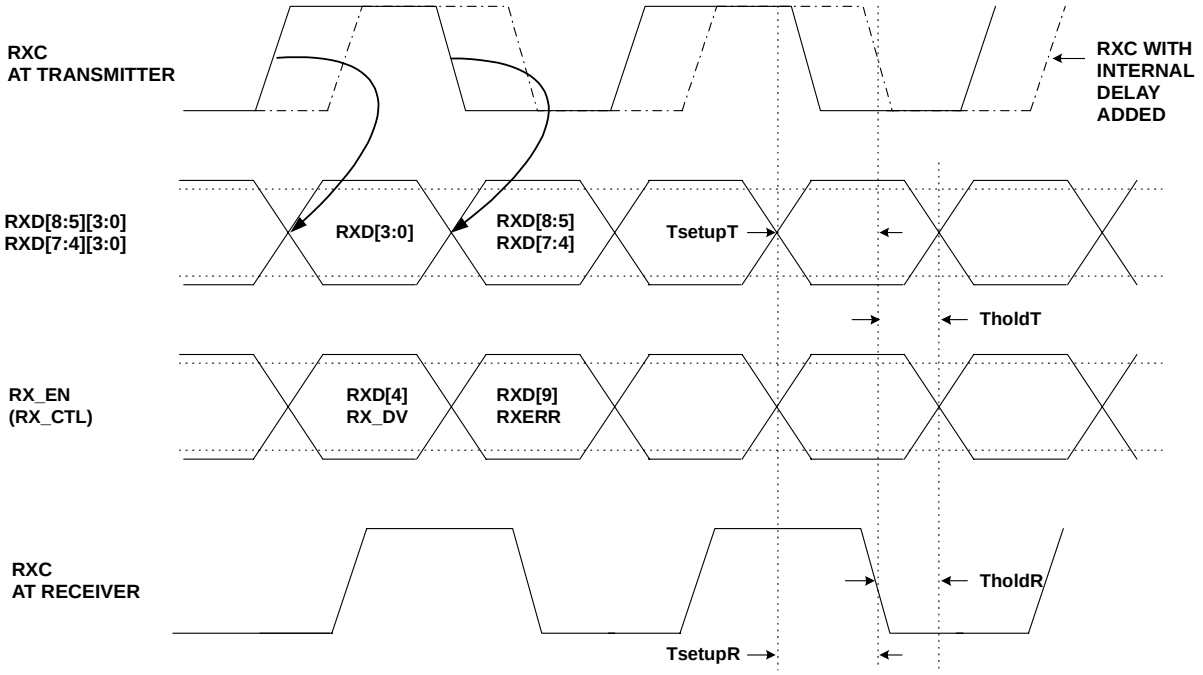


Figure 20. RGMII 1000Base-T Receive Timing—Internal Delay

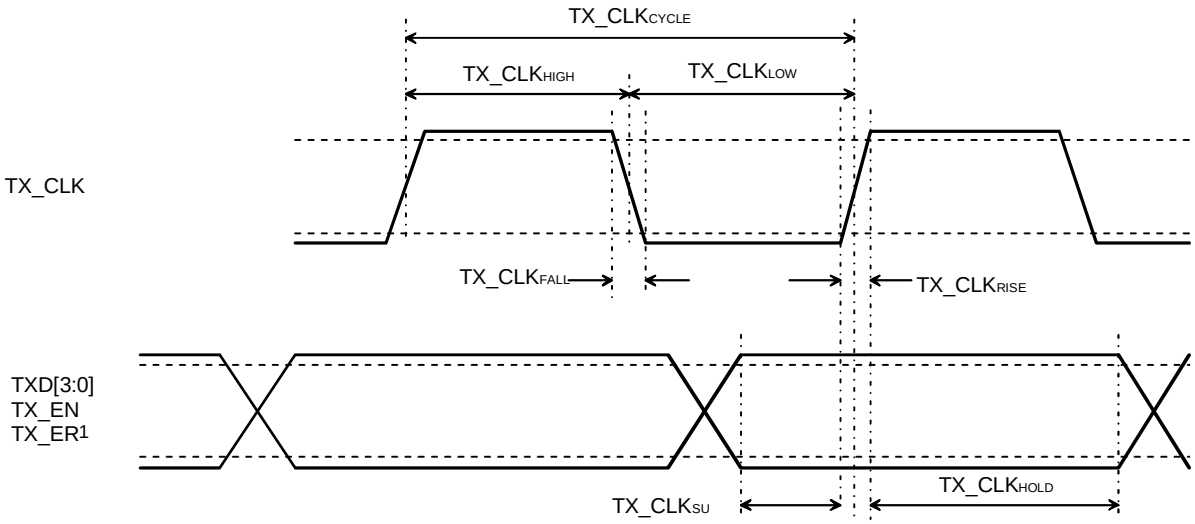
Table 71. RGMII 1000Base-T Receive Timing

Symbol	Parameter	Min	Typ	Max	Unit
TsetupT	Data to Clock Output Setup (at transmitter—integrated delay)[1]	1.2	2.0	—	ns
TholdT	Clock to Data Output Hold (at transmitter—integrated delay)[1]	1.2	2.0	—	ns
TsetupR	Data to Clock Input Setup (at receiver—integrated delay)[1]	1.0	2.0	—	ns
TholdR	Data to Clock Input Hold (at receiver—integrated delay)[1]	1.0	2.0	—	ns
Tcyc	Clock Cycle Duration[2]	7.2	8	8.8	ns
Duty_G	Duty Cycle for Gigabit[3]	45	50	55	%
Duty_T	Duty Cycle for 10Base-T/100Base-TX[3]	40	50	60	%
Tr/Tf	Rise/Fall Time (20%—80%)	—	—	0.75	ns

1. The PHY uses internal delay to compensate by delaying both incoming and outgoing clocks by ~2.0 ns.
2. For 10Base-T and 100Base-TX, Tcyc scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
3. Duty cycle may be shrunk/stretched during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three Tcyc of the lowest speed transitioned between.

Timing Specifications (continued)

MII 100Base-TX Transmit Timing



1. TX_ER is not available on the 68-pin MLCC.

Figure 21. MII 100Base-TX Transmit Timing

Table 72. MII 100Base-TX Transmit Timing

Symbol	Parameter	Min	Typ	Max	Unit
TX_CLKCYCLE	TX_CLK Cycle Time	—	40	—	ns
TX_CLKHIGH	TX_CLK High Time	—	20	—	ns
TX_CLKLOW	TX_CLK Low Time	—	20	—	ns
TX_CLKRISE	TX_CLK Rise Time	—	—	5	ns
TX_CLKFALL	TX_CLK Fall Time	—	—	5	ns
TX_CLKSU	MII Input Signal Setup Time to TX_CLK	15	—	—	ns
TX_CLKHOLD	MII Input Signal Hold Time to TX_CLK	0	—	—	ns

Timing Specifications (continued)

MII 100Base-TX Receive Timing

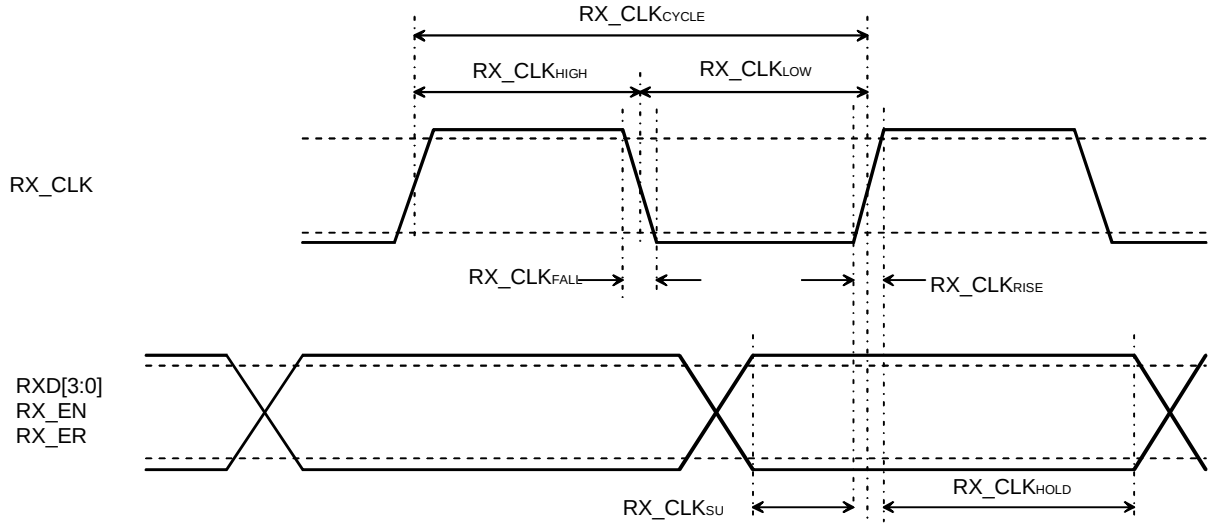


Figure 22. MII 100Base-TX Receive Timing

Table 73. MII 100Base-TX Receive Timing

Symbol	Parameter	Min	Typ	Max	Unit
RX_CLKCYCLE	RX_CLK Cycle Time	—	40	—	ns
RX_CLKHIGH	RX_CLK High Time	—	20	—	ns
RX_CLKLOW	RX_CLK Low Time	—	20	—	ns
RTX_CLKRISE	RX_CLK Rise Time	—	1	—	ns
RX_CLKFALL	RX_CLK Fall Time	—	1	—	ns
RX_CLKSU	MII Output Signal Setup Time to RX_CLK	10	—	—	ns
RX_CLKHOLD	MII Output Signal Hold Time to RX_CLK	10	—	—	ns

Timing Specifications (continued)

MII 10Base-T Transmit Timing

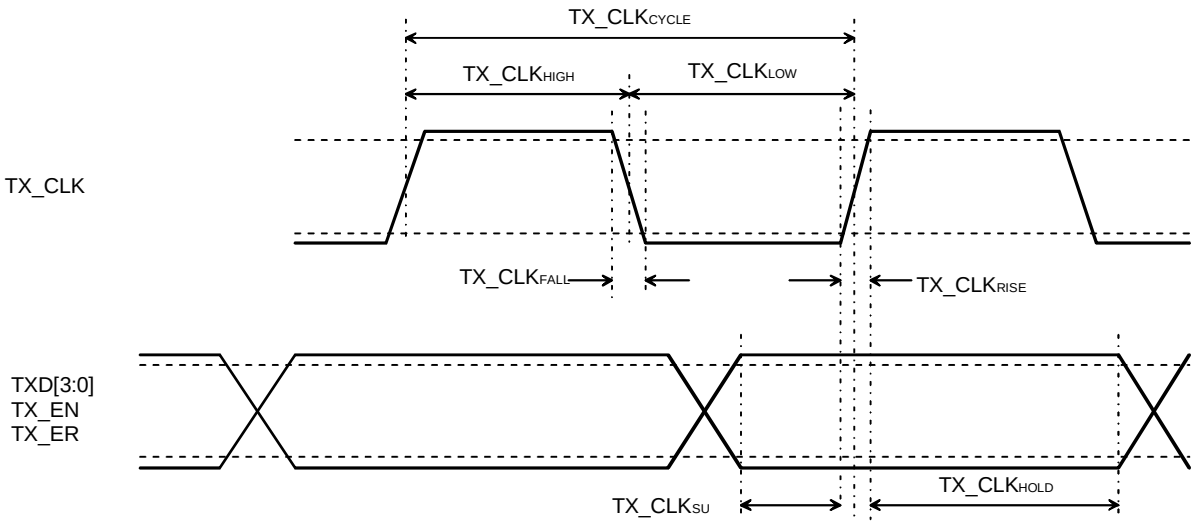


Figure 23. MII 10Base-T Transmit Timing

Table 74. MII 10Base-T Transmit Timing

Symbol	Parameter	Min	Typ	Max	Unit
TX_CLKCYCLE	TX_CLK Cycle Time	—	400	—	ns
TX_CLKHIGH	TX_CLK High Time	—	200	—	ns
TX_CLKLOW	TX_CLK Low Time	—	200	—	ns
TX_CLKRISE	TX_CLK Rise Time	—	1	—	ns
TX_CLKFALL	TX_CLK Fall Time	—	1	—	ns
TX_CLKSU	MII Input Signal Setup Time to TX_CLK	15	—	—	ns
TX_CLKHOLD	MII Input Signal Hold Time to TX_CLK	0	—	—	ns

Timing Specifications (continued)

MII 10Base-T Receive Timing

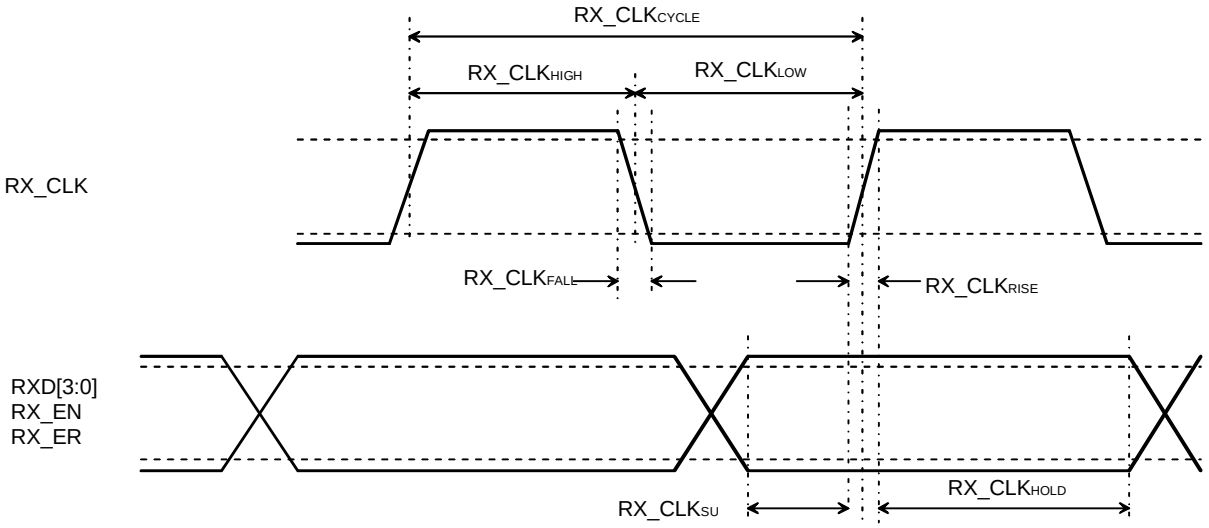


Figure 24. MII 10Base-T Receive Timing

Table 75. MII 10Base-T Receive Timing

Symbol	Parameter	Min	Typ	Max	Unit
RX_CLKCYCLE	RX_CLK Cycle Time	—	400	—	ns
RX_CLKHIGH	RX_CLK High Time	—	200	—	ns
RX_CLKLOW	RX_CLK Low Time	—	200	—	ns
RTX_CLKRISE	RX_CLK Rise Time	—	1	—	ns
RX_CLKFALL	RX_CLK Fall Time	—	1	—	ns
RX_CLKSU	MII Output Signal Setup Time to RX_CLK	10	—	—	ns
RX_CLKHOLD	MII Output Signal Hold Time to RX_CLK	10	—	—	ns

Timing Specifications (continued)

Serial Management Interface Timing

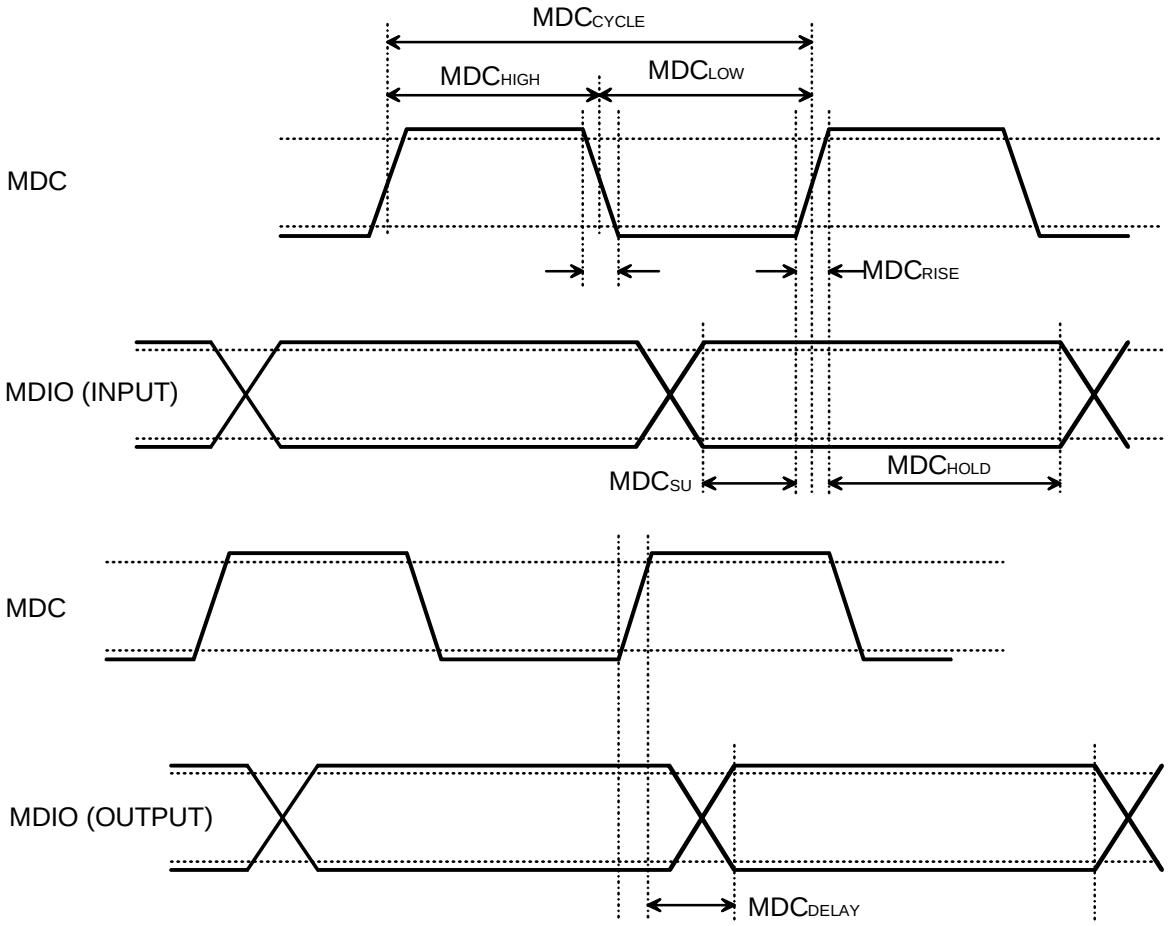


Figure 25. Serial Management Interface Timing

Table 76. Serial Management Interface Timing

Symbol	Parameter	Min	Typ	Max	Unit
MDC_{CYCLE}	MDC Cycle Time	100	—	—	ns
MDC_{HIGH}	MDC High Time	40	—	—	ns
MDC_{LOW}	MDC Low Time	40	—	—	ns
MDC_{RISE}	MDC Rise Time	—	—	5	ns
MDC_{FALL}	MDC Fall Time	—	—	5	ns
MDC_{SU}	MDIO Signal Setup Time to MDC	10	—	—	ns
MDC_{HOLD}	MDIO Signal Hold Time to MDC	10	—	—	ns
MDC_{DELAY}	MDIO Delay Time from MDC	—	—	80	ns

Timing Specifications (continued)

Reset Timing

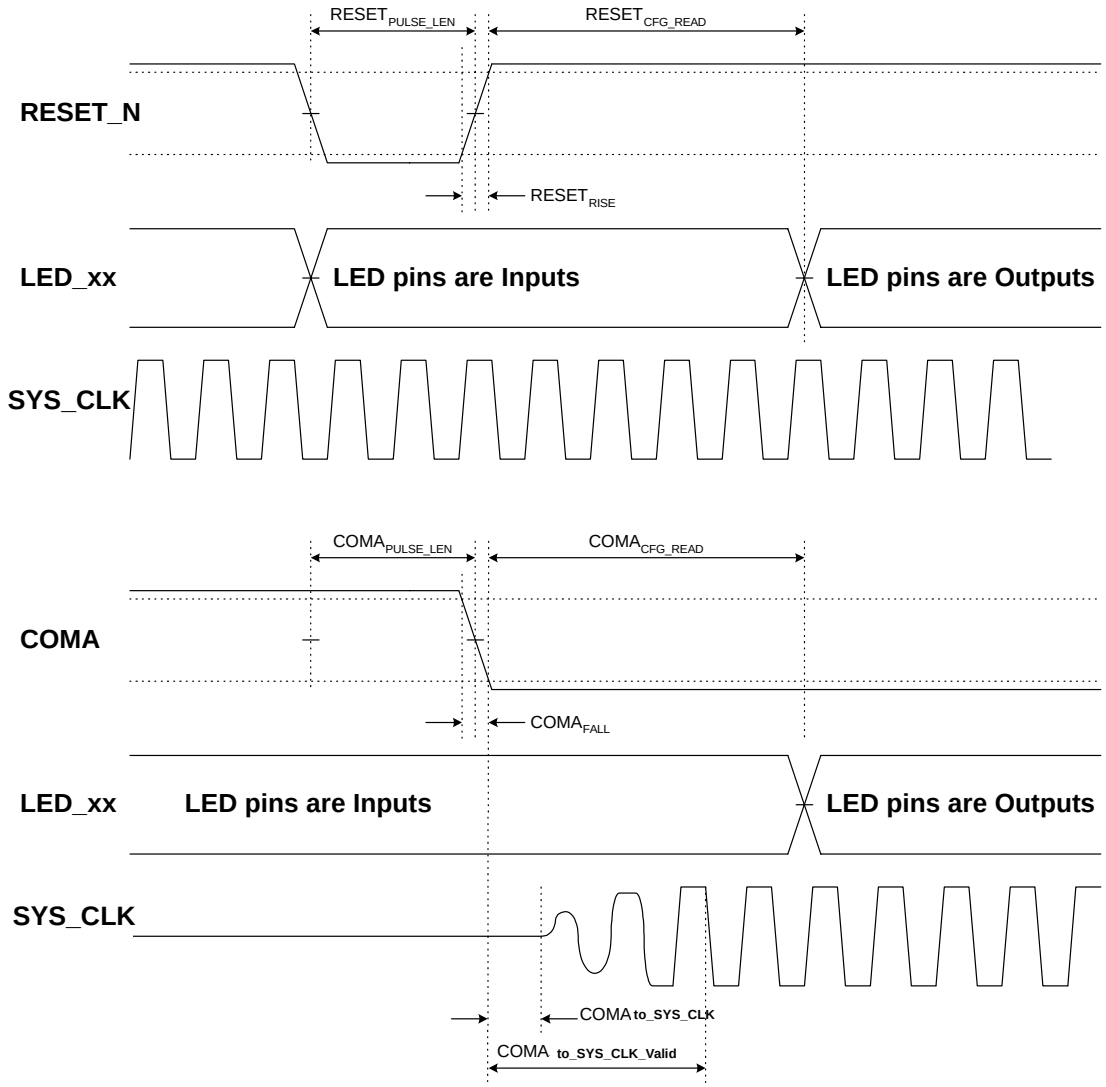


Figure 26. Reset Timing

Table 77. Reset Timing

Symbol	Parameter	Min	Typ	Max	Unit
$RESET_{PULSE\_LEN}$	RESET_N Pulse Length	20	—	—	µs
$RESET_{RISE}$	RESET_N Rise Time	—	1.0	—	ns
$RESET_{CFG\_READ}$	RESET_N Deassertion to Configuration Read	—	—	5.0	ms
$COMA_{PULSE\_LEN}$	COMA Pulse Length	20	—	—	µs
$COMA_{FALL}$	COMA Fall Time	—	1.0	—	ns
$COMA_{TO\_SYS\_CLK}$	COMA Deassertion to SYS_CLK	—	1.0	—	µs
$COMA_{TO\_SYS\_CLK\_VALID}$	COMA Deassertion to SYS_CLK Valid	—	—	4.2	ms
$COMA_{CFG\_READ}$	COMA Deassertion to Configuration Read	—	—	5.0	ms

Timing Specifications (continued)

Clock Timing

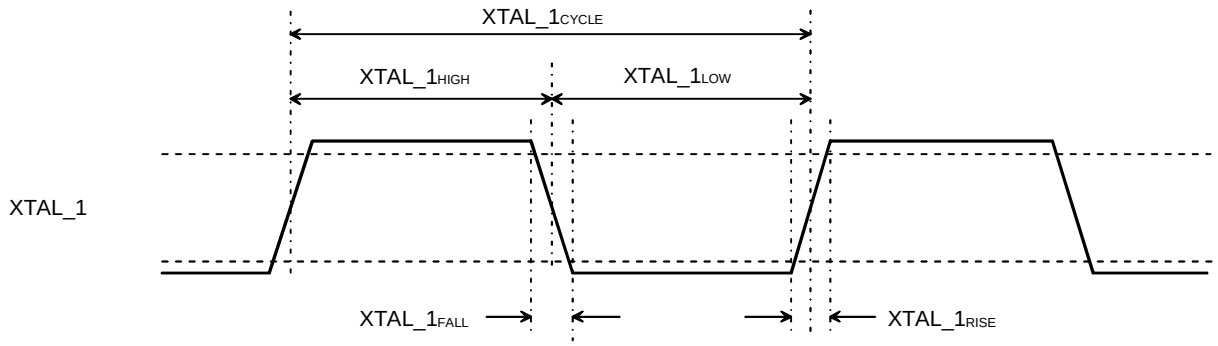


Figure 27. Clock Timing

Table 78. Clock Timing

Symbol	Parameter	Min	Typ	Max	Unit
XTAL_1CYCLE	XTAL_1 Cycle Time	39.998	40	40.002	ns
XTAL_1HIGH	XTAL_1 High Time	15	20	25	ns
XTAL_1LOW	XTAL_1 Low Time	15	20	25	ns
XTAL_1RISE	XTAL_1 Rise Time	—	—	3	ns
XTAL_1FALL	XTAL_1 Fall Time	—	—	3	ns
—	XTAL_1 Input Clock Jitter (RMS)	—	—	20	ps
—	XTAL_1 Input Clock Frequency	—	25	—	MHz
—	XTAL_1 Input Clock Accuracy	—	—	50	ppm

Timing Specifications (continued)

JTAG Timing

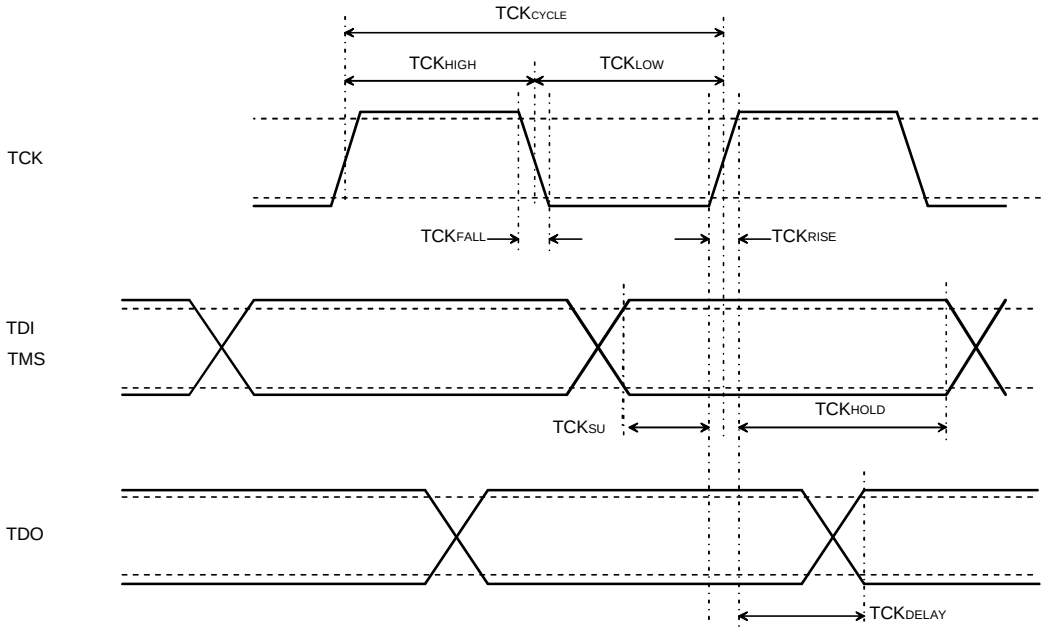


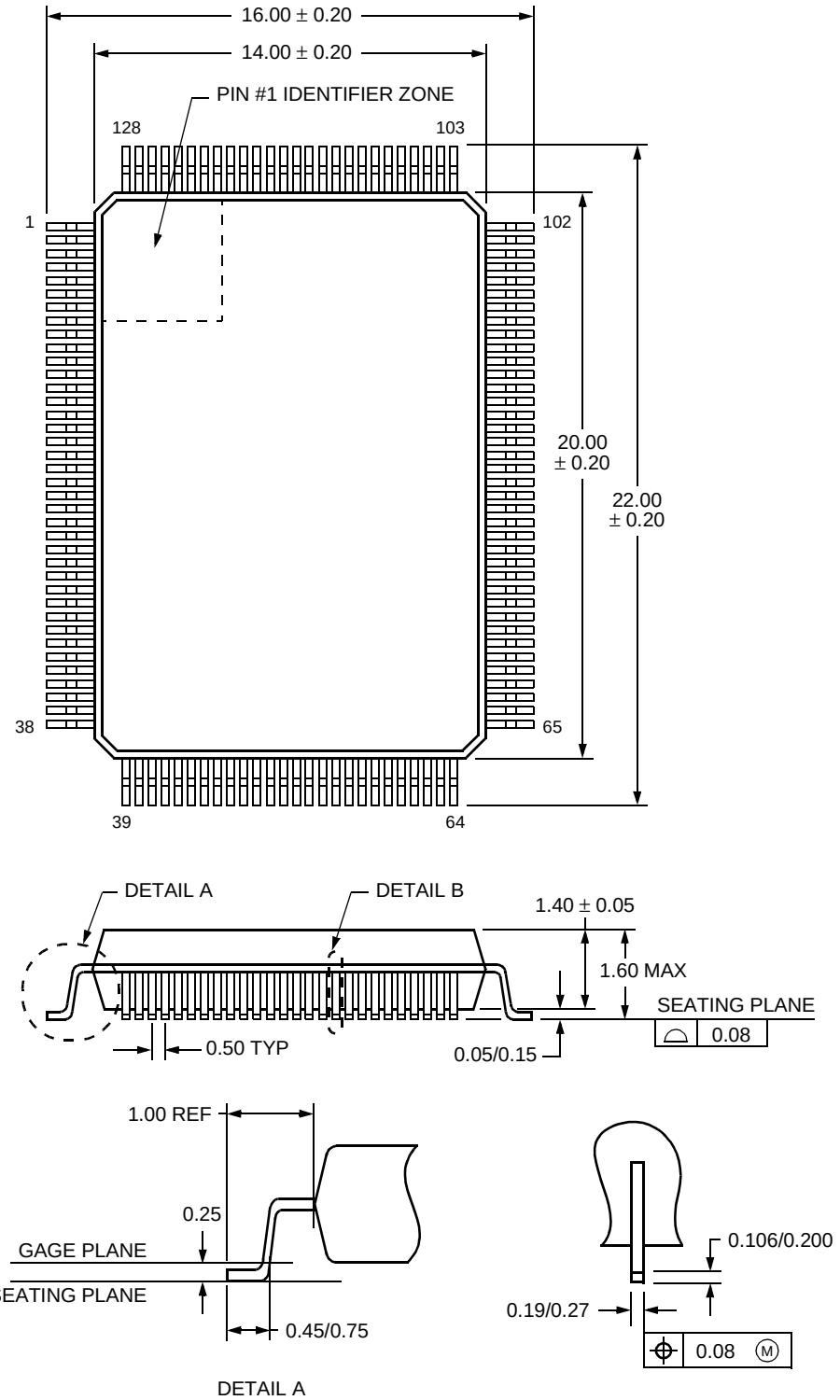
Figure 28. JTAG Timing

Table 79. JTAG Timing

Symbol	Parameter	Min	Typ	Max	Unit
TCK_{CYCLE}	TCK Cycle Time	20	—	—	ns
TCK_{HIGH}	TCK High Time	10	—	—	ns
TCK_{LOW}	TCK Low Time	10	—	—	ns
TCK_{RISE}	TCK Rise Time	—	1	—	ns
TCK_{FALL}	TCK Fall Time	—	1	—	ns
TCK_{SU}	TDI, TMS Setup Time to TCK	2.7	—	—	ns
TCK_{HOLD}	TDI, TMS Hold Time to TCK	0.8	—	—	ns
TCK_{DELAY}	TDO Delay Time from TCK	—	—	8.1	ns

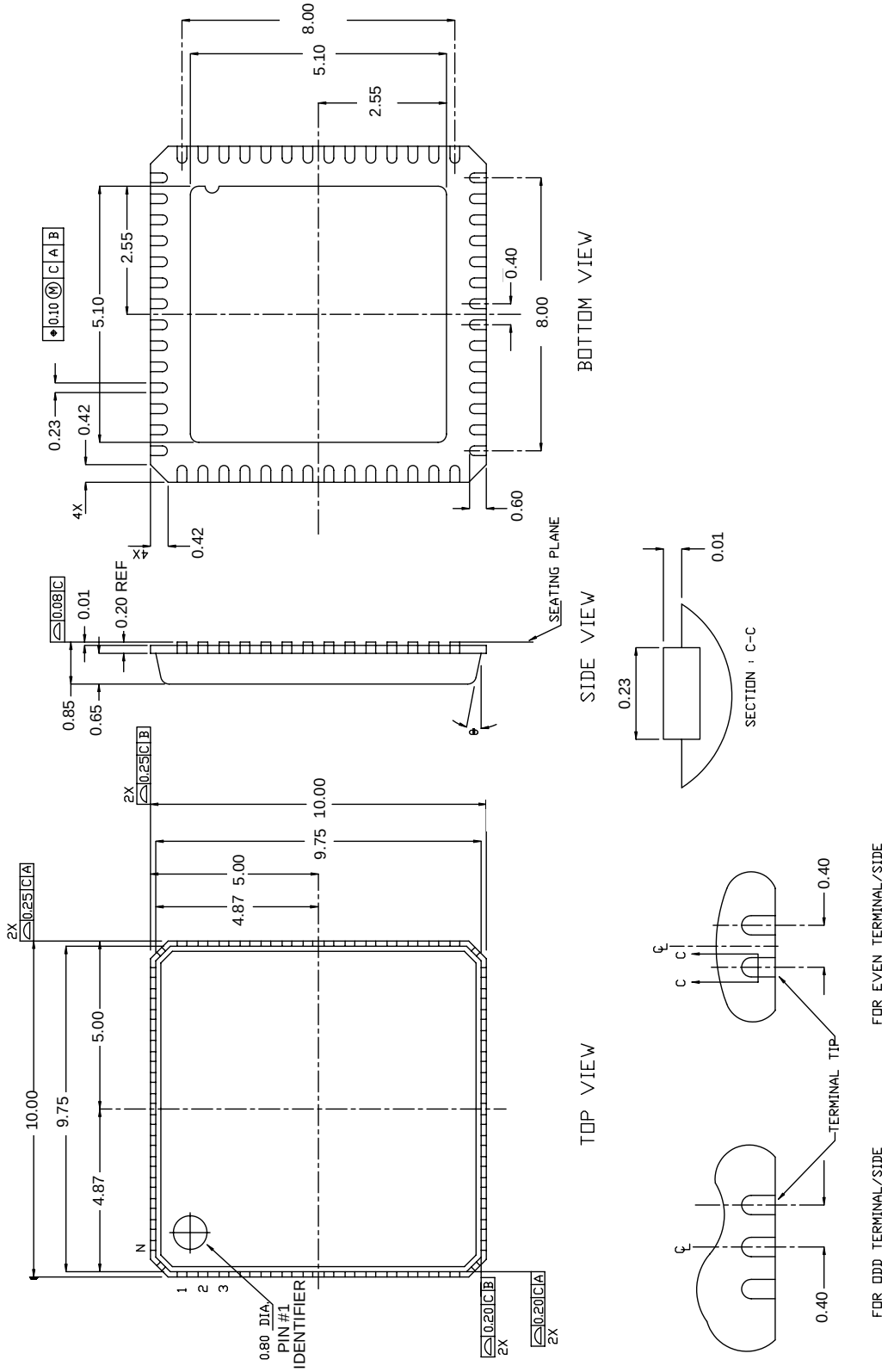
Package Diagram, 128-Pin TQFP (Dimensions are in millimeters.)

Note: Package outlines are unofficial and for reference only.



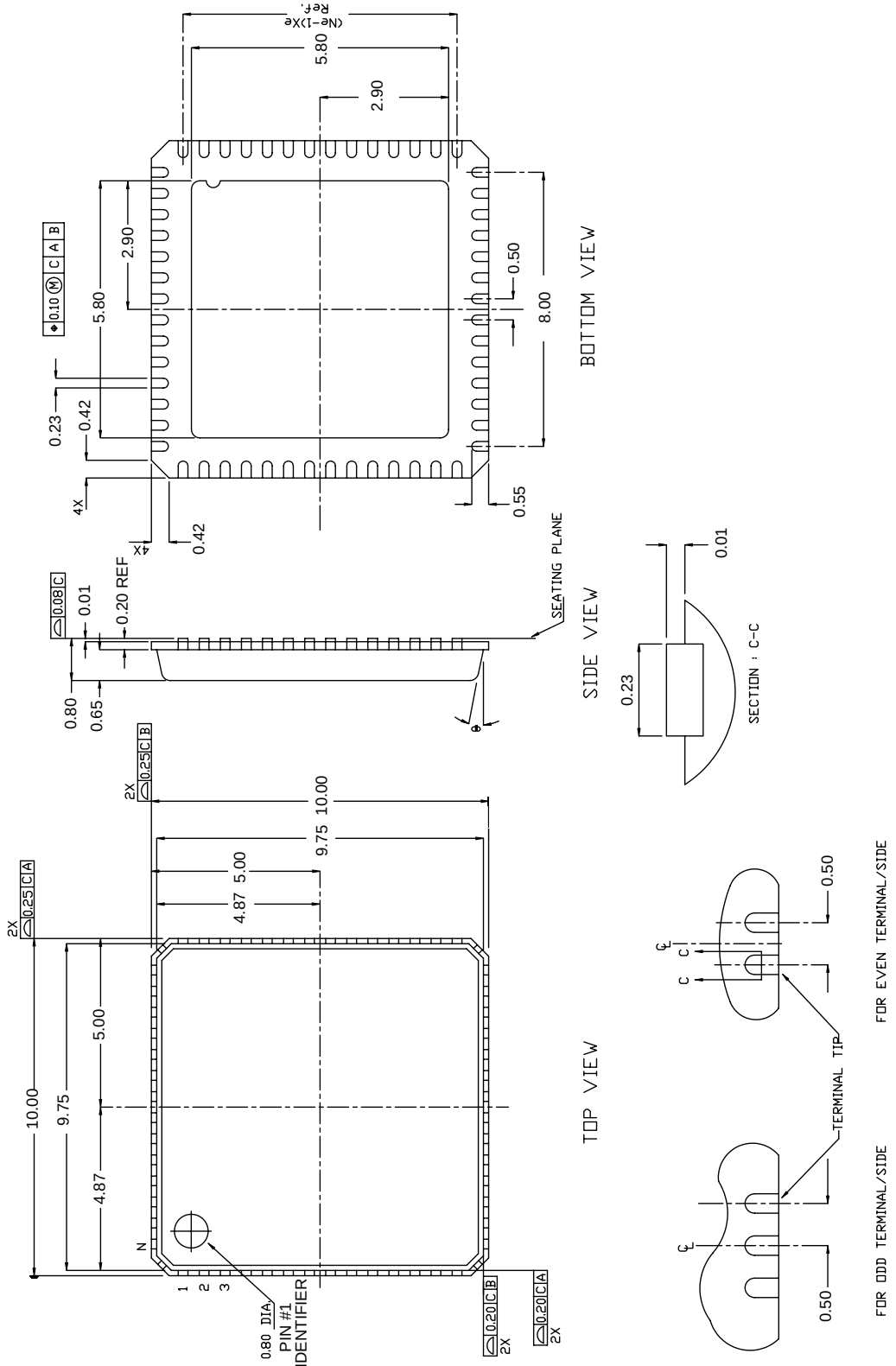
Package Diagram, 84-Pin MLCC (Dimensions are in millimeters.)

Note: Package outlines are unofficial and for reference only.



Package Diagram, 68-Pin MLCC (Dimensions are in millimeters.)

Note: Package outlines are unofficial and for reference only.



Ordering Information

Table 80. Ordering Information

Device/ Package	Description	Part Number*	Comcode
ET1011C 84-pin MLCC	Commercial GbE Transceiver, Lead-Free	M-L-ET1011C2-C-D	711017464M
	Commercial GbE Transceiver, Lead-Free	L-ET1011C2-C-D	711017464
	Commercial GbE Transceiver, Lead-Free	L-ET1011C2-C-DT	711017465
	Industrial GbE Transceiver, Lead-Free	M-L-ET1011C2-CI-D	711017462M
	Industrial GbE Transceiver, Lead-Free	L-ET1011C2-CI-D	711017462
	Industrial GbE Transceiver, Lead-Free	L-ET1011C2-CI-DT	711017463
ET1011C 68-pin MLCC	Commercial GbE Transceiver, Lead-Free	M-L-ET1011C2-M-D	711017468M
	Commercial GbE Transceiver, Lead-Free	L-ET1011C2-M-D	711017468
	Commercial GbE Transceiver, Lead-Free	L-ET1011C2-M-DT	711017469
	Industrial GbE Transceiver, Lead-Free	L-ET1011C2-MI-D	711017466
	Industrial GbE Transceiver, Lead-Free	L-ET1011C2-MI-DT	711017467
ET1011C 128-pin TQFP	Commercial GbE Transceiver, Lead-Free	M-L-ET1011C2-T-DB	711017470M
	Commercial GbE Transceiver, Lead-Free	L-ET1011C2-T-DB	711017470

* M = models; L = lead-free.

Ordering Information (continued)

Related Documentation

Table 81. Related Documentation

Device	Description	Document Type
ET1011	Gigabit Ethernet Transceiver	Product Brief Data Sheet Application Note
ET1310	Gigabit Ethernet Controller	
ET1081	Gigabit Ethernet Octal PHY	Product Brief Data Sheet
ET2008-50/40/30	Gigabit Ethernet Octal Switch and PHY	Product Brief Data Sheet
ET2005-50/40/30	Gigabit Ethernet Five-Port Switch and PHY	Product Brief Data Sheet
ET3028-50	Single-Chip 28 x 1 Gbit/s Layer 2 Ethernet Switch	Product Brief Data Sheet Application Note
ET3048-50	Single-Chip 48 x 1 Gbit/s Layer 2 Ethernet Switch	
ET4028-50	Single-Chip 28 x 1 Gbit/s Layer 2+ Ethernet Switch	
ET4048-50	Single-Chip 48 x 1 Gbit/s Layer 2+ Ethernet Switch	
ET4128-50	Single-Chip 28 x 1 Gbit/s + 2 x 10 Gbits/s Layer 2+ Ethernet Switch	
ET4148-50	Single-Chip 48 x 1 Gbit/s + 2 x 10 Gbits/s Layer 2+ Ethernet Switch	
ET5028-50	Single-Chip 28 x 1 Gbit/s Layer 2/3 Ethernet Switch	Product Brief
ET5048-50	Single-Chip 48 x 1 Gbit/s Layer 2/3 Ethernet Switch	
ET5128-50	Single-Chip 28 x 1 Gbit/s + 2 x 10 Gbits/s Layer 2/3 Ethernet Switch	
ET5148-50/60/70	Single-Chip 48 x 1 Gbit/s + 2 x 10 Gbits/s Layer 2/3 Ethernet Switch	
ET5148-50	Single-Chip 48 x 1 Gbit/s + 2 x 10 Gbits/s Layer 2/3 Ethernet Switch	Data Sheet

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