8M BYTE (2x1M x32) FLASH (5VSupply; 12V Program) SIMM MODULE

*PRELIMINARY**

FEATURES

- Access Time of 120ns
- Packaging:
  - 80 pin SIMM
- TTL compatible inputs and outputs
- 5V V_{CC} and 12V V_{PP}
- $\overline{RESET}$ control options:
  - $\overline{RESET}$ tied to Vcc
  - $\overline{RESET}$ tied to pin 7 for system control of reset
  - $\overline{RESET}$ tied to power supervisor circuit
- JEDEC standard
- Gold edge connectors
- Flash Memory Components:
  - WPF29041-120G1XI with Intel Part Number E28F008SA
  - WPF29041-120G1XS with Sharp Part Number LH28F008SAT

GENERAL DESCRIPTION

The White Microelectronics WPF29081-120G1XX is a 2 x 1M x 32 bits 80-pin Flash Single In-line Memory Module (SIMM). The WPF29081-120G1XX consists of eight 1M x 8 bits CMOS Flash memory in 40-pin TSOP-I packages mounted on an 80-pin glass epoxy substrate. Decoupling capacitors of 0.1µF are mounted for the Flash memory.

The WPF29081-120G1XX has gold edge connectors and is intended for mounting into 80-pin gold edge connector sockets. The WPF29081-120G1XX uses the standard programming algorithms for Intel or Sharp 28F008SA Flash memory components.

* *This data sheet describes a product under development, not fully characterized, and is subject to change without notice.*

PIN CONFIGURATION

Pin Symbols

Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V_{SS}	28	DQ_{31}	55	DQ_{15}
2	V_{CC}	29	$\overline{WE}_2$	56	DQ_{14}
3	V_{PP}	30	NC	57	DQ_{13}
4	$\overline{OE}$	31	NC	58	DQ_{12}
5	$\overline{WE}_0$	32	NC	59	DQ_{11}
6	$\overline{WE}_1$	33	A_{19}	60	DQ_{10}
7	NC/RESET*	34	A_{18}	61	DQ_9
8	DQ_{16}	35	A_{17}	62	DQ_8
9	DQ_{17}	36	A_{16}	63	DQ_7
10	DQ_{18}	37	A_{15}	64	DQ_6
11	DQ_{19}	38	A_{14}	65	DQ_5
12	DQ_{20}	39	A_{13}	66	DQ_4
13	DQ_{21}	40	A_{12}	67	DQ_3
14	DQ_{22}	41	A_{11}	68	DQ_2
15	DQ_{23}	42	A_{10}	69	DQ_1
16	DQ_{24}	43	A_9	70	DQ_0
17	DQ_{25}	44	A_8	71	V_{PP}
18	DQ_{26}	45	A_7	72	V_{CC}
19	DQ_{27}	46	A_6	73	PD_1
20	DQ_{28}	47	A_5	74	PD_2
21	NC	48	A_4	75	PD_3
22	NC	49	A_3	76	PD_4
23	$\overline{CE}_1$	50	A_2	77	PD_5
24	$\overline{CE}_0$	51	A_1	78	PD_6
25	V_{SS}	52	A_0	79	PD_7
26	DQ_{29}	53	$\overline{WE}_3$	80	V_{SS}
27	DQ_{30}	54	V_{SS}		

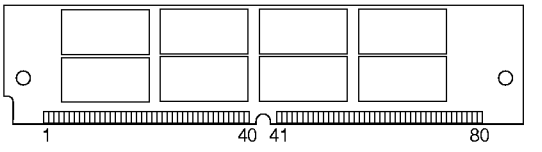
Pin Functions

Pin Symbol	Pin Function
A_0-A_{19}	Address Inputs
DQ_0-DQ_{31}	Data In/Out
$\overline{CE}_0$, $\overline{CE}_1$	Chip Enable
$\overline{WE}_0$-$\overline{WE}_3$	Write Enable
$\overline{OE}$	Output Enable
PD_1-PD_7	Presence Detect
V_{CC}	Power (+5V)
V_{PP}	Programming Voltage (+12V)
V_{SS}	Ground
NC	No Connection

Presence Detect Pins*

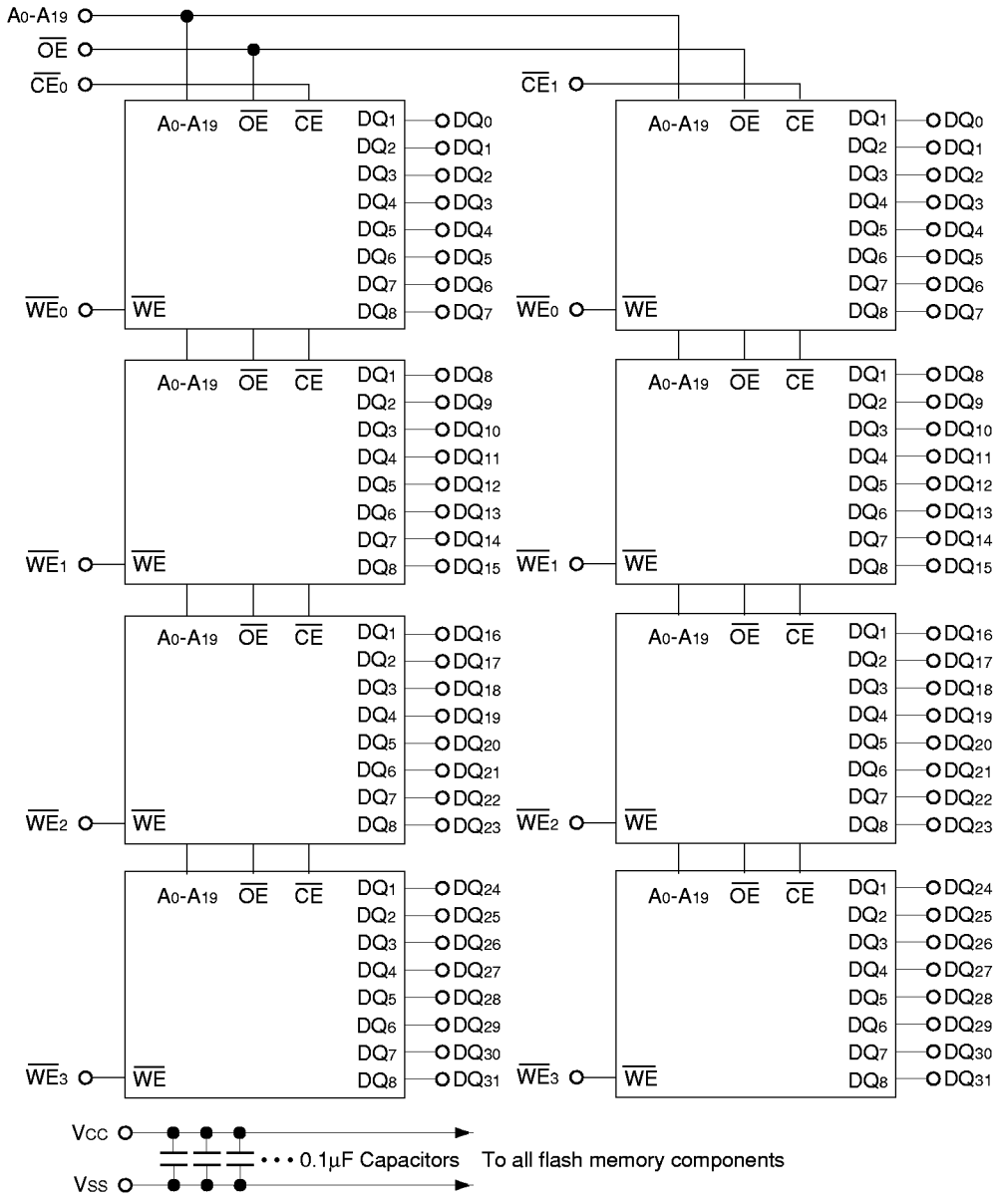
Pin Name	Signal
PD_1	V_{SS}
PD_2	V_{SS}
PD_3	NC
PD_4	V_{SS}
PD_5	V_{SS}
PD_6	NC
PD_7	V_{SS}

* Pin Connection Changing Available



* Pin 7 = NC for $\overline{RESET}$ option V and P, and tied to component $\overline{RESET}$ for option "R".

FUNCTIONAL BLOCK DIAGRAM



Notes:

1. $\overline{RP}$ of the flash memory components is connected as shown in the $\overline{RESET}$ options in ordering information.
2. RD/$\overline{BY}$ of the flash memory components is not connected.

ABSOLUTE MAXIMUM RATINGS[1]

Item	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS} except V_{CC} and V_{PP}[2]	V_{IN}, V_{OUT}	-2.0 to +7.0	V
Voltage on V_{CC} Relative to V_{SS}[2]	V_{CC}	-2.0 to +7.0	V
Voltage on V_{PP} Relative to V_{SS}[2, 3]	V_{PP}	-2.0 to +14.0	V
Storage Temperature	T_{stg}	-65 to +125	°C
Short Circuit Output Current[4]	I_{OS}	100	mA

1. Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the oprerational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Minimum DC voltage on input or I/O pins is -0.5 V is -0.2V. During voltage transitions, this level may undershoot V_{SS} to -2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O pins is V_{CC}+0.5 V. During voltage transitions, input and I/O pins may overshoot to V_{CC}+2.0 V for periods up to 20 ns.
3. Maximum DC voltage on V_{PP} may overshoot to +14.0V for periods <20ns.
4. No more than one output shorted to ground at a time. Duration of the short circuit should not be greater than one second.

CAPACITANCE (T_A=25 °C; V_{CC}=5.0V±0.5V; f=1MHz)

Item	Symbol	Typ	Units
A_0-A_{19}, $\overline{OE}$ Input Capacitance (V_{IN}=0)	C_{IN1}	63	pF
$\overline{WE}_0$-$\overline{WE}_3$ Input Capacitance (V_{IN}=0)	C_{IN2}	27	pF
$\overline{CE}_0$, $\overline{CE}_1$ Input Capacitance (V_{IN}=0)	C_{IN3}	39	pF
DQ_0-DQ_{31} Input Capacitance (V_{IN}=0)	C_{IN4}	27	pF
DQ_0-DQ_{31}Output Capacitance (V_{OUT}=0)	C_{OUT}	31	pF

DC CHARACTERISTICS (V_{CC}=5.0V±0.5V; T_A= 0°C to +70°C)

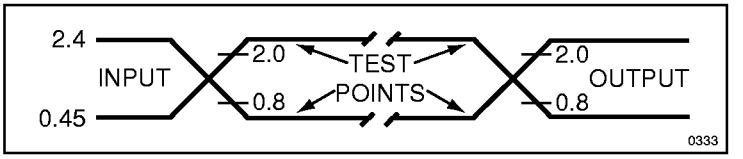
Parameter	Symbol	Min	Typ	Max	Units	Notes
Input Load Current (V_{IN}=V_{SS} or V_{CC}, V_{CC}=V_{CC}Max)	I_{LI}			8	µA	1
Output Leakage Current (V_{OUT}=V_{SS} to V_{CC}, V_{CC}=V_{CC}Max)	I_{LO}			20	µA	1
V_{CC} Standby Current (V_{CC}=V_{CC}Max, $\overline{CE}$=V_{CC}±0.2V) (V_{CC}=V_{CC}Max, $\overline{CE}$=V_{IH})	I_{CCS}		240 8	800 16	µA mA	1,5
V_{CC} Read Current ($\overline{CE}$=V_{IL}, $\overline{OE}$=V_{IH}, f=8MHz, I_{OUT}=0mA, CMOS inputs)	$I_{CCR}1$		80	140	mA	1,4,5
V_{CC} Read Current ($\overline{CE}$=V_{IL}, $\overline{OE}$=V_{IH}, f=8MHz, I_{OUT}=0mA, TTL inputs)	$I_{CCR}2$		104	208	mA	1,4,5
V_{CC} Write Current (Word Write in Progress)	I_{CCW}		44	128	mA	1
V_{CC} Block Erase Current (Block Erase in Progress)	I_{CCE}		44	128	mA	1
V_{CC} Erase Suspend Current (Block Erase Suspended, $\overline{CE}$=V_{IH})	I_{CCES}		24	48	mA	1,2
V_{PP} Standby/Read Current (V_{PP}≤V_{CC}) (V_{PP}>V_{CC})	I_{PPS} I_{PPR}		8	120 1600	µA	1
V_{PP} Write Current (Word Write in Progress, V_{PP}=V_{PPH})	I_{PPW}		40	120	mA	1
V_{PP} Block Erase Current (Block Erase in Progress, V_{PP}=V_{PPH})	I_{PPE}		40	120	mA	1
V_{PP} Erase Suspend Current (Block Erase Suspended)	I_{PPES}		274	860	µA	1,2
Input Low Voltage	V_{IL}	-0.5		0.8	V	
Input High Voltage	V_{IH}	2.0		V_{CC}+0.5	V	
Output Low Voltage (I_{OL}=5.8 mA, V_{CC}=V_{CC}Min)	V_{OL}			0.45	V	
Output High Voltage (I_{OH}=-2.5mA, V_{CC}=V_{CC}Min) (I_{OH}=-100µA, V_{CC}=V_{CC}Min)	$V_{OH}1$ $V_{OH}2$	0.85V_{CC} V_{CC}-0.4			V V	
V_{PP} Write/Erase Lock Voltage	V_{PPLK}	0.0		6.5	V	
V_{PP} during Write/Erase Operations	V_{PPH}	11.4	12.0	12.6	V	
V_{CC} Write/Erase Lock Voltage	V_{LKO}	2.0			V	

1. All currents are in RMS unless otherwise noted. Typical values at V_{CC}=5.0V, V_{PP}=12.0V, T=25°C.
2. I_{CCES} is specified with the device de-selected. If the device is read while in erase suspend mode, current draw is the sum of I_{CCES} and I_{CCR}.
3. BlockErases, Word Writes and Lock Block operations are inhibited when V_{PP}≤V_{PPLK} and not guaranteed in the ranges between V_{PPLK}(max) and V_{PPH}(min), and above V_{PPH}(max).
4. Automatic Power Saving (APS) reduces I_{CCR} to 1mA typical in Static operation.
5. CMOS inputs are either V_{CC}±0.2V or VSS±0.2V. TTL inputs are either V_{IL} or V_{IH}.

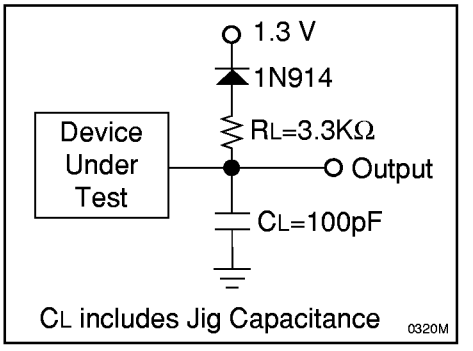
AC CHARACTERISTICS

AC Test Conditions

AC test inputs are driven at V_{OH} (2.4 V_{TTL}) for a Logic "1" and V_{OL} (0.45 V_{TTL}) for a logic "0." Input timing begins at V_{IH} (2.0 V_{TTL}) and V_{IL} (0.8 V_{TTL}). Output timing ends at V_{IH} and V_{IL}. Input rise and fall times (10% to 90%) <10ns. Refer to the Transient Input/Output Reference Waveform and Transient Equivalent Testing Load Circuit figures below.



Transient Input/Output Reference Waveform



Transient Equivalent Testing Load Circuit

Read Only Operations[1] (V_{CC}=5V±10%; T_A=0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Read cycle time	t_{AVAV}	120			ns	
Address to output delay	t_{AVQV}			120	ns	
$\overline{CE}$ to output delay	t_{ELQV}			120	ns	2
$\overline{RST}$ to output delay	t_{PHQV}			400	ns	
$\overline{OE}$ to output delay	t_{GLQV}			50	ns	2
$\overline{CE}$ to output in low Z	t_{ELQX}	0			ns	
$\overline{CE}$ to output high Z	t_{EHQZ}			55	ns	
$\overline{OE}$ to output in low Z	t_{GLQX}	0			ns	
$\overline{OE}$ to output high Z	t_{GHQZ}			30	ns	
Output hold from address, $\overline{CE}$ or $\overline{OE}$ change, whichever occurs first	t_{OH}	0			ns	

1. See AC input/output reference waveforms for timing measurements.
2. $\overline{OE}$ may be delayed up to t_{ELQV}-t_{GLQV} after the falling edge of $\overline{CE}$, without impacting t_{ELQV}.

AC CHARACTERISTICS (continued)

$\overline{WE}$-Controlled Command Write Operations[1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Write cycle time	t_{AVAV}	120			ns	
V_{PP} setup to $\overline{WE}$ going high	t_{VPWH}	100			ns	
$\overline{CE}$ setup to $\overline{WE}$ going low	t_{ELWL}	10			ns	
Address setup to $\overline{WE}$ going high	t_{AVWH}	40			ns	2
Data setup to $\overline{WE}$ going high	t_{DVWH}	40			ns	2
$\overline{WE}$ pulse width	t_{WLWH}	40			ns	
Data hold rom $\overline{WE}$ high	t_{WHDX}	5			ns	
Address hold from $\overline{WE}$ high	t_{WHAX}	5			ns	
$\overline{CE}$ hold from $\overline{WE}$ high	t_{WHEH}	10			ns	
$\overline{WE}$ pulse width high	t_{WHWL}	30			ns	
Read recovery before Write	t_{GHWL}	0			ns	
Write recovery before Read	t_{WHGL}	0			ns	
V_{PP} hold from valid Status Register (CSR, GSR, BSR) data	t_{QVVL}	0			µs	
Duration of Byte Write operation	$t_{WHQV}1$	6			µs	
Duration of Block Erase operation	$t_{WHQV}2$	0.3			s	

1. Read timings during write and erase are the same as for normal read.
2. Address and data are latched on the rising edge of $\overline{WE}$ for all Command Write operations.

$\overline{CE}$-Controlled Command Write Operations (See note 1)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Write cycle time	t_{AVAV}	120			ns	
V_{PP} setup to $\overline{CE}$ going high	t_{VPEH}	100			ns	
$\overline{WE}$ setup to $\overline{CE}$ going low	t_{WLEL}	0			ns	
Address setup to $\overline{CE}$ going high	t_{AVEH}	40			ns	2
Data setup to $\overline{CE}$ going high	t_{DVEH}	40			ns	2
$\overline{CE}$ pulse width	t_{ELEH}	50			ns	
Data hold from $\overline{CE}$ high	t_{EHDX}	5			ns	
Address hold from $\overline{CE}$ high	t_{EHAX}	5			ns	
$\overline{WE}$ hold from $\overline{CE}$ high	t_{EHWH}	0			ns	
$\overline{CE}$ pulse width high	t_{EHEL}	25			ns	
Write recovery before Read	t_{EHGL}	0			ns	
V_{PP} hold from valid Status Register (CSR, GSR, BSR) data	t_{QVVL}	0			µs	
Duration of Byte Write operation	$t_{EHQV}1$	6			µs	
Duration of Block Erase operation	$t_{EHQV}2$	0.3			s	

1. Read timings during write and erase are the same as for normal read.
2. Address and data are latched on the rising edge of $\overline{WE}$ for all Command Write operations.

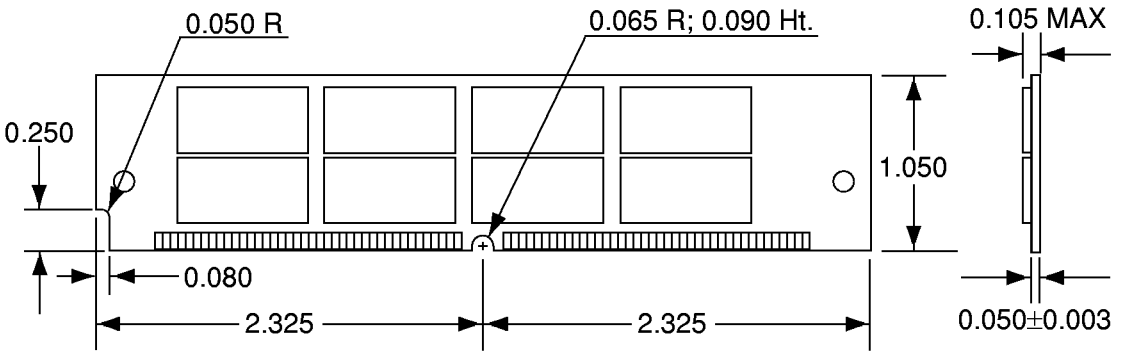
ERASE AND BYTE WRITE PERFORMANCE[1]

Parameter	Typ	Max	Unit	Notes
Block erase time	1.6	10	s	2
Block write time	0.6	2.1	s	2
Byte write time	8		µs	

1. 25°C, and nominal voltages.
2. Excludes system-level overhead.

PACKAGE DIMENSIONS

Units: Inches



TOLERANCES: ±0.005 UNLESS OTHERWISE SPECIFIED

ORDERING INFORMATION