SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER

DESCRIPTION

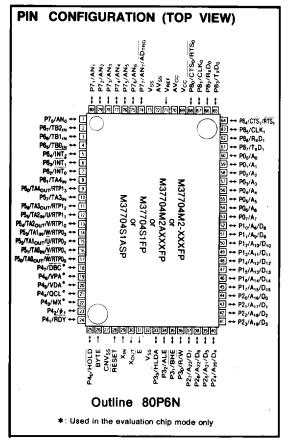
The M37704M2-XXXFP, M37704M2AXXXFP, M37704S1FP and M37704S1AFP are single-chip microcomputers designed with high-performance CMOS silicon gate technology. These are housed in a 80-pin plastic molded QFP. These single-chip microcomputers have a large 16M bytes address space, three instruction queue buffers, and two data buffers for high-speed instruction execution. The CPU is a 16-bit parallel processor that can also be switched to perform 8-bit parallel processing. These microcomputers are suitable for office, business, and industrial equipment controller that require high-speed processing of large data. Also, the incorporated motor control circuit makes these microcomputers suitable for control of equipment that requires motor control.

The differences between M37704M2-XXXFP, M37704M2A XXXFP, M37704S1FP and M37704S1AFP are the ROM size and the external clock input frequency as shown below. Therefore, the following descriptions will be for the M37704M2-XXXFP unless otherwise noted.

Type name	ROM size	External clock input frequency
M37704M2-XXXFP	16K bytes	8 MHz
M37704M2AXXXFP	16K bytes	16MHz
M37704S1FP	External	8 MHz
M37704S1AFP	External	16MHz

DISTINCTIVE FEATURES

U	PHINCHAE	
•	Number of bas	ic instructions·····103
•	Memory size	
		RAM 512 bytes
•	Instruction exe	
	M37704M2-XX	KFP, M37704S1FP
		struction at 8 MHz frequency) 500ns
		XFP, M37704S1AFP
		struction at 16 MHz frequency)······ 250ns
•		upply5V±10%
•		sipation (at 8 MHz frequency)
	_on ponor alo	
_		30mW (Typ.)
•		19 types 7 levels
•	•	n 16-bit timer ····· 5+3
	(Three-phase	motor drive waveform or pulse motor
		can be output.)
•	UART (may als	o be synchronous)2
•	8-bit A-D conve	rter ····· 8-channel inputs
•	12-bit watchdo	
•	Programmable	input/output
		2, P3, P4, P5, P6, P7, P8) ····· 68



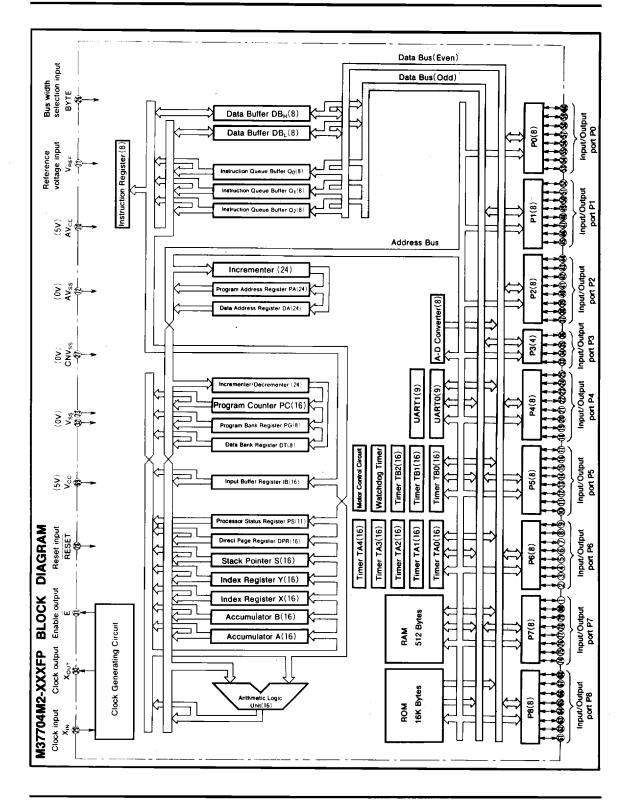
APPLICATION

Control devices for office equipment such as copiers, printers, typewriters, facsimiles, word processors, and personal computers

Control devices for industrial equipment such as ME, NC, general purpose inverter and measuring instruments.

M37704M2-XXXFP,M37704M2AXXXFP M37704S1FP,M37704S1AFP

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FUNCTIONS OF M37704M2-XXXFP

Parameter		Functions	
Number of basic Instructions		103	
Instruction execution time	M37704M2-XXXFP, M37704S1FP	500ns (the fastest instructions, at 8MHz frequency)	
	M37704M2AXXXFP, M37704S1AFP	250ns (the fastest instructions, at 16MHz frequency)	
Memory size	ROM	16K bytes	
	RAM	512 bytes	
Input/Output ports	P0~P2, P4~P8	8-bit×8	
input/Output ports	P3	4-bit×1	
Multi-function timers	TAO, TA1, TA2, TA3, TA4	16-bit× 5	
Multi-function timers	TB0, TB1, TB2	16-bit× 3	
Serial I/O		(UART or clock synchronous serial I/O)X2	
A-D converter		8-bitX1 (8 channels)	
Watchdog timer		12-bit× 1	
Dead-time timer		8 -bit× 3	
Intermete		3 external types, 16 internal types	
Interrupts		(Each interrupt can be set the priority levels to $0 \sim 7$.)	
Clock generating circuit		Built-in(externally connected to a ceramic resonator or quartz crystal resonator	
Supply voltage		5 V±10%	
Power dissipation		30mW(at external 8 MHz frequency)	
Input/Output characteristic	Input/Output voltage	5 V	
	Output current	5 mA	
Memory expansion		Maximum 16M bytes	
Operating temperature range		-10~70°C	
Device structure		CMOS high-performance silicon gate process	
Package		80-pin plastic molded QFP	



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PIN DESCRIPTION

Pin	Name	Input/Output	Functions
V _{CC} , V _{SS}	Power supply		Supply 5 V±10% to V _{CC} and 0 V to V _{SS} .
CNVss	CNV _{SS} input	Input	This pin controls the processor mode. Connect to V_{SS} for single-chip mode, and to V_{CC} for external ROM types.
RESET	Reset input	Input	To enter the reset state, this pin must be kept at a "L" condition should be maintained for the required time.
XIN	Clock input	input	These are I/O pins of internal clock generating circuit. Connect a ceramic or quartz crystal resonator be-
Хоит	Clock output	Output	tween X_{IN} and X_{OUT} . When an external clock is used, the clock source should be connected to the X_{IN} pin and the X_{OUT} pin should be left open.
Ē	Enable output	Output	Data or instruction read and data write are performed when output from this pin is "L".
BYTE	Bus width selection input	Input	In memory expansion mode or microprocessor mode, this pin determines whether the external data bus is 8-bit width or 16-bit width. The width is 16 bits when "L" signal inputs and 8 bits when "H" signal inputs.
AV _{CC} AV _{SS}	Analog supply input		Power supply for the A-D converter. Connect AV _{CC} to V _{CC} and AV _{SS} to V _{SS} externally.
V _{REF}	Reference voltage input	Input	This is reference voltage input pin for the A-D converter.
P0 ₀ ~P0 ₇	I/O port P0	1/0	In single-chip mode, port P0 becomes an 8-bit I/O port. An I/O directional register is available so that each pin can be programmed for input or output. These ports are in input mode when reset . Address($A_7 \sim A_0$) is output in memory expansion mode or microprocessor mode.
P1 ₀ ~P1 ₇	I/O port P1	1/0	In single-chip mode, these pins have the same functions as port P0. When the BYTE pin is set to "L" in memory expansion mode or microprocessor mode and external data bus is 16-bit width, high-order data $(D_{15}\sim D_8)$ is input or output when \overline{E} output is "L" and an address $(A_{15}\sim A_8)$ is output when \overline{E} output is "H". If the BYTE pin is "H" that is an external data bus is 8-bit width, only address $(A_{15}\sim A_8)$ is output.
P2 ₀ ~P2 ₇	I/O port P2	1/0	In single-chip mode, these pins have the same functions as port P0. In memory expansion mode or microp-rocessor mode low-order data($D_7 \sim D_0$) is input or output when \overline{E} output is "L" and an address($A_{23} \sim A_{16}$) is output when \overline{E} output is "H".
P3 ₀ ~P3 ₃	I/O port P3	1/0	In single-chip mode , these pins have the same functions as port P0. In memory expansion mode or microprocessor mode, R/W, BHE, ALE, and HLDA signals are output.
P4 ₀ ~P4 ₇	I/O port P4	1/0	In single-chip mode, these pins have the same functions as port P0. In memory expansion mode or microprocessor mode, P4 $_0$ and P4 $_1$ become \overline{HOLD} and \overline{RDY} input pin respectively. Functions of other pins are the same as in single-chip mode. In single-chip mode or memory expansion mode, port P4 $_2$ can be programed for ϕ_1 output pin divided the clock to X_{IN} pin by 2. In microprocessor mode, P4 $_2$ always has the function as ϕ_1 output pin.
P5 ₀ ~P5 ₇	I/O port P5	1/0	in addition to having the same functions as port P0 in single-chip mode, these pins also function as I/O pins for timer A0, timer A1, timer A2 and timer A3. P5 ₀ to P5 ₀ also have the function as motor control output pins.
P6 ₀ ~P6 ₇	I/O port P6	1/0	In addition to having the same functions as port P0 in single-chip mode, these pins also function as $\frac{1}{1}$ CO pins for timer A4, external interrupt input $\frac{1}{1}$ NT ₁ , $\frac{1}{1}$ NT ₁ and $\frac{1}{1}$ NT ₂ pins, and input pins for timer B0, timer B1 and timer B2. P6 ₀ and P6 ₂ also have the function as motor control output pins.
P7 ₀ ~P7,	I/O port P7	1/0	In addition to having the same functions as port P0 in single-chip mode, these pins also function as analog input ANo~AN7 input pins. P77 also has an A-D conversion trigger input function.
P8 ₀ ~P8 ₇	I/O port P8	1/0	In addition to having the same functions as port P0 in single-chip mode, these pins also function as R _X D T _X D, CLK, CTS/RTS pins for UART 0 and UART 1.



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BASIC FUNCTION BLOCKS

The M37704M2-XXXFP contains the following devices on a single chip: ROM and RAM for storing instructions and data, CPU for processing, bus interface unit (which controls instruction prefetch and data read/write between CPU and memory), timers, UART, A-D converter, and other peripheral devices such as I/O ports. Each of these devices are described below.

MEMORY

The memory map is shown in Figure 1. The address space is 16M bytes from addresses 0_{16} to FFFFFF $_{16}$. The address space is divided into 64K bytes units called banks. The banks are numbered from 0_{16} to FF $_{16}$.

Built-in ROM, RAM and control registers for built-in peripheral devices are assigned to bank 0.

The 16K bytes area from addresses C000₁₆ to FFFF₁₆ is the built-in ROM. Addresses FFD6₁₆ to FFFF₁₆ are the RESET and interrupt vector addresses and contain the interrupt vectors. Refer to the section on interrupts for details.

The 512 bytes area from addresses 80_{16} to $27F_{18}$ contains the built-in RAM. In addition to storing data, the RAM is used as stack during a subroutine call, or interrupts.

Assigned to addresses 0₁₆ to 7F₁₆ are peripheral devices such as I/O ports, A-D converter, UART, timer, and interrupt control registers.

A 256 bytes direct page area can be allocated anywhere in bank 0 using the direct page register DPR. In direct page addressing mode, the memory in the direct page area can be accessed with two words thus reducing program steps.

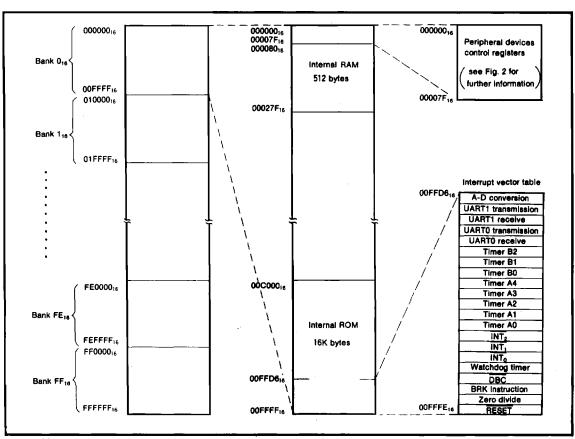


Fig. 1 Memory map

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	decimal notation)	Address (Hexad	
000000		000040	Count start flag
000001		000041	
000002	Port P0	000042	One shot start flag
000003	Port P1	000043	
000004	Port P0 data direction register	000044	Up-down flag
000005	Port P1 data direction register	000045	
000006	Port P2	000048	Timer A0
000007	Port P3	000047	THIO FIG
800000	Port P2 data direction register	000048	Timer A1
000009	Port P3 data direction register	000049	Timer A)
A00000	Port P4	00004A	Timer A2
00000B	Port P5	00004B	Timer AZ
00000C	Port P4 data direction register	00004C	Timer A3
00000D	Port P5 data direction register	00004D	Timer A3
00000E	Port P6	00004E	
00000F	Port P7	00004F	Timer A4
000010	Port P6 data direction register	000050	
000011	Port P7 data direction register	000051	Timer B0
000011	Port P8	000052	
	POIL FO	000053	Timer B1
000013	D. J. DO. data affectables as sinkers	000054	
000014	Port P8 data direction register		Timer B2
000015		000055	
000016		000056	Timer A0 mode register
000017		000057	Timer A1 mode register
000018		000058	Timer A2 mode register
000019		000059	Timer A3 mode register
00001A		00005A	Timer A4 mode register
00001B		00005B	Timer B0 mode register
00001C		00005C	Timer B1 mode register
00001D		00005D	Timer B2 mode register
00001E	A-D control register	00005E	Processor mode register
00001E	A-D sweep pin selection register	00005F	
000017		000060	Watchdog timer
	A-D register 0	000061	Watchdog timer frequency selection flag
000021		000062	Waveform output mode register
000022	A-D register 1		
000023		000063	Dead-time timer
000024	A-D register 2	000064	Pulse output data register 1
000025		000065	Pulse output data register ()
000026	A-D register 3	000066	
000027		000067	
000028	A-D register 4	000068	
000029		000069	
00002A	A-D register 5	00006A	
00002B		00006B	
00002C	A-D register 6	00006C	
00002D		00006D	
00002E	A-D register 7	00006E	
00002E	A. D. (Oglotel)	00006F	
	LIART O transmit/receive made register	000070	A-D conversion interrupt control register
000030	UART 0 transmit/receive mode register		
000031	UART 0 bit rate generator	000071	UARTO transmission interrupt control register
000032	UART 0 transmission buffer register	000072	UARTO receive Interrupt control register
000033		000073	UART1 transmission interrupt control register
000034	UART 0 transmit/receive control register 0	000074	UART1 receive interrupt control register
000035	UART 0 transmit/receive control register 1	000075	Timer A0 interrupt control register
000036		000076	Timer A1 interrupt control register
000037	UART 0 receive buffer register	000077	Timer A2 interrupt control register
000038	UART 1 transmit/receive mode register	000078	Timer A3 interrupt control register
000039	UART 1 bit rate generator	000079	Timer A4 interrupt control register
000039 00003A		00007A	Timer B0 interrupt control register
	UART 1 transmission buffer register	00007B	Timer B1 interrupt control register
00003B	114 DT 4 have a sit (see a live a content of a live a		Timer B2 interrupt control register
00003C	UART 1 transmit/receive control register 0	00007C	
00003D	UART 1 transmit/receive control register 1	00007D	INTo interrupt control register
00003E	UART 1 receive buffer register	00007E	INT ₁ interrupt control register
00003F	Trust I Industry provide Inflicator	00007F	INT ₂ interrupt control regiter

Fig. 2 Location of peripheral devices and interrupt control registers



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CENTRAL PROCESSING UNIT (CPU)

The CPU has ten registers and is shown in Figure 3. Each of these registers is described below.

ACCUMULATOR A (A)

Accumulator A is the main register of the microcomputer. It consists of 16 bits and the lower 8 bits can be used separately. The data length flag m determines whether the register is used as 16-bit register or as 8-bit register. It is used as a 16-bit register when flag m is "0" and as an 8-bit register when flag m is "1". Flag m is a part of the processor status register (PS) which is described later.

Data operations such as calculations, data transfer, input/output, etc., is executed mainly through the accumulator.

ACCUMULATOR B (B)

Accumulator B has the same functions as accumulator A, but the use of accumulator B requires more instruction bytes and execution cycles than accumulator A.

INDEX REGISTER X (X)

Index register X consists of 16 bits and the lower 8 bits can be used separately. The index register length flag x determines whether the register is used as 16-bit register or as 8-bit register. It is used as a 16-bit register when flag x is "0" and as an 8-bit register when flag x is "1". Flag x is a part of the processor status register (PS) which is described later.

In index addressing mode, register X is used as the index register and the contents of this address is added to obtain the real address.

Also, when executing a block transfer instruction MVP or MVN, the contents of index register X indicates the low-order 16 bits of the source data address. The third byte of the MVP and MVN is the high-order 8 bits of the source data address.

INDEX REGISTER Y (Y)

Index register Y consists of 16 bits and the lower 8 bits can be used separately. The index register length flag x determines whether the register is used as 16-bit register or as 8-bit register. It is used as a 16-bit register when flag x "0" and as an 8-bit register when flag x is "1". Flag x is a part of the processor status register (PS) which is described later.

In Index addressing mode, register Y is used as the index register and the contents of this address is added to obtain the real address.

Also, when executing a block transfer instruction MVP or MVN, the content of index register Y indicates the low-order 16 bits of the destination address. The second byte of the MVP and MVN is the high-order 8 bits of the destination data address.

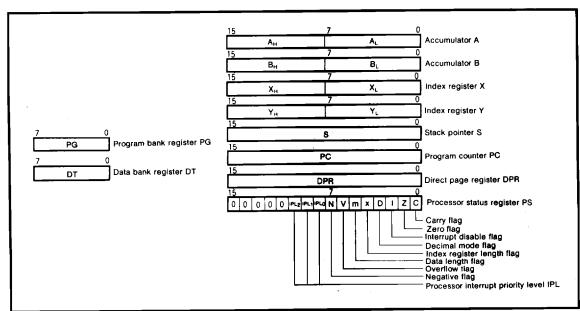


Fig. 3 Register structure

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STACK POINTER (S)

Stack pointer (S) is an 16-bit register. It is used during a subroutine call or interrupts. It is also used during stack, stack pointer relative, or stack pointer relative indirect indexed Y addressing mode.

PROGRAM COUNTER (PC)

Program counter (PC) is a 16-bit counter that indicates the low-order 16 bits of the next program memory address to be executed. These is a bus interface unit between the program memory and the CPU, so that the program memory is accessed through bus interface unit. This is described later.

PROGRAM BANK REGISTER (PG)

Program bank register is an 8-bit register that indicates the high-order 8 bits of the next program memory address to be executed. When a carry occurs by incrementing the contents of the program counter, the cotents of the program bank register (PG) is incremented by 1. Also, when a carry or borrow occurs after adding or subtracting the offset value to or from the contents of the program counter (PC) using branch instruction, the contents of the program bank register (PG) is incremented or decremented by 1 so that programs can be written without worrying about bank boundaries.

DATA BANK REGISTER (DT)

Data bank register (DT) is an 8-bit register. With some addressing modes, a part of the data bank register (DT) is used to specify a memory address. The contents of data bank register (DT) is used as the high-order 8 bits of a 24-bit address. Addressing modes that use the data bank register (DT) are direct indirect, direct indexed X indirect, direct indirect indexed Y, absolute bit, absolute indexed X, absolute indexed Y, absolute bit relative, and stack pointer relative indirect indexed Y.

DIRECT PAGE REGISTER (DPR)

Direct page register (DPR) is a 16-bit register. Its contents is used as the base address of a 256-byte direct page area. The direct page area is allocated in bank 0, but when the contents of DPR is FF01₁₆ or greater, the direct page area spans across bank 0 and bank 1. All direct addressing modes use the contents of the direct page register (DPR) to generate the data address. If the low-order 8 bits of the direct page register (DPR) is "00₁₆", the number of cycles required to generate an address is minimized. Normally the low-order 8 bits of the direct page register (DPR) is set to "00₁₆".

PROCESSOR STATUS REGISTER (PS)

Processor status register (PS) is an 11-bit register. It consists of a flag to indicate the result of operation and CPU interrupt levels.

Branch operations can be performed by testing the flags C, Z, V, and N.

The details of each processor status register bit are described below.

1. Carry flag (C)

The carry flag contains the carry or borrow generated by the ALU after an arithmetic operation. This flag is also affected by shift and rotate instructions. This flag can be set and reset directly with the SEC and CLC instructions or with the SEP and CLP instructions.

2. Zero flag (Z)

This zero flag is set if the result of an arithmetic operation or data transfer is zero and reset if it is not. This flag can be set and reset directly with the SEP and CLP instructions.

3. Interrupt disable flag (1)

When the interrupt disable flag is set to "1", all interrupts except watchdog timer, DBC, and software interrupt are disabled. This flag is set to "1" automatically when these is an interrupt. It can be set and reset directly with the SEI and CLI instructions or SEP and CLP instructions.

4. Decimal mode flag (D)

The decimal mode flag determines whether addition and subtraction are performed as binary or decimal. Binary arithmetic is performed when this flag is "0". If it is "1", decimal arithmetic is performed with each word treated as two or four digit decimal. Arithmetic operation is performed using four digits when the data length flag m is "0" and with two digits when it is "1". (Decimal operation is possible only with the ADC and SBC instructions.) This flag can be set and reset with the SEP and CLP instructions.



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5. Index register length flag (x)

The index register length flag determines whether index register X and index register Y are used as 16-bit registers or as 8-bit registers. The registers are used as 16-bit registers when flag x is "0" and as 8-bit registers when it is "1". This flag can be set and reset with the SEP and CLP instructions.

6. Data length flag (m)

The data length flag determines whether the data length is 16-bit or 8-bit. The data length is 16-bit when flag m is "0" and 8-bit when it is "1". This flag can be set and reset with the SEM and CLM instructions or with the SEP and CLP instructions.

7. Overflow flag (V)

The overflow flag has meaning when addition or subtraction is performed a word as signed binary number. When the data length flag m is "0", the overflow flag is set when the result of addition or subtraction is outside the range between -32768 and +32767. When the data length flag m is "1", the overflow flag is set when the result of addition or subtraction is outside the range between -128 and +127. It is reset in all other cases. The overflow flag can also be set and reset directly with the SEP, and CLV or CLP instructions.

8. Negative flag (N)

The negative flag is set when the result of arithmetic operation or data transfer is negative (If data length flag m is "0", when data bit 15 is "1". If data length flag m is "1", when data bit 7 is "1".) It is reset in all other cases. It can also be set and reset with the SEP and CLP instructions.

9. Processor interrupt priority level (IPL)

The processor interrupt priority level (IPL) consists of 3 bits and determines the priority of processor interrupts from level 0 to level 7. Interrupt is enabled when the interrupt priority of the device requesting interrupt (set using the interrupt control register) is higher than the processor interrupt priority. When interrupt is enabled, the current processor interrupt priority level is saved in a stack and the processor interrupt priority level is replaced by the interrupt priority level of the device requesting the interrupt. Refer to the section on interrupts for more details.

BUS INTERFACE UNIT

The CPU operates on an internal clock frequency which is obtained by dividing the external clock frequency $f_{(X_{\text{NN}})}$ by two. This frequency is twice the bus cycle frequency. In order to speed-up processing, a bus interface unit is used to pre-fetch instructions when the data bus is idle. The bus interface unit synchronizes the CPU and the bus and prefetches instructions. Figure 4 shows the relationship between the CPU and the bus interface unit. The bus interface unit has a program address register, a 3-byte instruction queue buffer, a data address register, and a 2-byte data buffer.

The bus interface unit obtains an instruction code from memory and stores it in the instruction queue buffer, obtains data from memory and stores it in the data buffer, or writes the data from the data buffer to the memory.

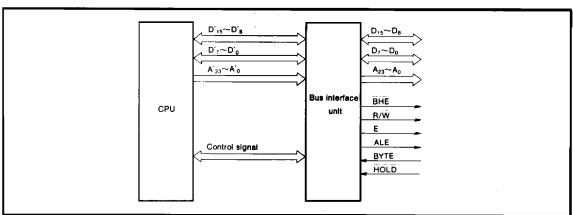


Fig. 4 Relationship between the CPU and the bus interface unit

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The bus interface unit operates using one of the waveforms (1) to (6) shown in Figure 5. The standard waveforms are (1) and (2).

The ALE signal is used to latch only the address signal from the multiplexed signal containing data and address.

The \overline{E} signal becomes "L" when the bus interface unit reads an instruction code or data from memory or when it writes data to memory. Whether to perform read or write is controlled by the R/\overline{W} signal. Read is performed when the R/\overline{W} signal is "H" state and write is performed when it is "L" state.

Waveform (1) in Figure 5 is used to access a single byte or two bytes simultaneously. To read or write two bytes simultaneously, the first address accessed must be even. Furthermore, when accessing an external memory area in memory expansion mode or microprocessor mode, set the bus width selection input pin BYTE to "L". (external data bus width to 16 bits) The internal memory area is always treated as 16-bit bus width regardless of BYTE.

When performing 16-bit data read or write, if the conditions for simultaneously accessing two bytes are not satisfied, waveform (2) is used to access each byte one by one. However, when prefetching the instruction code, if the address of the instruction code is odd, waveform (1) is used, and only one byte is read in the instruction queue buffer.

The signals A_0 and \overline{BHE} in Figure 5 are used to control these cases: 1-byte read from even address, 1-byte read from odd address, 2-byte simultaneous read from even and odd addresses, 1-byte write to even address, 1-byte write to odd address, or 2-byte simultaneous write to even and odd addresses. The A_0 signal that is the address bit 0 is "L" when an even number address is accessed. The \overline{BHE} signal becomes "L" when an odd number address is accessed.

The bit 2 of processor mode register (address $5E_{16}$) is the wait bit. When this bit is set to "0", the ALE signal and \overline{E} signal are extended and the access time is doubled when accessing an external memory area in memory expansion mode or microprocessor mode. However, these signals are not extended when an internal memory area is accessed. When the wait bit is "1", the access time is not extended for any access. Waveform (3) is an expansion of waveform (1). Waveform (4),(5), and (6) are expansion of the entire waveform (2), first half of waveform (2), and the last half of waveform (2) respectively.

Instruction code read, data read, and data write are described below.

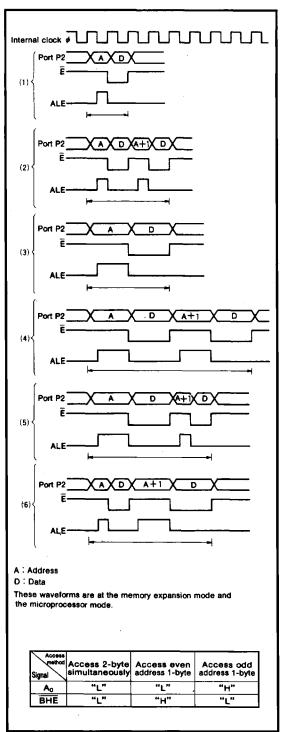


Fig. 5 Relationship between access method and signals A₀ and BHE



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Instruction code read will be described first.

The CPU obtains instruction codes from the Instruction queue buffer and executes them. The CPU notifies the bus interface unit that it is requesting an instruction code during an instruction code request cycle. If the requested Instruction code is not yet stored in the instruction queue buffer, the bus interface unit halts the CPU until it can store more instructions than requested in the instruction queue buffer. Even if there is no instruction code request from the CPU, the bus interface unit reads instruction codes from memory and stores them in the instruction queue buffer when the instruction queue buffer is empty or when only one instruction code is stored and the bus is idle on the next cycle. This is referred to as instruction pre-fetching.

Normally, when reading an instruction code from memory, if the accessed address is even the next odd address is read together with the instruction code and stored in the instruction queue buffer.

However, in memory expansion mode or microprocessor mode, if the bus width switching pin BYTE is "H", external data bus width is 8 bits and the address to be read is in external memory area is odd, only one byte is read and stored in the instruction queue buffer. Therefore, waveform (1) or (3) in Figure 5 is used for instruction code read. Data read and write are described below.

The CPU notifies the bus interface unit when performing data read or write. At this time, the bus interface unit halts the CPU if the bus interface unit is already using the bus or if there is a request with higher priority. When data read or write is enabled, the bus interface unit uses one of the waveforms from (1) to (6) in Figure 5 to perform the operation

During data read, the CPU waits until the entire data is stored in the data buffer. The bus interface unit sends the address received from the CPU to the address bus. Then it reads the memory when the \overline{E} signal is "L" and stores the result in the data buffer.

During data write, the CPU writes the data in the data buffer and the bus interface unit writes it to memory. Therefore, the CPU can proceed to the next step without waiting for write to complete. The bus interface unit sends the address received from the CPU to the address bus. Then when the \widetilde{E} signal is "L", the bus interface unit sends the data in the data buffer to the data bus and writes it to memory



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INTERRUPTS

Table 1 shows the interrupt types and the corresponding interrupt vector addresses. Reset is also treated as a type of interrupt and is discussed in this section, too.

DBC is an interrupt used during debugging.

Interrupts other than reset, \overline{DBC} , watchdog timer, zero divide, and BRK instruction all have interrupt control registers. Table 2 shows the addresses of the interrupt control registers and Figure 6 shows the bit configuration of the interrupt control register.

The interrupt request bit is automatically cleared by the hardware during reset or when processing an interrupt. Also, interrupt request bits other than $\overline{\text{DBC}}$ and watchdog timer can be cleared by software.

 $\overline{\text{INT}_2}$ to $\overline{\text{INT}_0}$ are external interrupts and whether to cause an interrupt at the input level (level sense) or at the edge (edge sense) can be selected with the level sense/edge sense selection bit. Furthermore, the polarity of the interrupt input can be selected with polarity selection bit.

Timer and UART interrupts are described in the respective section.

The priority of interrupts when multiple interrupts are caused simultaneously is partially fixed by hardware, but, it can also be adjusted by software as shown in Figure 7. The hardware priority is fixed the following:

reset > DBC > watchdog timer > other interrupts

Table 1. Interrupt types and the interrupt vector addresses

Interrupts	Vector at	dresses
A-D conversion	00FFD6 ₁₆	00FFD7 ₁₆
UART1 transmit	00FFD8 ₁₆	00FFD9 ₁₆
UART1 receive	00FFDA ₁₆	00FFDB ₁₆
UARTO transmit	00FFDC ₁₆	00FFDD ₁₆
UART0 receive	00FFDE ₁₈	00FFDF ₁₆
Timer B2	00FFE0 ₁₆	00FFE1 ₁₈
Timer B1	00FFE2 ₁₈	00FFE3 ₁₆
Timer B0	00FFE4 ₁₈	00FFE5 ₁₆
Timer A4	00FFE6 ₁₆	00FFE7 ₁₆
Timer A3	00FFE8 ₁₆	00FFE9 ₁₆
Timer A2	00FFEA ₁₆	00FFEB ₁₆
Timer A1	00FFEC ₁₈	00FFED ₁₆
Timer A0	00FFEE ₁₆	00FFEF ₁₆
INT ₂ external interrupt	00FFF0 ₁₆	00FFF1 ₁₆
INT ₁ external interrupt	00FFF2 ₁₆	00FFF3 ₁₈
INT ₀ external interrupt	00FFF4 ₁₆	00FFF5 ₁₈
Watchdog timer	00FFF6 ₁₆	00FFF7 ₁₈
DBC (unusable)	00FFF8 ₁₆	00FFF9 ₁₆
Break instruction	00FFFA ₁₆	00FFFB ₁₆
Zero divide	00FFFC ₁₆	00FFFD ₁₆
Reset	00FFFE ₁₆	00FFFF ₁₆

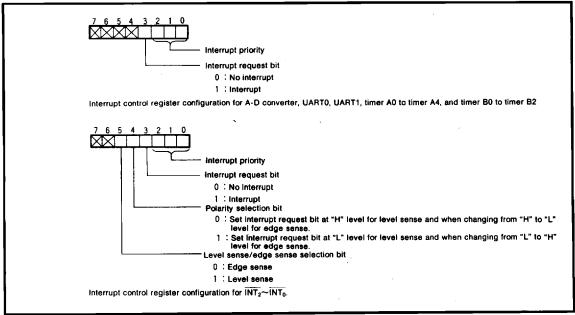


Fig. 6 Interrupt control register configuration

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Table 2. Addresses of Interrupt control registers

Interrupt control registers	Addresses
A-D conversion interrupt control register	000070 ₁₆
UARTO transmit interrupt control register	00007110
UART0 receive interrupt control register	00007216
UART1 transmit interrupt control register	00007316
UART1 receive interrupt control register	00007416
Timer A0 interrupt control register	000075 ₁₆
Timer A1 interrupt control register	000076 ₁₆
Timer A2 interrupt control register	000077 ₁₆
Timer A3 interrupt control register	000078 ₁₈
Timer A4 Interrupt control register	00007918
Timer B0 interrupt control register	00007A ₁₆
Timer B1 interrupt control register	00007B ₁₆
Timer B2 interrupt control register	00007C ₁₆
INTo interrupt control register	00007D ₁₆
INT ₁ interrupt control register	00007E ₁₆
INT ₂ Interrupt control register	00007F ₁₆

Interrupts caused by a BRK instruction and when dividing by zero are software interrupts and are not included in this list.

Other interrupts previously mentioned are A-D converter, UART, Timer, INT interrupts. The priority of these interrupts can be changed by changing the priority level in the corresponding interrupt control register by software.

Figure 8 shows a diagram of the interrupt priority resolution circuit. When an interrupt is caused, the each interrupt device compares its own priority with the priority from above and if its own priority is higher, then it sends the priority below and requests the interrupt. If the priorities are the same, the one above has priority.

This comparison is repeated to select the interrupt with the highest priority among the interrupts that are being requested. Finally the selected interrupt is compared with the processor interrupt priority level (IPL) contained in the processor status register (PS) and the request is accepted if it is higher than IPL and the interrupt disable flag I is "0". The request is not accepted if flag I is "1". The reset, DBC, and watchdog timer interrupts are not affected by the interrupt disable flag I.

When an interrupt is accepted, the contents of the processor status register (PS) is saved to the stack and the interrupt disable flag i is set to "1".

Furthermore, the interrupt request bit of the accepted interrupt is cleared to "0" and the processor interrupt priority level (IPL) in the processor status register (PS) is replaced by the priority level of the accepted interrupt.

Therefore, multi-level priority interrupts are possible by resetting the interrupt disable flag I to "0" and enable further interrupts.

For reset, DBC, watchdog timer, zero divide, and BRK instruction interrupts, which do not have an interrupt control register, the processor interrupt level (IPL) is set as shown in Table 3.

Priority resolution is performed by latching the interrupt request bit and interrupt priority level so that they do not change. They are sampled at the first half and latched at the last half of the operation code fetch cycle.

Because priority resolution takes some time, no sampling pulse is generated for a certain interval even if it is the next operation code fetch cycle.

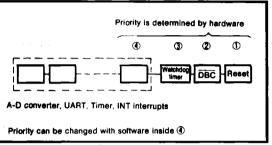


Fig. 7 Interrupt priority

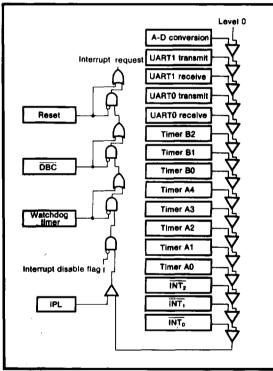


Fig. 8 Interrupt priority resolution

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As shown in Figure 9, there are three different interrupt priority resolution time from which one is selected by software. After the selected time has elapsed, the highest priority is determined and is processed after the currently executing instruction has been completed.

The time is selected with bits 4 and 5 of the processor mode register (address $5E_{10}$) shown in Figure 10. Table 4 shows the relationship between these bits and the number of cycles. After a reset, the processor mode register is initialized to "00₁₆" and therefore, the longest time is selected.

However, the shortest time may be selected by software.

Table 3. Value set in processor interrupt level (IPL) during an interrupt

Interrupt types	Setting value
Reset	. 0
DBC	7
Watchdog timer	7
Zero divide	Not change value of IPL.
BRK instruction	Not change value of IPL.

Table 4. Relationship between priority level evaluation time selection bit and number of cycles

Priority level resolution time selection bit		Mumb on at qual or
Bit 5	Bit 4	Number of cycles
0	0	7 cycles of ø
0	1	4 cycles of ø
1	0	2 cycles of ø

ø∶internal clock

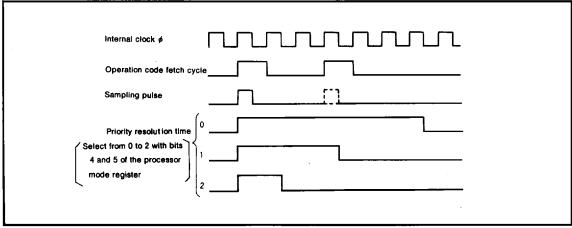


Fig. 9 Interrupt priority resolution time

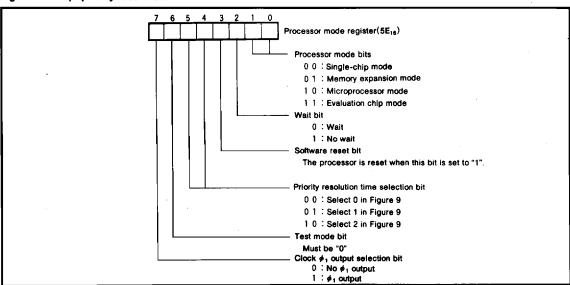


Fig. 10 Processor mode register configuration



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TIMER

There are eight 16-bit timers. They are divided by type into timer A(5) and timer B(3).

The timer I/O pins are shared with I/O pins for port P5 and P6. To use these pins as timer input pins, the data direction register bit corresponding to the pin must be cleared to "0" to specify input mode.

Using this timer, confirm the function as this timer is different a little from M37700M2-XXXFP's.

TIMER A

Figure 11 shows a block diagram of timer A.

Timer A has four modes; timer mode, event counter mode, one-shot pulse mode, and pulse width modulation mode. The mode is selected with bits 0 and 1 of the timer Ai mode register (i=0 to 4). Each of these modes is described below.

(1) **Timer** mode (00)

Figure 12 shows the bit configuration of the timer Ai mode register during timer mode. Bits 0, 1, and 5 of the timer Ai mode register must always be "0" in timer mode.

Bit 3 is ignored if bit 4 is "0".

Bits 6 and 7 are used to select the timer counter source. The counting of the selected clock starts when the count start flag is "1" and stops when it is "0".

Figure 13 shows the bit configuration of the count start flag. The counter is decremented, an interrupt is caused and the interrupt request bit in the timer Ai interrupt control register is set when the contents becomes 0000₁₆. At the same time, the contents of the reload register is transferred to the counter and count is continued.

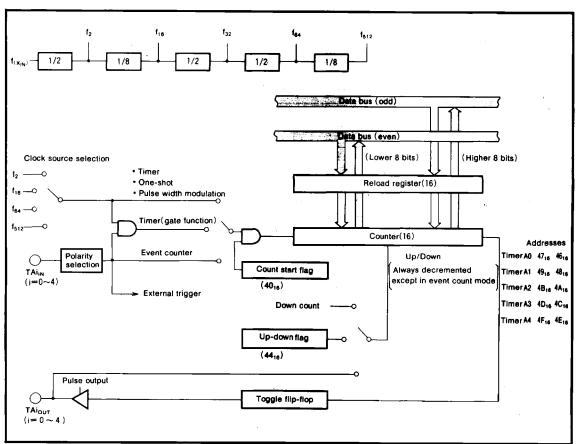


Fig. 11 Block diagram of timer A

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When bit 2 of the timer Ai mode register is "1", the output is generated from TAi_{OUT} pin. The output is toggled each time the contents of the counter reaches to 0000_{16} . When the contents of the count start flag is "0", "L" is output from TAi_{OUT} pin.

When bit 2 is "0", TAi_{OUT} can be used as a normal port pin. When bit 4 is "0", TAi_{IN} can be used as a normal port pin. When bit 4 is "1", counting is performed only while the input signal from the TAi_{IN} pin is "H" or "L" as shown in Figure 14. Therefore, this can be used to measure the pulse width of the TAi_{IN} input signal. Whether to count while the input signal is "H" or while it is "L" is determined by bit 3. If bit 3 is "1", counting is performed while the TAi_{IN} pin input

signal is "H" and if bit 3 is "0", counting is performed while it is "L" $\!\!\!$

Note that the duration of "H" or "L" on the TAi_{1N} pin must be two or more cycles of the timer count source.

When data is written to timer Ai register with timer Ai halted, the same data is also written to the reload register and the counter. When data is written to timer Ai which is busy, the data is written to the reload register, but not to the counter. The counter is reloaded with new data from the reload register at the next reload time. The contents of the counter can be read at any time.

When the value set in the timer Ai register is n, the timer frequency dividing ratio is 1/(n+1).

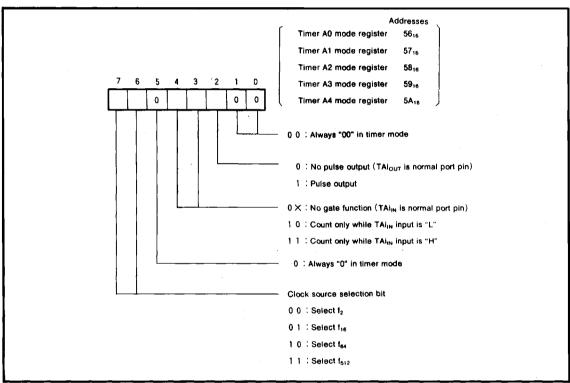


Fig. 12 Timer Ai mode register bit configuration during timer mode

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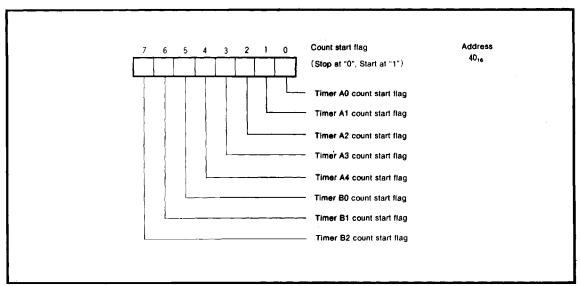


Fig. 13 Count start flag bit configuration

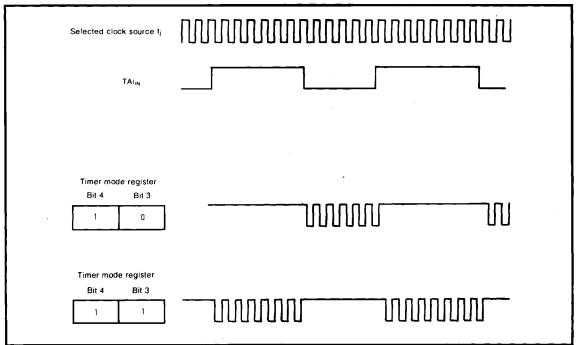


Fig. 14 Count waveform when gate function is available

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(2) Event counter mode (01)

Figure 15 shows the bit configuration of the timer Al mode register during event counter mode. In event counter mode, the bit 0 of the timer Al mode register must be "1" and bit 1 and 5 must be "0".

The input signal from the TAi_{IN} pin is counted when the count start flag shown in Figure 13 is "1" and counting is stopped when it is "0".

Count is performed at the fall of the input signal when bit 3 is "0" and at the rise of the signal when it is "1".

In event counter mode, whether to increment or decrement the count can be selected with the up-down flag or the input signal from the TAl_{OUT} pin.

When bit 4 of the timer Al mode register is "0", the updown flag is used to determine whether to increment or decrement the count (decrement when the flag is "0" and increment when it is "1"). Figure 16 shows the bit configuration of the up-down flag.

When bit 4 of the timer Ai mode register is "1", the input signal from the TAi_{OUT} pin is used to determine whether to increment or decrement the count. However, note that bit 2 must be "0" if bit 4 is "1" because if bit 2 is "1", TAi_{OUT} pin becomes an output pin with pulse output.

The count is decremented when the input signal from the TAi_{OUT} pin is "L" and incremented when it is "H". Determine the level of the input signal from the TAi_{OUT} pin before valid edge is input to the TAi_{IN} pin.

An interrupt request signal is generated and the interrupt request bit in the timer Ai interrupt control register is set when the counter reaches 0000₁₆ (decrement count) or FFFF₁₆ (increment count). At the same time, the contents of the reload register is transferred to the counter and the count is continued.

When bit 2 is "1" and the counter reaches 0000_{16} (decrement count) or FFFF₁₆ (increment count), the waveform reversing polarity is output from TAl_{OUT} pin.

If bit 2 is "0", TAi_{OUT} pin can be used as a normal port pin. However, if bit 4 is "1" and the TAi_{OUT} pin is used as an output pin, the output from the pin changes the count direction. Therefore, bit 4 should be "0" unless the output from the TAi_{OUT} pin is to be used to select the count direction.

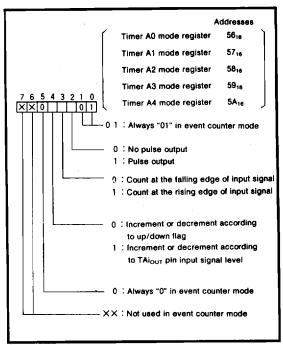


Fig. 15 Timer Al mode register bit configuration during event counter mode

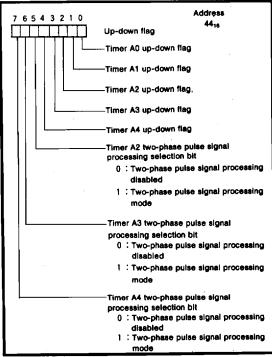


Fig. 16 Up-down flag bit configuration

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Data write and data read are performed in the same way as for timer mode. That is, when data is written to timer Ai halted, it is also written to the reload register and the counter. When data is written to timer Ai which is busy, the data is written to the reload register, but not to the counter. The counter is reloaded with new data from the reload register at the next reload time. The counter can be read at any time.

In event counter mode, whether to increment or decrement the counter can also be determined by supplying two-phase pulse input with phase shifted by 90° to timer A2, A3, or A4. There are two types of two-phase pulse processing operations. One uses timers A2 and A3, and the other uses timer A4. In either processing operation, two-phase pulse is input in the same way, that is, pulses out of phase by 90° are input at the TAj_{OUT} (j=2 to 4) pin and TAj_{IN} pin.

When timers A2 and A3 are used, as shown in Figure 17, the count is incremented when a rising edge is input to the TAk_{IN} pin after the level of TAk_{OUT} (k=2, 3) pin changes from "L" to "H", and when the falling edge is inserted, the count is decremented.

For timer A4, as shown in Figure 18, when a phase related pulse with a rising edge input to the $TA4_{IN}$ pin is input after the level of $TA4_{OUT}$ pin changes from "L" to "H", the count is incremented at the respective rising edge and falling edge of the $TA4_{OUT}$ pin and $TA4_{IN}$ pin.

When a phase related pulse with a falling edge input to the TA4_{OUT} pin is input after the level of TA4_{IN} pin changes from "H" to "L", the count is decremented at the respective rising edge and falling edge of the TA4_{IN} pin and TA4_{OUT} pin. When performing this two-phase pulse signal proces-

sing, timer Aj mode register bit 0 and bit 4 must be set to "1" and bits 1, 2, 3, and 5 must be "0". Bits 6 and 7 are ignored. Note that bits 5, 6, and 7 of the up-down flag register (44₁₅) are the two-phase pulse signal processing selection bit for timer A2, A3, and A4 respectively. Each timer operates in normal event counter mode when the corresponding bit is "0" and performs two-phase pulse signal processing when it is "1".

Count is started by setting the count start flag to "1". Data write and read are performed in the same way as for normal event counter mode. Note that the direction register of the input port must be set to input mode because two-phase pulse signal is input. Also, there can be no pulse output in this mode.

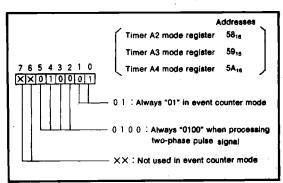


Fig. 19 Timer Aj mode register bit configuration when performing two-phase pulse signal processing in event counter mode

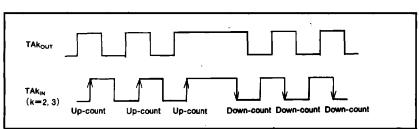


Fig. 17 Two-phase pulse processing operation of timer A2 and timer A3

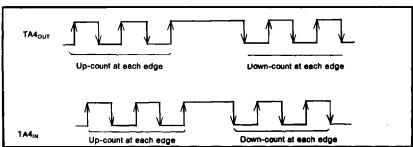


Fig. 18 Two-phase pulse processing operation of timer A4

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(3) One-shot pulse mode (10)

Figure 20 shows the bit configuration of the timer Ai mode register during one-shot pulse mode. In one-shot pulse mode, bit 0 and bit 5 must be "0" and bit 1 and bit 2 must be "1".

The trigger is enabled when the count start flag is "1". The trigger can be generated by software or it can be input from the TAi_{IN} pin. Software trigger is selected when bit 4 is "0" and the input signal from the TAi_{IN} pin is used as the trigger when it is "1".

Bit 3 is used to determine whether to trigger at the fall of the trigger signal or at the rise. The trigger is at the fall of the trigger signal when bit 3 is "0" and at the rise of the trigger signal when it is "1".

Software trigger is generated by setting the bit in the oneshot start flag corresponding to each timer.

Figure 21 shows the bit configuration of the one-shot start flag. Bit 7 of the one-shot start flag must always be "0".

As shown in Figure 22, when a trigger signal is received, the counter counts the clock selected by bits 6 and 7.

If the contents of the counter is not 0000_{16} , the TAl_{OUT} pin goes "H" when a trigger signal is received. The count direction is decrement.

When the counter reaches 0001₁₆. The TAl_{OUT} pin goes "L" and count is stopped. The contents of the reload register is transferred to the counter. At the same time, an interrupt request signal is generated and the interrupt request bit in the timer Ai interrupt control register is set. This is repeated each time a trigger signal is received. The output pulse width is

pulse frequency of the selected clock

X(counter's value at the time of trigger).

If the count start flag is "0", TAl_{OUT} goes "L". Therefore, the value corresponding to the desired pulse width must be written to timer Ai before setting the timer Ai count start flag.

As shown in Figure 23, a trigger signal can be received before the operation for the previous trigger signal is completed. In this case, the contents of the reload register is transferred to the counter by the trigger and then that value is decremented.

Except when retriggering while operating, the contents of the reload register is not transferred to the counter by triggering

When retriggering, there must be at least one timer count source cycle before a new trigger can be issued.

Data write is performed to the same way as for timer mode. When data is written in timer Al halted, it is also written to the reload register and the counter.

When data is written to timer Ai which is busy, the data is written to the reload register, but not to the counter. The counter is reloaded with new data from the reload register at the next reload time.

Undefined data is read when timer Ai is read.

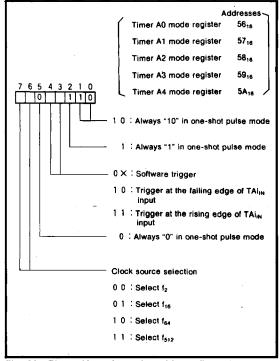


Fig. 20 Timer Ai mode register bit configuration during one-shot pulse mode

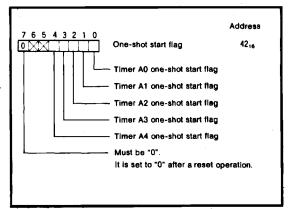


Fig. 21 One-shot start flag bit configuration

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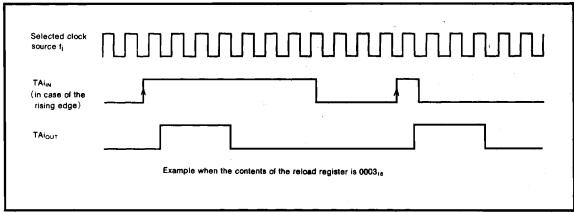


Fig. 22 Pulse output example when external rising edge is selected

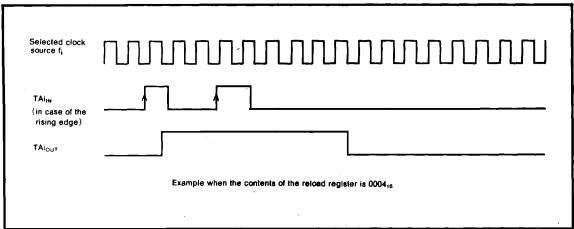


Fig. 23 Example when trigger is re-issued during pulse output



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(4) Pulse width modulation mode (11)

Figure 24 shows the bit configuration of the timer Ai mode register during pulse width modulation mode. In pulse width modulation mode. In pulse width modulation mode, bits 0, 1, and 2 must be set to "1". Bit 5 is used to determine whether to perform 16-bit length pulse width modulator or 8-bit length pulse width modulator. 16-bit length pulse width modulator. 16-bit length pulse width modulator is performed when it is "1". The 16-bit length pulse width modulator is described first.

The pulse width modulator can be started with a software trigger or with an input signal from a TAi_{IN} pin (external trigger).

The software trigger mode is selected when bit 4 is "0". Pulse width modulator is started, and pulse is output from TAi_{QUT} when the timer Ai start flag is set to "1".

The external trigger mode is selected when bit 4 is "1". Pulse width modulator starts when a trigger signal is input from the TAi_{IN} pin when the timer Ai start flag is "1". Whether to trigger at the fall or rise of the trigger signal is determined by bit 3. The trigger is at the fall of the trigger signal when bit 3 is "0" and at the rise when it is "1".

When data is written to timer Ai with the pulse width modulator halted, it is written to the reload register and the counter.

Then when the time Al start flag is set to "1" and a software trigger or an external trigger is issued to start modulation, the waveform shown in Figure 25 is output continuously. Once modulation is started, triggers are not accepted. If the value in the reload register is m, the duration "H" of pulse is

An interrupt request signal is generated and the interrupt request bit in the timer Ai interrupt control register is set at each fall of the output pulse.

The width of the output pulse is changed by updating timer data. The update can be performed at any time. The output pulse width is changed at the rise of the pulse after data is written to the timer.

The contents of the reload register are transferred to the counter just before the rise of the next pulse so that the pulse width is changed from the next output pulse.

Undefined data is read when timer Ai is read.

The 8-bit length pulse width modulator is described next.

The 8-bit length pulse width modulator is selected when the timer Ai mode register bit 5 is "1".

The reload register and the counter are both divided into 8-bit halves.

The low order 8 bits function as a prescaler and the high

order 8 bits function as the 8-bit length pulse width modulator. The prescaler counts—the clock selected by bits 6 and 7. A pulse is generated when the counter reaches 0000_{16} as shown in Figure 26. At the same time, the contents of the reload register is transferred to the counter and count is continued.

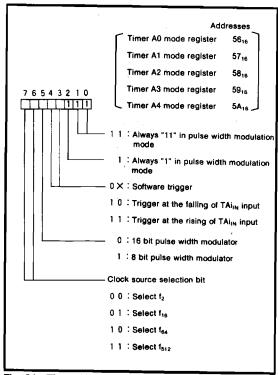


Fig. 24 Timer Al mode register bit configuration during pulse width modulation mode



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Therefore, if the low order 8-bit of the solution register is n, the period of the generated $\mu^{**}(\omega)$ is

 $\frac{1}{\text{selected clock frequency}} \times (n+1).$

The high order 8-bit function as an 8-bit length pulse width modulator using this pulse as input. The operation is the same as for 16-bit length pulse width modulator except that

the length is 8 bits. If the high order 8-bit of the reliced register is m, the duration "H" of pulse is

selected clock frequency ×(n+1)× m.

And the output pulse period is

 $\frac{1}{\text{selected clock frequency}} \times (n+1) \times (2^{\theta}-1).$

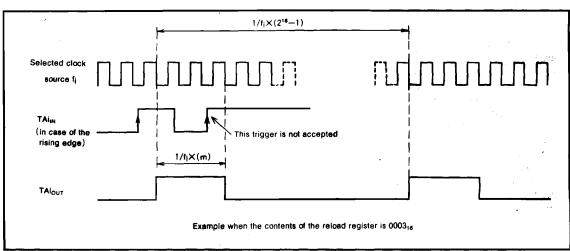


Fig. 25 16-bit length pulse width modulator output pulse example

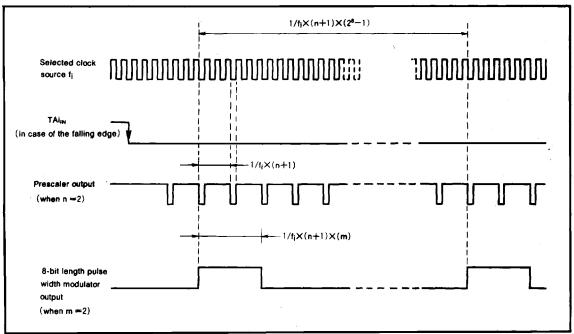


Fig. 26 8-bit length pulse width modulator output pulse example

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TIMER B

Figure 27 shows a block diagram of timer B.

Timer B has three modes; timer mode, event counter mode, and pulse period measurement/pulse width measurement mode. The mode is selected with bits 0 and 1 of the timer Bi mode register (i = 0 to 2). Each of these modes is described below.

(1) Timer mode (00)

Figure 28 shows the bit configuration of the timer Bi mode register during timer mode. Bits 0, and 1 of the timer Bi mode register must always be "0" in timer mode.

Bits 6 and 7 are used to select the clock source. The counting of the selected clock starts when the count start flag "1" and stops when "0".

As shown in Figure 13, the timer Bi count start flag is at the same address as the timer Ai count start flag. The count is decremented, an interrupt occurs, and the interrupt request bit in the timer Bi interrupt control register is set when the contents becomes 0000_{1e}. At the same time, the contents of the reload register is stored in the counter and count is continued.

Timer Bi does not have a pulse output function or a gate function like timer A.

When data is written to timer Bi halted, it is written to the reload register and the counter. When data is written to timer Bi which is busy, the data is written to the reload register, but not to the counter. The counter is reloaded with new data from the reload register at the next reload time. The contents of the counter can be read at any time.

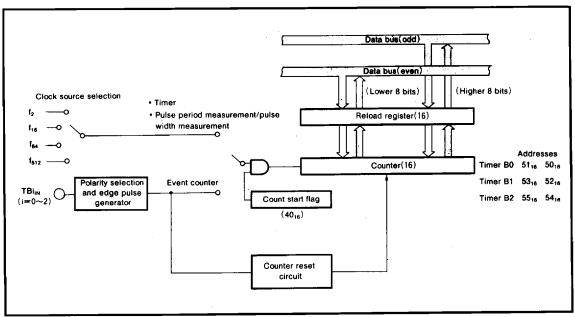


Fig. 27 Timer B block diagram

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(2) Event counter mode (01)

Figure 29 shows the bit configuration of the timer Bi mode register during event counter mode. In event counter mode, the bit 0 in the timer Bi mode register must be "1" and bit 1 must be "0".

The input signal from the TBi_{IN} pin is counted when the count start flag is "1" and counting is stopped when it is "0". Count is performed at the fall of the input signal when bits 2, and 3 are "0" and at the rise of the input signal when bit 3 is "0" and bit 2 is "1".

When bit 3 is "1" and bit 2 is "0", count Is performed at the rise and fall of the input signal.

Data write, data read and timer interrupt are performed in the same way as for timer mode.

(3) Pulse period measurement/pulse width measurement mode (10)

Figure 30 shows the bit configuration of the timer BI mode register during pulse period measurement/pulse width measurement mode.

In pulse period measurement/pulse width measurement mode, bit 0 must be "0" and bit 1 must be "1". Bits 6 and 7 are used to select the clock source. The selected clock is counted when the count start flag is "1" and counting stops when it is "0".

The pulse period measurement mode is selected when bit 3 is "0". In pulse period measurement mode, the selected clock is counted during the interval starting at the fall of the input signal from the $TBi_{\rm IN}$ pin to the next fall or at the rise of the input signal to the next rise and the result is stored in the reload register. In this case, the reload register acts as a buffer register.

When bit 2 is "0", the clock is counted from the fall of the input signal to the next fall. When bit 2 is "1", the clock is counted from the rise of the input signal to the next rise.

In the case of counting from the fall of the input signal to the next fall, counting is performed as follows. As shown in Figure 31, when the fall of the input signal from TBI_{IN} pin is detected, the contents of the counter is transferred to the reload register. Next the counter is cleared and count is started from the next clock. When the fall of the next input signal is detected, the contents of the counter is transferred to the reload register once more, the counter is cleared, and the count is started. The period from the fall of the input signal to the next fall is measured in this way.

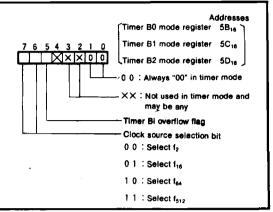


Fig. 28 Timer Bi mode register bit configuration during timer mode

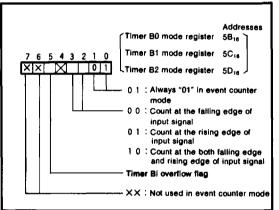


Fig. 29 Timer Bi mode register bit configuration during event counter mode

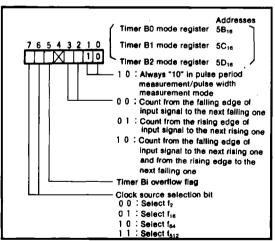


Fig. 30 Timer Bi mode register bit configuration during pulse period measurement/pulse width measurement mode



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After the contents of the counter is transferred to the reload register, an interrupt request signal is generated and the interrupt request bit in the timer Bi interrupt control register is set. However, no interrupt request signal is generated when the contents of the counter is transferred first time to the reload register after the count start flag is set to "1". When bit 3 is "1", the pulse width measurement mode is

When bit 3 is "1", the pulse width measurement mode is selected. Pulse width measurement mode is similar to pulse period measurement mode except that the clock is counted from the fall of the TBi_{IN} pin input signal to the next rise or from the rise of the input signal to the next fall as

shown in Figure 32.

When timer Bi is read, the contents of the reload register is read.

Note that in this mode, the interval between the fall of the $TBi_{\rm IN}$ pin input signal to the next rise or from the rise to the next fall must be at least two cycles of the timer count source.

Timer Bi overflow flag which is bit 5 of timer Bi mode register is set to "1" when the timer Bi counter reaches 0000₁₆. This flag is cleared by writing to corresponding timer Bi mode register.

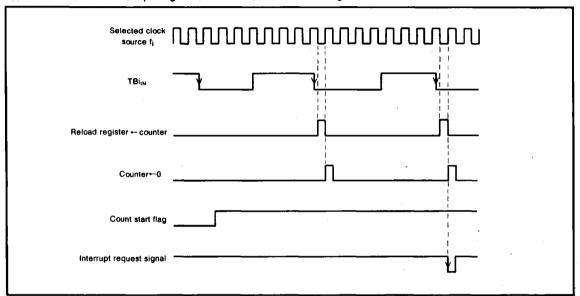


Fig. 31 Pulse period measurement mode operation (example of measuring the interval between the falling edge to next falling one)

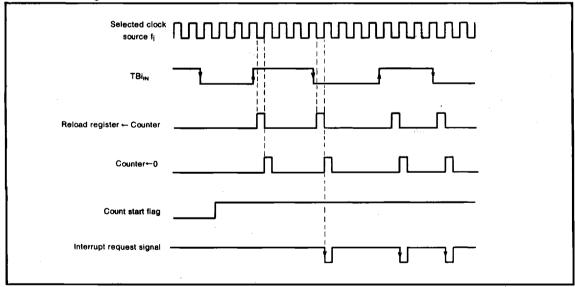


Fig. 32 Pulse width measurement mode operation

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Timer B can detect phase difference by using timer B1 and timer B0. The phase detection mode is explained below. Figure 33 shows a block diagram of the phase detection mode. In the phase detection mode, timer B1 and timer B0 are used. Set timer B1 to the timer mode and timer B0 to the pulse period measurement/pulse width measurement mode. For selection of the phase detection mode, set bit 4 of the timer B0 mode register (5B₁₆ address) to "1". Bit 5 of timer B0 mode register functions as phase detection flag by setting bit 4 to "1". Figure 34 shows the bit configuration of the timer B0 mode register and the timer B1 mode register in the phase detection mode.

Figure 35 shows an example of operation in the phase detection mode. First, each time the counter of timer B1 is set to 0000₁₆ in the timer mode of timer B1, a signal reversing polarity is generated as a reference signal. Next an external signal is input from the $\ensuremath{\mathsf{TB0_{IN}}}$ pin. By setting bit 4 of the timer B0 mode register to "1", timer B0 measures the pulse width of the logical sum (AND) signal of the reference signal generated from timer B1 and the external input signal from the TB0_{IN} pin. The bit 5 (phase detection flag) of the timer B0 mode register indicates whether the phase of the signal from the TB0_{IN} pin is ahead or behind with respect to the reference signal. The phase detection flag gets the input level from the TB0_{IN} pin at the rising from "L" to "H" of the reference signal. "0" of phase detection flag indicates that the phase of the input signal from the TB0_{IN} pin is behind with respect to the reference signal. "1" indicates that the phase of the input signal from the TBO_{IN} pin is ahead with respect to the reference signal.

To detect the phase difference between the reference signal and the input signal of the $TB0_{IN}$ pin, advance the phase of the input signal from the $TB0_{IN}$ pin with respect to the reference signal. In this state, the phase difference between the reference signal and the input signal from the

TB0_{IN} pin can be detected by measuring the pulse width by timer B0.

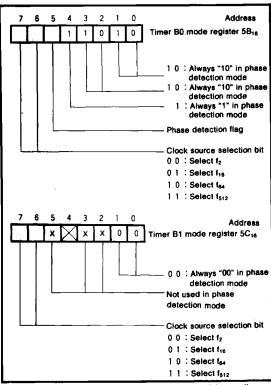


Fig. 34 Timer B0 and B1 mode register bit configuration during phase detection mode

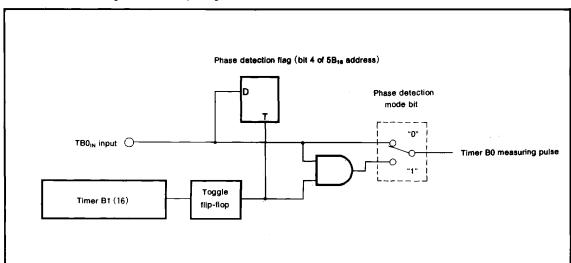


Fig. 33 Block diagram of phase detection mode

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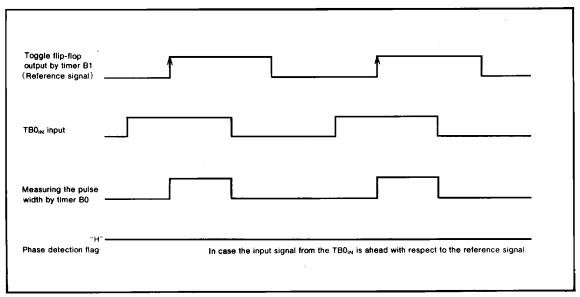


Fig. 35 Example operation of the phase detection mode

Timer function for motor control

Three-phase motor drive waveform and pulse motor drive waveform can be output using more than one incorporated timer A and timer B. The waveform output modes are explained below.

Three-phase motor drive waveform output mode (three-phase waveform mode)

The three-phase waveform mode in which four timers A0, A1, A2, and B3 are used is selected when bit 2 of the waveform output mode register shown in Figure 36 is set to "1" and, bits 1 and 0 are set to "0". In this mode, bits 3, 4, and 5 of the waveform output mode register are insignificant because they are ignored. As shown in Figure 37, timers A0, A1 and A2 must be set by the respective timer mode registers to the rising edge of external trigger signal in one-shot pulse mode is valid, and timer B2 must be set to the timer mode by the timer B2 mode register.

Figure 38 shows a block diagram in the three-phase waveform mode. In the three-phase waveform mode, six waveforms, positive waveforms (U phase, V phase, and W phase) and negative phase waveforms (\overline{U} phase, \overline{V} phase, and \overline{W} phase) are output from ports P5₆, P5₄, P5₃, P5₂, P5₁ and P5₀ with "L" level active. Among the timers used in this mode, timer A2 controls the waveforms of U and \overline{U} phases, timer A1 controls the waveforms of V and \overline{V} phases, and timer A0 controls the waveforms W and \overline{W} phases, and timer A0 controls the waveforms W and \overline{W} phases, and timer A0 controls the waveforms W and \overline{W}

er B2 controls the period of the one-shot pulse output of timers A2, A1 and A0.

In the waveform output, a short circuit prevention time can be set to prevent "L" level of three-phase waveform outputs (U phase, V phase, and W phase) from overlapping with "L" level of their negative-phase waveform outputs (\overline{U} phase, V phase, and \overline{W} phase). The short circuit prevention time is set by three eight-bit dead-time timers that share the reload register. The dead-time timers operate as one-shot timers. The dead-time timers can use both the rising and falling edge or only the falling edge of one-shot pulse generated by timer A2, A1 or A0 as the start trigger. The start trigger is selected by the bit 6 of the waveform output mode register (62₁₆ address). The start trigger is both the rising and falling edge when bit 6 is "0" and only the falling edge when bit 6 is "1".

When a value is written to the dead-time timer (63_{16} address), it is written to the reload register shared by the three dead-time timers. The dead-time timer puts the value of the reload register in the counter when the start trigger arrives from the corresponding timers, and decrements the count in f_2 (signal with source oscillation frequency divided by 2). This timer can accept the trigger again before completion of operation by the preceding trigger. In this case, after the contents of the reload register is transferred to the dead-time timer by the trigger, the value is decrement.

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The dead-time timer operates as a one-shot pulse timer. When a trigger arrives, the dead-time timer starts pulse output, and when the value of the timer reaches 00₁₆, it terminates pulse output, stops operation, and waits for the next trigger.

The output polarity of three-phase waveform depends on the output polarity setting toggle flip-flops. When the contents of the output polarity toggle flip-flops is "0", the positive phase waveform is output at "H" level, and when "1", it is output at "L" level (three-phase waveform is output using negative logic).

The output polarity setting toggle flip-flops each have output polarity setting buffers shown in Figure 39. When the contents of timer B2 counter reaches 0000_{18} , the contents of output polarity setting buffers is set in the output polarity setting toggle flip-flops. After this, the output polarity setting toggle flip-flops have polarity reversed for each termination of one-shot pulse of timer (timer A2, A1 or A0) corresponding to each phase.

An example of U phase waveform is shown in Figure 40 to explain waveform output operation. Writing "0" to the U phase waveform start level setting bit (bit 1 of 64_{16} address) and actuating timer B2 makes the three-phase waveform mode effective. When the contents of timer B2 counter reaches 0000_{16} , timer A2 starts one-shot pulse output. At this time, the contents ("0" in this case) of U phase output polarity setting buffer is set in the output polarity setting toggle filip-flop 2. At termination of one-shot pulse output of timer A2, the contents of the output polarity setting toggle filip-flop 2 changes from "0" to "1" and a one-shot pulse of the eight-bit dead-time timer is output to set a time so that the "L" level of U phase waveform and $\overline{\rm U}$ phase waveform with the negative phase of U phase waveform does not overlap.

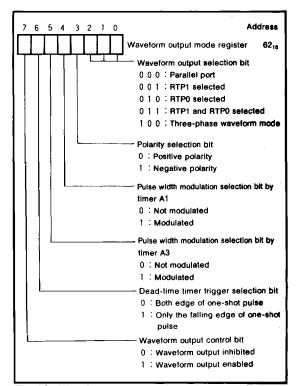


Fig. 36 Waveform output mode register bit configuration

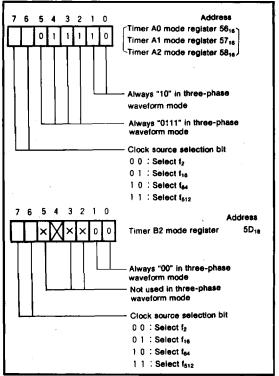


Fig. 37 Timer A0, A1, A2 mode register and timer B2 mode register bit configuration



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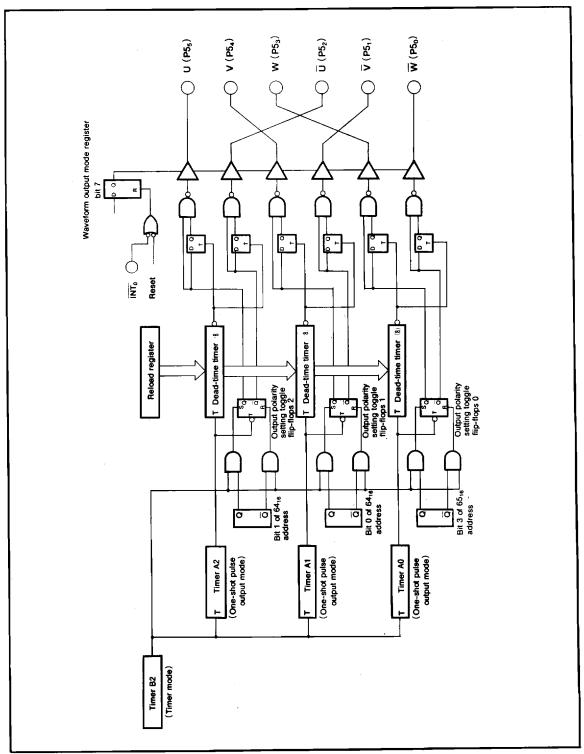


Fig. 38 Block diagram in three-phase waveform mode

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The U-phase waveform output that began at "H" level remains at "H" level until termination of the one-shot pulse output of the dead-time timer, even when the contents of the output polarity setting toggle flip-flop 2 changes from "0" to "1" due to one-shot pulse output of timer A2. At termination of the one-shot pulse output of the dead-time timer, "1" of the output polarity setting toggle flip-flop 2 already reversed becomes effective and the U-phase waveform changes to "L" level. Next write "1" again to the U-phase output polarity setting buffer (bit 1 of 6416 address) before the counter of timer B2 reaches 000018. When the counter of timer B2 reaches 000018, the one-shot pulse output of timer B2 begins to operate. At the same time, "1" written to the U-phase output polarity setting buffer is set in the output polarity setting toggle flip-flop 2 and the U-phase waveform output remains at "L" level. At termination of the one-shot pulse output of timer A2, the contents of the output polarity setting toggle flip-flop 2 changes from "1" to "0" and the one-shot pulse output of the deadtime timer begins to operate. The U-phase waveform output, when the contents of the output polarity setting toggle flip-flop changes from "1" to "0", changes form "L" to "H" without waiting for termination of the one-shot pulse output of the dead-time timer.

U-phase waveform is generated by repeating the above operation. U-phase waveform with the negative phase of U-phase waveform is generated in the same way as U-phase waveform, except that the signal contents of the output polarity setting toggle flip-flop 2 is the very reverse of that in U-phase waveform. In this way, U-phase waveform and U-phase waveform with the negative phase are generated from the pins so that the "L" level does not overlap.

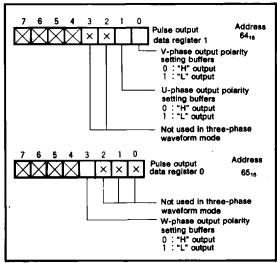


Fig. 39 Pulse output data register 0, 1 in three-phase waveform mode

The width of "L" level can be changed by changing the value of timer B2 and the value of timer A2. This technique for generating waveforms with "L" level not overlapping is also applicable to V phase, W phase, and their negative phases, \overline{V} phase and \overline{W} phase, by using corresponding timers.

The above explanation is for an example of generating three-phase waveform by the triangular wave modulation (called double edge modulation), but three-phase waveform by the saw-tooth-wave modulation (called signal edge modulation) can also be generated by fixing the start level of each phase.

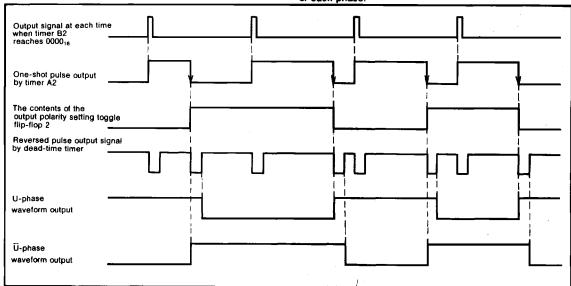


Fig. 40 Example of U-phase waveform output (three-phase waveform by triangular wave modulation)

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Three-phase waveforms (U phase, V phase, and W phase) generated in this way and their negative-phase waveforms (\overline{U} phase, \overline{V} phase, and \overline{W} phase) are output from each port by setting the waveform output control bit (bit 7) of the waveform output mode register to "1". Setting this bit to "0" places a port into floating states. This bit can be set to "0" by instructions, by inputting a falling edge to the $\overline{INT_0}$ input pin of external interrupt, or reset.

Pulse output port mode

Figure 41 shows a block diagram for pulse output port mode. In the pulse output port mode, two pairs of four-bit pulse output ports are used. Whether using pulse output port or not can be selected by waveform output selection bit (bit 0, bit 1, bit 2) of waveform output mode register (62₁₆ address) shown in Figure 36. When bit 2 of waveform output selection bit is set to "0" and bit 0 is set to "1", ports P6₀, P5₆, P5₅ and P5₄ are used as pulse output ports (RTP1 selected), and when bit 2 of waveform output selection bit is set to "0" and bit 1 is set to "1", ports P5₃, P5₂, P5₁, and P5₀ are used as pulse output ports (PTP0 selected). When

bit 2 of waveform output selection bits is set to "0" and bits 1 and 0 are set to "1", ports $P6_0$, $P5_0$, $P5_5$, and $P5_4$, and ports $P5_3$, $P5_2$, $P5_1$ and $P5_0$ are used as pulse output ports (RTP1 and RTP0 selected).

The ports not used as pulse output ports can be used as normal parallel ports or timer input/output.

In the pulse output port mode, set timers A2 and A0 to timer mode as timers A2 and A0 are used. Figure 42 shows the bit configuration of timer A0, A2 mode registers in pulse output port mode.

Data can be set in each bit of the pulse output data register corresponding to four ports selected as pulse output ports. Figure 43 shows the bit configuration of the pulse output data register. The contents of the pulse output data register 1 (low-order four bits of 64₁₆ address) corresponding to ports P6₀, P5₆, P5₅ and P5₄ is output to the ports each time the counter of timer A2 becomes 0000₁₆. The contents of the pulse output data register 0 (low-order four bits of 65₁₆ address) corresponding to ports P5₃, P5₂, P5₁, and P5₀ is output to the ports each time the counter of timer A0 becomes 0000₁₆.

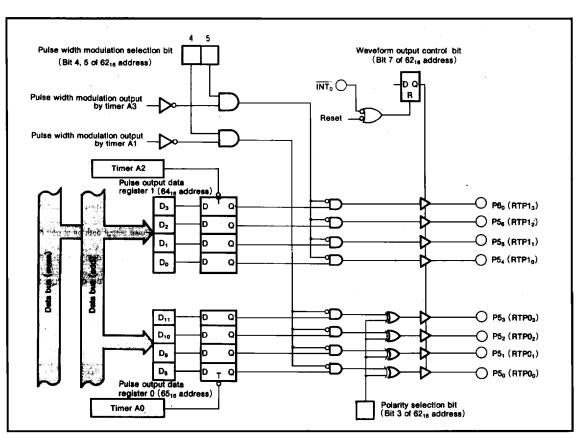


Fig. 41 Block diagram for pulse output port mode

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When "0" is written to a specified bit of the pulse output data register, "L" level is output to the corresponding pulse output port when the counter of corresponding timer becomes 0000₁₆, and when "1" is written, "H" level is output to the pulse output port.

Pulse width modulation can be applied to each pulse output port. Since pulse width modulation involves the use of timers A3 and A1, activate these timers in pulse width modulation mode. When a certain bit of the pulse output register is "1", pulse width modulation is output from the pulse output port when the counter of the corresponding timer becomes 0000₁₆.

Ports P6 $_0$, P5 $_5$, P5 $_5$ and P5 $_4$ are applied pulse width modulation by timer A3 by setting the pulse width modulation selection bit by timer A3 (bit 5) of the waveform output mode register to "1".

Ports $P5_3$, $P5_2$, $P5_1$ and $P5_0$ are applied pulse width modulation by timer A1 by setting the pulse width modulation selection bit by timer A1 (bit 4) of the waveform output mode register to "1".

The contents of the pulse output data register 0 can be reversed and output to pulse output ports $P5_3$, $P5_2$, $P5_1$ and $P5_0$ by the polarity selection bit (bit 3) of the waveform output mode register. When the polarity selection bit is "0", the contents of the pulse output data register 0 is output unchangeably, and when "1", the contents of the pulse output data register 0 is reversed and output. When pulse width modulation is applied, likewise the polarity reverse to pulse width modulation can be selected by the polarity selection bit.

Figure 44 shows example of waveforms in pulse output port mode.

Ports selecting the pulse output port mode can control output as in the three-phase wavefrom mode by the waveform output control bit (bit 7) of the waveform output mode register (62₁₆ address).

When the waveform output control bit is set to "1", a waveform is output from the port. When this bit is set to "0", waveform output from the port is stopped and the port is placed in floating state.

This bit can be set to "0" by instructions, by inputting a falling edge to the $\overline{\text{INT}_0}$ pin, or reset.

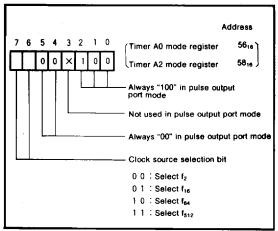


Fig. 42 Timer A0, A2 mode register bit configuration in pulse output port mode

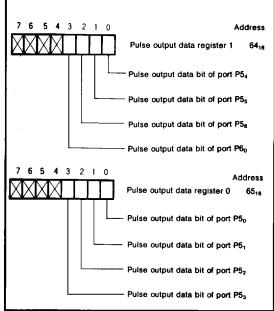


Fig. 43 Pulse output data register bit configuration

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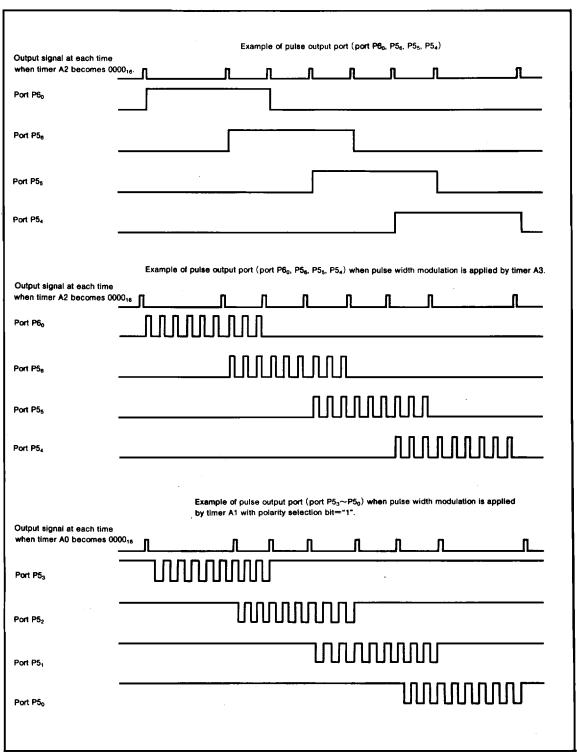


Fig. 44 Example of waveforms in pulse output port mode

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SERIAL I/O PORTS

Two independent serial I/O ports are provided. Figure 45 shows a block diagram of the serial I/O ports.

Bits 0, 1, and 2 of the UARTi (i = 0, 1) Transmit/Receive mode register shown in Figure 46 are used to determine whether to use port P8 as parallel port, clock synchronous serial I/O port, or asynchronous (UART) serial I/O port us-

ing start and stop bits.

Figures 47 and 48 show the connections of receiver/transmitter according to the mode.

Figure 49 shows the bit configuration of the UARTi transmit/receive control register.

Each communication method is described below.

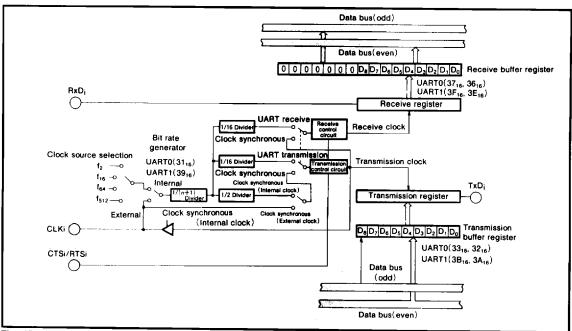


Fig. 45 Serial I/O port block diagram

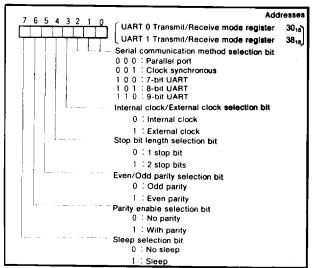


Fig. 46 UART I Transmit/Receive mode register bit configuration



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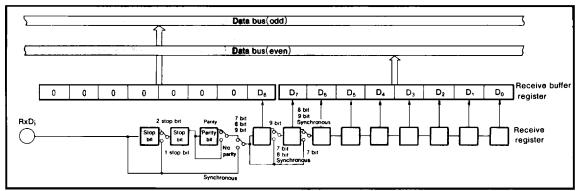


Fig. 47 Receiver block diagram

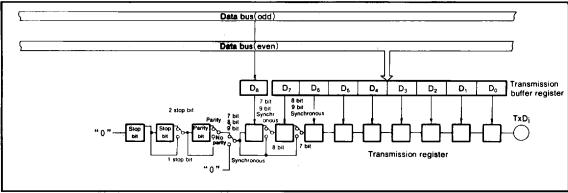


Fig. 48 Transmitter block diagram

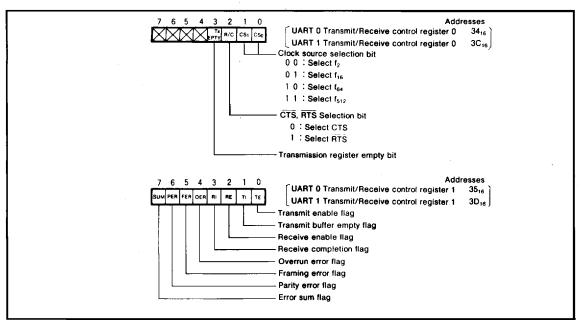


Fig. 49 UARTI Transmit/Receive control register bit configuration

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CLOCK SYNCHRONOUS SERIAL COMMUNICATION

A case where communication is performed between two clock synchronous serial I/O ports as shown in Figure 50 will be described. (The transmission side will be denoted by subscript j and the receiving side will be denoted by subscript k.)

Bit 0 of the UART; transmit/receive mode register and UARTk transmit/receive mode register must be set to "1" and bits 1 and 2 must be "0". The length of the transmission data is fixed at 8 bits.

Bit 3 of the UARTj transmit/receive mode register of the clock sending side is cleared to "0" to select the internal clock. Bit 3 of the UARTk transmit/receive mode register of the clock receiving side is set to "1" to select the external clock. Bits 4, 5 and 6 are ignored in clock synchronous mode. Bit 7 must always be "0".

The clock source is selected by bit 0 (CS_0) and bit 1 (CS_1) of the clock sending side UARTj transmit/receive control register 0. As shown in Figure 45, the selected clock is divided by (n + 1), then by 2, passed through a transmisson control circuit, and output as transmisson clock CLKj. Therefore, when the selected clock is fi.

Bit Rate=fi/ $\{(n+1)\times 2\}$

On the clock receiving side, the CS₀ and CS₁ bits of the UARTk transmit/receive control register are ignored because an external clock is selected.

The bit 2 of the clock sending side UARTj transmit/receive control register is clear to "0"to select CTSj input. The bit 2 of the clock receiving side is set to "1" to select RTSk output. CTS, and RTS signals are described later.

Transmission

Transmission is started when the bit 0 (TEj flag) of UARTj transmit/receive control register 1 is "1", bit 1 is (TIj flag) of one is "0", and CTSj input is "L". As shown in Flgure 51, data is output from TxDj pin when transmission clock CLKj changes from "H" to "L". The data is output from the least significant bit.

The TIj flag indicates whether the transmission buffer register is empty or not. It is cleared to "0" when data is written in the transmission buffer register and set to "1" when the contents of the transmission buffer register is transferred to the transmission register.

When the transmission register becomes empty after the contents has been transmitted, data is transferred automatically from the transmission buffer register to the transmission register if the next transmission start condition is satisfied. If the bit 2 of UARTj transmit/receive control register 0 is "1", CTSj input is ignored and transmission start is controlled only by the TEj flag and Tlj flag. Once transmission has started, the TEj flag, Tlj flag, and CTSj signals are ignored until data transmission completes. Therefore, trans-

mission is not interrupt when CTSj input is changed to "H" during transmission.

The transmission start condition indicated by TEj flag, TIj flag, and $\overline{\text{CTS}}$ j is checked while the T_{END} j signal shown in Figure 51 is "H". Therefore, data can be transmitted continuously if the next transmission data is written in the transmission buffer register and Tij flag is cleared to "0" before the T_{END} j signal goes "H".

The bit 3 (TxEPTY) flag) of UARTj transmit/receive control register 0 changes to "1" at the next cycle after the $T_{\rm ENDj}$ signal goes "H" and changes to "0" when transmission starts. Therefore, this flag can be used to determine whether data transmission has completed.

When the Tij flag changes from "0" to "1", the interrupt request bit in the UARTj transmission interrupt control register is set to "1".

Receive

Receive starts when the bit 2 (RE_K flag) of UART_K transmit/receive control register 1 is set to "1".

The $\overline{RTS_k}$ output is "H" when the RE_k flag is "0" and goes "L" when the RE_k flag changed to "1". It goes back to "H" when receive starts. Therefore, the $\overline{RTS_k}$ output can be used to determine whether the receive register is ready to receive. It is ready when $\overline{RTS_k}$ output is "L".

The data from the RxDk pin is retrieved and the contents of the receive register is shifted by 1 bit each time the transmission clock CLKj changes from "L" to"H". When an 8-bit data is received, the contents of the receive register is transferred to the receive buffer register and the bit 3 (RIk flag) of UARTk transmit/receive control register 1 is set to "1". In other words, the setting of the Rik flag indicates that the receive buffer register contains the received data. At this point, RTSj output goes "L" to indicate that the next data can be received. When the RIk flag changes from "0" to "1", the interrupt request bit in the UARTk receive interrupt control register is set to "1". Bit 4 (OERk flag) of UART_k transmit/receive control register is set to "1" when the next data is transferred from the receive register to the receive buffer register while RIk flag is "1", and indicates that the next data was transferred to the receive register before the contents of the receive buffer register was read. Rik and OERk flags are cleared automatically to "0" when the low-order byte of the receive buffer register is read. The OERk flag is also cleared when the REk flag is cleared. Bit 5 (FERk flag), bit 6 (PERk flag), and bit 7 (SUM_k flag) are ignored in clock synchronous mode.

As shown in Figure 50, with clock synchronous serial communication, data cannot be received unless the transmitter is operating because the receive clock is created from the transmission clock. Therefore, the transmitter must be operating even when there is no data to be sent from UART $_{\rm K}$ to UARTI.



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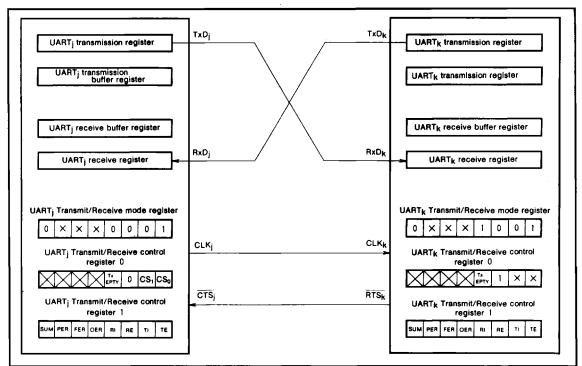


Fig. 50 Clock synchronous serial communication

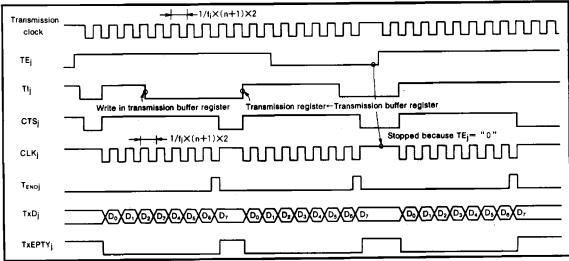


Fig. 51 Clock synchronous serial I/O timing

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ASYNCHRONOUS SERIAL COMMUNICATION

Asynchronous serial communication can be performed using 7-, 8-, or 9-bit length data. The operation is the same for all data lengths. The following is the description for 8-bit asynchronous communication.

With 8-bit asynchronous communication, the bit 0 of UARTI transmit/receive mode register is "1", the bit 1 is "0", and the bit 2 is "1".

Bit 3 is used to select an internal clock or an external clock. If bit 3 is "0", an internal clock is selected and if bit 3 is "1", then external clock is selected. If an internal clock is selected, the bit 0 (CS_0) and bit 1 (CS_1) of UARTi transmit/receive control register 0 are used to select the clock source. When an internal clock is selected for asynchronous serial communication, the CLK pin can be used as a normal I/O pin.

The selected internal or external clock is divided by (n+1), then by 16, and passed through a control circuit to create the UART transmission clock or UART receive clock.

Therefore, the transmission speed can be changed by changing the contents n of the bit rate generator. If the selected clock is an internal clock fi or an external clock fext.

Bit Rate = $(f_i \text{ or } f_{EXT})/\{(n+1)\times 16\}$

Bit 4 is the stop bit length selection bit to select 1 stop bit or 2 stop bits.

The bit 5 is a selection bit of odd parity or even parity. In the odd parity mode, the parity bit is adjusted so that the sum of the 1's in the data and parity bit is always odd.

In the even parity mode, the parity bit is adjusted so that the sum of the 1's in the data and parity bit is always even.

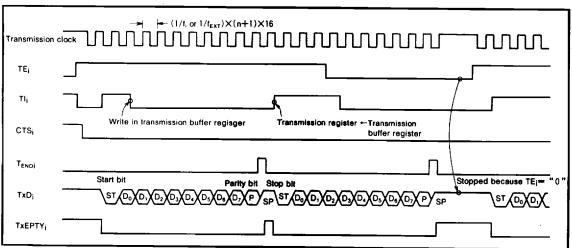


Fig. 52 Transmit timing example when 8-bit asynchronous communication with parity and 1 stop bit is selected

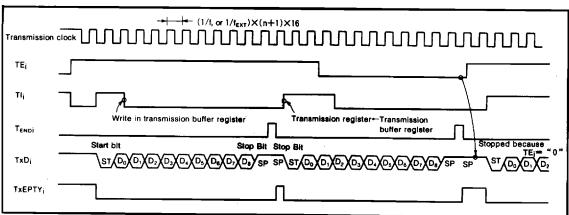


Fig. 53 Transmit timing example when 9-bit asynchronous communication with no parity and 2 stop bits is selected

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Bit 6 is the parity bit selection bit which indicates whether to add parity bit or not.

Bits 4 to 6 should be set or reset according to the data format of the communicating devices.

Bit 7 is the sleep selection bit. The sleep mode is described later

The UART_i transmit/receive control regisger 0 bit 2 is used to determine whether to use $\overline{CTS_i}$ input or $\overline{RTS_i}$ output. $\overline{CTS_i}$ input used if bit 2 is "0" and $\overline{RTS_i}$ output is used if bit 2 is "1".

If $\overline{CTS_i}$ input is selected, the user can control whether to stop or start transmission by external $\overline{CTS_i}$ input. $\overline{RTS_i}$ will be described later.

Transmission

Transmission is started when the bit 0 (TEi flag) of UART_i transmit/receive control register 1 is "1", the bit 1 (TI_i flag) is "0", and CTS_i input is "L" if CTS_i input is selected. As shown in Figure 52 and 53, data is output from the TxD_i pin with the stop bit and parity bit specified by the bits 4 to 6 of UART_i transmit/receive mode register bits. The data is output from the least significant bit.

The TI_i flag indicates whether the transmission butter is empty or not. It is cleared to "0" when data is written in the transmission buffer and set to "1" when the contents of the transmission buffer register is transferred to the transmission register.

When the transmission register becomes empty after the contents has been transmitted, data is transferred automatically form the transmission buffer register to the transmission register if the next transmission start condition is satisfied.

Once transmission has started, the TE_i flag, TI_i flag, and $\overline{CTS_i}$ signal (if $\overline{CTS_i}$ input is selected) are ignored until data transmission is completed.

Therefore, transmission does not stop until it completes even if the TE; flag is cleared during transmission.

The transmission start condition indicated by TE_I flag, TI_I flag, and $\overline{\text{CTS}_{\text{I}}}$ is checked while the T_{ENDI} signal shown in Figure 52 is "H". Therefore, data can be transmitted continuously if the next transmission data is written in the transmission butter register and TI_I flag is cleared to 0 before the T_{ENDI} signal goes "H".

The bit 3 (TxEPTY_I flag) of UART_I transmit/receive control register 0 changes to "1" at the next cycle after the $T_{\rm ENDI}$ signal goes "H" and changes to "0" when transmission starts. Therefore, this flag can be used to determine whether data transmission is completed.

When the Tij flag changes from "0" to "1", the interrupt request bit in the UARTj transmissoin interrupt control register is set to "1".

Receive

Receive is enabled when the bit 2 (RE; flag) of UART; transmit/receive control register 1 is set. As shown in Figure 54, the frequency divider circuit at the receiving end begin to work when a start bit is arrived and the data is received.

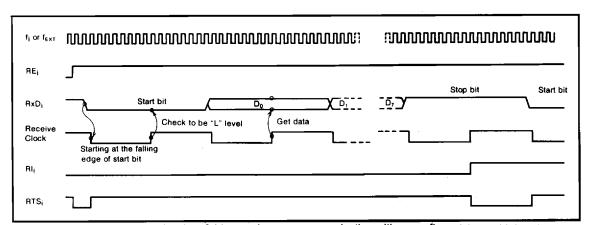


Fig. 54 Receive timing example when 8-bit asynchronous communication with no parity and 1 stop bit is selected

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If RTS_i output is selected by setting the bit 2 of UART_i transmit/receive control register 0 to "1", the RTSi output is "H" when the RE_i flag is "0". When the RE_i flag changes to "1", the RTSi output goes "L" to indicate receive ready and returns to "H" once receive has started. In other words, RTS_i output can be used to determine externally whether the receive register is ready to receive.

The entire transmission data bits are received when the start bit passes the final bit of the receive block shown in Figure 33. At this point, the contents of the receive register is transferred to the receive buffer register and the bit 3 of UART; transmit/receive control register 1 is set. In other words, the RI; flag indicates that the receive buffer register contains data when it is set. If RTS; output is selected, RTS; output goes "L" to indicate that the register is ready to receive the next data.

The interrupt request bit in the UART_i receive interrupt control register is set when the RI_i flag changes from "0" to "1"

The bit 4 (OER_i flag) of UART_i transmission control register 1 is set when the next data is transferred from the receive register to the receive buffer register while the Rl_i flag is "1". In other words when an overrun error occurs. If the OER_i flag is "1", it indicates that the next data has been transferred to the receive buffer register before the contents of the receive butter register has been read.

Bit 5 (FER; flag) is set when the number of stop bits is less than required (framing error).

Bit 6 (PER; flag) is set when a parity error occurs.

Bit 7 (SUM_i flag) is set when either the OER_i flag, FER_i flag, or the PER_i flag is set. Therefore, the SUM_i flag can be used to determine whether there is an error.

The setting of the RI; flag, OER; flag, FER; flag, and the PERi flag is performed while transferring the contents of the receive register to the receive buffer register. The RI; OERi, FERi, PERi, and SUM; flags are cleared when the low order byte of the receive buffer register is read or when the RE; flag is cleared.

Sleep mode

The sleep mode is used to communicate only between certain microcomputers when multiple microcomputers are connected through serial I/O.

The sleep mode is entered when the bit 7 of UART; transmit/receive mode register is set.

The operation of the sleep mode for an 8-bit asynchronous communication is described below.

When sleep mode is selected, the contents of the receive register is not transferred to the receive buffer register if bit 7 (bit 6 if 7-bit asynchronous communication and bit 8 if 9-bit asynchronous communication) of the received data is "0". Also the RI_i, OER_i, FER_i, PER_i, and the SUM_i flag are unchanged. Therefore, the interrupt request bit of the UART_i receive interrupt control register is also unchanged.

Normal receive operation takes place when bit 7 of the received data is "1".

The following is an example of how the sleep mode can be used.

The main microcomputer first sends data with bit 7 set to "1" and bits 0 to 6 set to the address of the subordinate microcomputer which wants to communicate with. Then all subordinate microcomputers receive the same data. Each subordinate microcomputer checks the received data, clears the sleep bit if bits 0 to 6 are its own address and sets the sleep bit if not. Next the main microcomputer sends data with bit 7 cleared. Then the microcomputer with the sleep bit cleared will receive the data, but the microcomputer with the sleep bit set will not. In this way, the main microcomputer is able to communicate with only the designated microcomputer.



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A-D CONVERTER

The A-D converter is an 8-bit successive approximation converter.

Figure 55 shows a block diagram of the A-D converter and Figure 56 shows the bit configuration of the A-D control register. The frequency of the A-D converter operating clock ϕ_{AD} is selected by the bit 7 of the A-D control register. When bit 7 is "0", ϕ_{AD} is the clock frequency divided by 8. That is, ϕ_{AD} =f(X_{IN})/8. When bit 7 is "1", ϕ_{AD} is the clock frequency divided by 4 and ϕ_{AD} is=f(X_{IN})/4. The ϕ_{AD} during A-D conversion must be 250KHz minimum because the comparator consists of a capacity coupling amplifier.

The operating mode is selected by the bits 3 and 4 of A-D control register. The available operating modes are one-shot, repeat, single sweep, and repeat sweep.

The bit of data direction register bit corresponding to the A-D converter pin must be "0" (input mode) because the analog input port is shared with port P7.

The operation of each mode is described below.

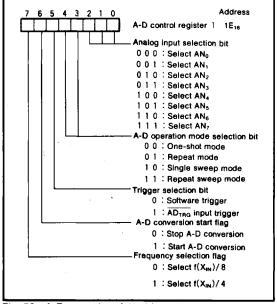


Fig. 56 A-D control register bit configuration

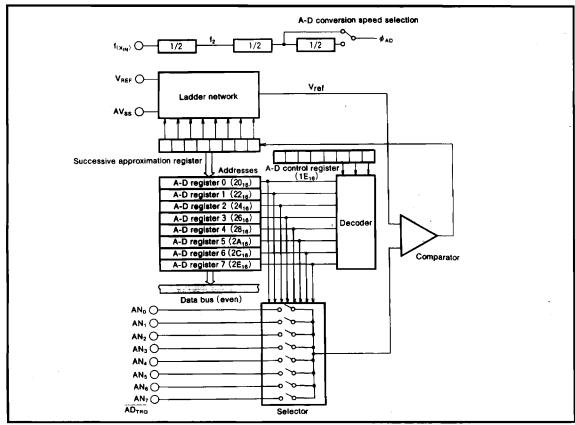


Fig. 55 A-D converter block diagram

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(1) One-shot mode (00)

The A-D conversion pins are selected with the bit 0 to 2 of A-D control register. A-D conversion can be started by a software trigger or by an external trigger.

A software trigger is selected when the bit 5 of A-D control register is "0" and an external trigger is selected when it is "1".

When a software trigger is selected, A-D conversion is started when bit 6 (A-D conversion start flag) is set. A-D conversion ends after 57 ϕ_{AD} cycles and an interrupt request bit is set in the A-D conversion interrupt control register. At the same time, A-D control register bit 6 (A-D conversion start flag) is cleared and A-D conversion stops. The result of A-D conversion is stored in the A-D register corresponding to the selected pin.

If an external trigger is selected, A-D conversion starts when the A-D conversion start flag is "1" and the $\overline{AD_{TRG}}$ input changes from "H" to "L". In this case, the pins that can be used for A-D conversion are AN_0 to AN_6 because the $\overline{AD_{TRG}}$ pin is shared with the analog voltage input pin AN_7 . The operation is the same as with software trigger except that the A-D conversion start flag is not cleared after A-D conversion and a retrigger can be available during A-D conversion.

(2) Repeat mode (01)

The operation of this mode is the same as the operation of one-shot mode except that when A-D conversion of the selected pin is complete and the result is stored in the A-D register, conversion does not stop, but is repeated. Also, no interrupt request is issued in this mode. Furthermore, If software trigger is selected, the A-D conversion start flag is not cleared. The contents of the A-D register can be read at any time.

(3) Single sweep mode [10]

In the sweep mode, the number of analog input plns to be swept can be selected. Analog input pins are selected by bits 1 and 0 of the A-D sweep pin selection register (1 F_{18} address) shown in Figure 57. Two pins, four plns, six pins, or eight pins can be selected as analog input pins, depending on the contents of these bits.

A-D conversion is performed only for selected input pins. After A-D conversion is performed for input of AN_0 pin, the conversion result is stored in A-D register 0, and in the same way, A-D conversion is performed for selected pins one after another. After A-D conversion is performed for all selected pins, the sweep is stopped.

A-D conversion can be started with a software trigger or with an external trigger input. A software trigger is selected when bit 5 is "0" and an external trigger is selected when it is "1"

When a software trigger is selected, A-D conversion is started when A-D control register bit 6 (A-D conversion start flag) is set. When A-D conversion of all selected pins end, an interrupt request bit is set in the A-D conversion in-

terrupt control register. At the same time, A-D control register bit 6 (A-D conversion start flag) is cleared and A-D conversion stops.

When an external trigger is selected, A-D conversion starts when the A-D conversion start flag is "1" and the $\overline{AD_{TRG}}$ input changes from "H" to "L". In this case, the A-D conversion result of the trigger input itself is stored in the A-D register 7 because the $\overline{AD_{TRG}}$ pin is shared with AN₇ pin.

The operation is the same as done by software trigger except that the A-D conversion start flag is not cleared after A-D conversion and a retrigger can be available during A-D conversion.

(4) Repeat sweep mode [11]

The difference with the single sweep mode is that A-D conversion does not stop after converting from the AN_0 pin to the selected pins, but repeats again from the AN_0 pin. The repeat is performed among the selected pins. Also, no interrupt request is generated. Furthermore, if software trigger is selected, the A-D conversion start flag is not cleared. The A-D register can be read at any time.

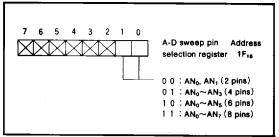


Fig. 57 A-D sweep pin selection register configuration

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WATCHDOG TIMER

The watchdog timer is used to detect unexpected execution sequence caused by software run-away.

Figure 58 shows a block diagram of the watchdog timer. The watchdog timer consists of a 12-bit binary counter.

The watchdog timer counts the clock frequency divided by $32 \ (f_{32})$ or by $512 \ (f_{512})$. Whether to count f_{32} or f_{512} is determined by the watchdog timer frequency selection flag shown in Figure 59. f_{512} is selected when the flag is "0" and f_{32} is selected when it is "1". The flag is cleared after reset. FFF₁₆ is set in the watchdog timer when "L" or $2V_{CC}$ is applied to the RESET pin, STP instruction is executed, data is written to the watchdog timer, or the most significant bit of the watchdog timer become "0".

After FFF $_{16}$ is set in the watchdog timer, the contents of watchdog timer is decremented by one at every cyle of selected frequency f_{32} or f_{512} , and after 2048 counts, the most significant bit of watchdog timer become "0", and a watchdog timer interrupt request bit is set, and FFF $_{16}$ is preset in the watchdog timer.

Normally, a program is witten so that data is written in the watchdog timer before the most significant bit of the watchdog timer become "0". If this routine is not executed due to unexpected program execution, the most significant bit of the watchdog timer become eventually "0" and an interrupt is generated.

The processor can be reset by setting the bit 3 (software reset bit) of processor mode register described in Figure 10 in the interrupt section and generating a reset pulse.

The watchdog timer stops its function when the $\overline{\text{RESET}}$ pin voltage is raised to double the V_{CC} voltage.

The watchdog timer can also be used to recover from when the clock is stopped by the STP Instruction. Refer to the section on clock generation circuit for more details.

The watchdog timer hold the contents during a hold state and the frequency is stopped to input.

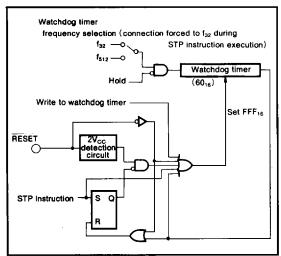


Fig. 58 Watchdog timer block diagram

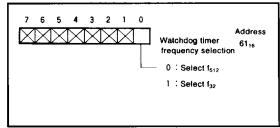


Fig. 59 Watchdog timer frequency selection flag

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RESET CIRCUIT

Reset occurs when the $\overline{\text{RESET}}$ pin is returned to "H" level after holding it at "L" level when the power voltage is at 5V \pm 10%. Program execution starts at the address formed by setting the address pins $A_{23} \sim A_{16}$ to 00_{16} . $A_{15} \sim A_{8}$ to the contents of address FFFF₁₆, and $A_{7} \sim A_{0}$ to the contents of address FFFE₁₆.

Figure 60 shows the status of the internal registers when a reset occurs.

Figure 61 shows an example of a reset circuit. The reset input voltage must be held 0.9V or lower when the power voltage reaches 4.5V.

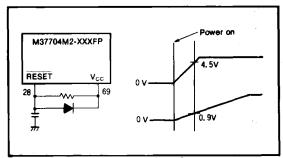


Fig. 61 Example of a reset circuit (perform careful evaluation at the system design level before using)

Γ	Α	ddress				Address	
(1)	Port P0 data directional register	(04 ₁₆)····	0016	(29)	Processor mode register	(5E ₁₆)····	0018
(2)	Port P1 data directional register	(05,6)	0016	(30)	Watchdog timer	(60 ₁₈)····	FFF ₁₆
(3)	Port P2 data directional register	(0816)	0016	(31)	Watchdog timer frequency selection flag	(61 ₁₆)····	0
(4)	Port P3 data directional register	(09 ₁₆)		(32)	Waveform output mode register	(62 ₁₆)····	0016
(5)	Port P4 data directional register	(0C16)	0016	(33)	A-D conversion interrupt control register	(70 ₁₆)····	$\bigvee \bigvee \bigvee \bigcirc \bigcirc \bigcirc \bigcirc \bigcirc \bigcirc \bigcirc$
(6)	Port P5 data directional register	(0D ₁₆)····	0016	(34)	UART 0 transmission interrupt control register	(71 ₁₆)····	
(7)	Port P6 data directional register	(1016)	00 ₁₆	(35)	UART 0 receive interrupt control register	(72 ₁₈)···	XXX 0 0 0 0
(8)	Port P7 data directional register	(11 ₁₆)	0016	(36)	UART 1 transmission interrupt control register	(73 ₁₆)····	
(9)	Port P8 data directional register	(14 ₁₆)	0016	(37)	UART 1 receive interrupt control register	(74 ₁₆)····	
(10)	A-D control register	(1E ₁₆)	0 0 0 0 0 ? ? ?	(38)	Timer A0 Interrupt control register	(75 ₁₆)····	
(11)	A-D sweep pin selection register	(1F ₁₆)	XXXXX11	(39)	Timer A1 interrupt control register	(76 ₁₆)····	$ \bigcirc \bigcirc$
(12)	UART 0 Transmit/Receive mode register	(30 ₁₆)···	0016	(40)	Timer A2 interrupt control register	(77 ₁₆)···	
(13)	UART 1 Transmit/Receive mode register	(38 ₁₆)	0016	(41)	Timer A3 interrupt control register	(78 ₁₆)···	
(14)	UART 0 Transmit/Receive control register 0	(34 ₁₆)	1000	(42)	Timer A4 interrupt control register	(79 ₁₈)···	
(15)	UART 1 Transmit/Receive control register 0	(3C ₁₆)	1000	(43)	Timer B0 interrupt control register	(7A ₁₆)	$\bigvee\!$
(16)	UART 0 Transmit/Receive control register 1	(35,6)	0 0 0 0 0 0 1 0	(44)	Timer B1 interrupt control register	(7B ₁₆)····	
(17)	UART 1 Transmit/Receive control register 1	(3D ₁₆)	0 0 0 0 0 1 0	(45)	Timer B2 interrupt control register	(7C ₁₆)····	$\times \times \times \circ \circ \circ \circ$
(18)	Count start flag	(40 ₁₆)	0016	(46)	INT 0 interrupt control register	(7D ₁₆)	00000
(19)	One-shot start flag	(42 ₁₆)····	0 0 0 0 0	(47)	INT 1 interrupt control register	(7E ₁₆)	000000
(20)	Up-down flag	(44 ₁₆)···	00 ₁₆	(48)	INT 2 interrupt control register	(7F ₁₆)	$\bigcirc \bigcirc $
(21)	Timer A0 mode register	(56 ₁₆)···	0018	(49)	Processor status register PS	0 0 0	? ? 0 0 0 1 ? ?
(22)	Timer A1 mode register	(57 ₁₆)···	0018	(50)	Program bank register PG		0016
(23)	Timer A2 mode register	(58 ₁₆)	0018	(51)	Program counter PC _H		Content of FFFF ₁₆
(24)	Timer A3 mode register	(59 ₁₆)···	0016	(52)	Program counter PCL		Content of FFFE ₁₆
(25)	Timer A4 mode register	(5A ₁₆)	0016	(53)	Direct page register DPR		000018
(26)	Timer B0 mode register	(5B ₁₆)	0016	(54)	Data bank register DT		0016
(21)	Timer B1 mode register	(5C ₁₆)	0 0 1 0 0 0 0]	ontents of other registers and RAI	M are not init	Halizad and should be in-
(28)	Timer B2 mode register	(5D ₁₆)···	0 0 1 0 0 0 0		alized by software.	** 015 HVI IIII	HONEOU SHOULD DO III-

Fig. 60 Microcomputer Internal status during reset

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INPUT/OUTPUT PINS

Ports P8 to P0 all have a data direction register and each bit can be programmed for input or output. A pin becomes an output pin when the corresponding data direction register is set and an input pin when it is cleared.

When pin programmed for output, the data is written to the port latch and it is output to the output pin. When a pin is programmed for output, the contents of the port latch is read instead of the value of the pin. Therefore, a previously output value can be read correctly even when the output "L" voltage is raised due to reasons such as directly driving an LED.

A pin programmed for input is floating and the value input to the pin can be read. When a pin is programmed for input, the data is written only in the port latch and the pin stays floating.

If an input/output pin is not used as an output port, clear the bit of the corresponding data direction register so that the pin become input mode.

Figure 62 shows a block diagram of ports P8 to P0 in single-chip mode and the $\overline{\bf E}$ pin output.

In memory expansion mode, microprocessor mode, and evaluation chip mode, ports P4 to P0 are also used as address, data, and control signal pins.

Refer to the section on processor modes for more details.

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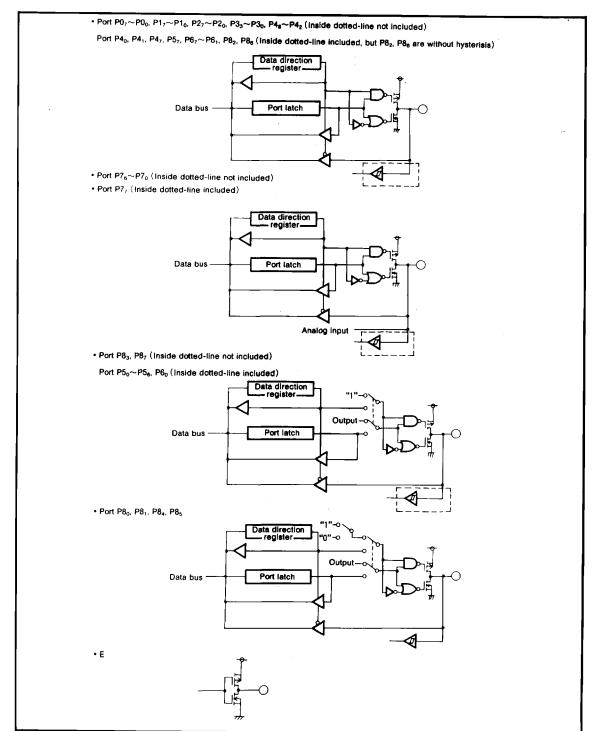


Fig. 62 Block diagram for ports P8 to P0 in single-chip mode and the E pin output

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PROCESSOR MODE

The bits 0 and 1 of processor mode register as shown in Figure 63 are used to select any mode of single-chip mode, memory expansion mode, microprocessor mode, and evaluation chip mode.

Ports P3 to P0 and a part of port P4 are used as address, data, and control signal I/O pins except in single-chip mode.

Figure 64 shows the functions of ports P4 to P0 in each mode.

The external memory area changes when the mode changes.

Figure 65 shows the memory map for each mode.

Refer to Figure 1 for the memory map of the single-chip mode. The external memory area can be accessed except in single-chip mode. The accessing of the external memory is affected by the BYTE pin and the bit 2 (wait bit) of processor mode register. These will be described next.

•BYTE pin

When accessing the external memory, the level of the BYTE pin is used to determine whether to use the data bus as 8-bit width or 16-bit width.

The data bus width is 8 bits when the level of the BYTE pin is "H" and port P2 becomes the data I/O pin.

The data bus width is 16 bits when the level of the BYTE pin is "L" and ports P1 and P2 become the data I/O pins.

When accessing the internal memory, the data bus width is always 16 bits regardless of the BYTE pin level.

An exclusive mode in the evaluation chip mode allows the BYTE pin level to be set to $2\cdot V_{CC}$. In this case, the operation is slightly different from the above. This is described in the evaluation chip mode section.

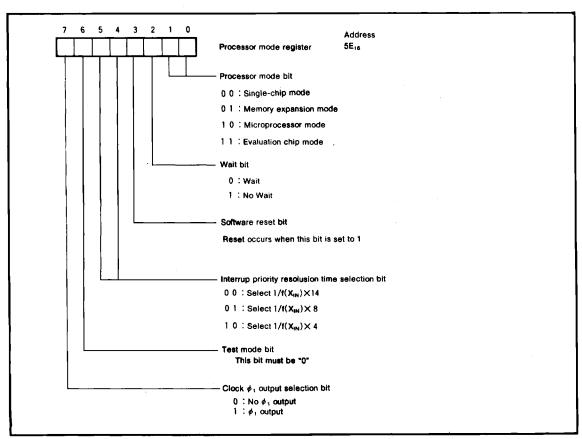


Fig. 63 Processor mode register bit configulation

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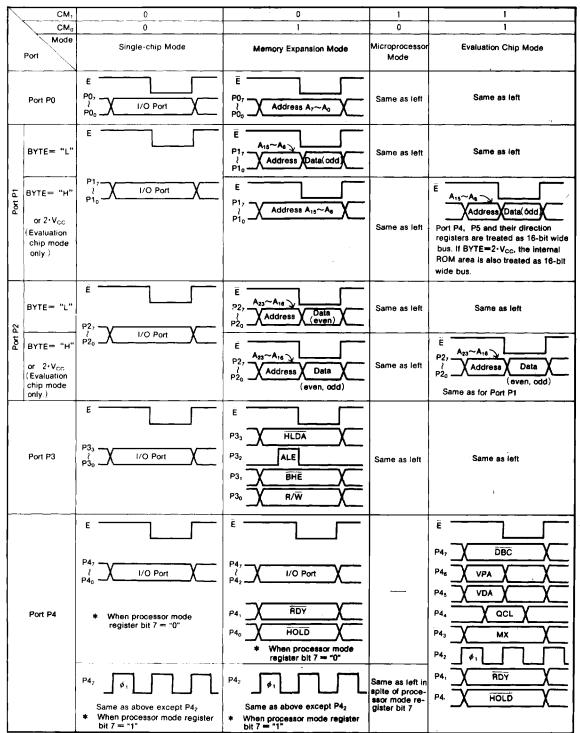


Fig. 64 Processor mode and ports P4 to P0 functions

M37704M2-XXXFP,M37704M2AXXXFP M37704S1FP,M37704S1AFP

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Walt bit

As shown in Figure 66, when the external memory area is accessed with the processor mode register bit 2 (wait bit) cleared to "0", the access time becomes twice the access time than the wait bit is "1" (no wait). The wait bit is cleared during reset.

The accessing of internal memory area is performed in no wait mode regardless of the wait bit.

The processor modes are described below.

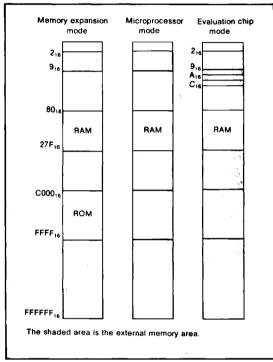


Fig. 85 External memory area for each processor

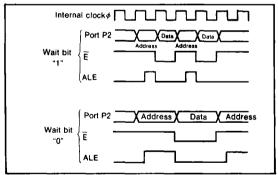


Fig. 66 Relationship between walt bit and access time

(1) Single-chip mode (00)

single-chip mode is entered by connecting the CNV_{SS} pin to V_{SS} and starting from reset. Ports P4 to P0 all function as normal I/O ports. Port P4₂ can be the ϕ_1 output pin divided the clock to X_{IN} pin by 2 by setting bit 7 of processor mode register to "1"

(2) Memory expansion mode [01]

Memory expansion mode is entered by setting the processor mode bits to "01" after connecting the CNV $_{\rm SS}$ pin to V $_{\rm SS}$ and starting from reset.

Port P0 becomes an address output pin and loses its I/O port function.

Port P1 has two functions depending on the level of the BYTE pin.

When the BYTE pin level is "L", port P1 functions as an address output pin while \overline{E} is "H" and as an odd address data I/O pin while \overline{E} is "L". However, if an internal memory is read, external data is ignored while \overline{E} is "L". In this case the I/O port function is lost.

When the BYTE pin level "H", port P1 functions as an address output pin and loses its I/O port function.

Port P2 has two functions depending on the level of the BYTE pin.

When the BYTE pin level is "L", port P2 functions as an address output pin while \overline{E} is "H" and as an even address data I/O pin while \overline{E} is "L". However, if an internal memory is read, external data is ignored while \overline{E} is "L".

When the BYTE pin level is "H", port P2 functions as an address output pin while \overline{E} is "H" and as an even and odd address data I/O pin while \overline{E} is "L". However, if an internal memory is read, external data is ignored while \overline{E} is "L". In this case the I/O port function is lost.

Ports P3₀, P3₁, P3₂, and P3₃ become R/ \overline{W} , \overline{BHE} , ALE, and \overline{HLDA} output pin respectively and lose their I/O port functions.

 R/\overline{W} is a read/write signal which indicates a read when it is "H" and a write when it is "L".

BHE is a byte high enable signal which indicates that an odd address is accessed when it is "L".

Therefore, two bytes at even and odd addresses are accessed simultaneously if address A_0 is "L" and \overline{BHE} is "L".

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ALE is an address latch enable signal used to latch the address signal from a multiplexed signal of address and data. The latch is transparent while ALE is "H" to let the address signal pass through and held while ALE is "L".

HLDA is a hold acknowledge signal and is used to notify externally when the microcomputer receives HOLD input and enters into hold state.

Ports P4₀ and P4₁ become HOLD and RDY input pin respectively and lose their output pin function, but the input pin function remains.

 $\overline{\text{HOLD}}$ is a hold request signal. It is an input signal used to put the microcomputer in hold state. Ports P0, P1, P2, P3₀, and P3₁ are floating while the microcomputer stays in hold state.

 $\overline{\text{RDY}}$ is a ready signal. If this signal goes "L", the **Internal** clock ϕ stops at "L". When ϕ_1 output from port $P4_2$ is selected by setting bit 7 of processor mode register to "1", ϕ_1 output keeps on. $\overline{\text{RDY}}$ is used when slow external memory is attached.

(3) Microprocessor mode [10]

Microprocessor mode is entered by connecting the CNV_{SS} pin to V_{CC} and starting from reset. It can also be entered by programming the processor mode bits to "10" after connecting the CNV_{SS} pin to V_{SS} and starting from reset. This mode is similar to memory expansion mode except that internal ROM is disabled and an external memory is required, and ϕ_1 from port $P4_2$ is always output in spite of bit 7 of processor mode register.

(4) Evaluation chip mode (11)

Evaluation chip mode is entered by applying voltage twice the $V_{\rm CC}$ voltage to the CNV $_{\rm SS}$ pin. This mode is normally used for evaluation tools.

The functions of ports P0 and P3 are the same as in memory expansion mode.

Port P1 functions as an address output pin while \overline{E} is "H" and as data I/O pin of odd addresses while \overline{E} is "L" regardless of the BYTE pin level. However, if an Internal memory is read, external data is ignored while \overline{E} is "L".

Port P2 function as an address output pin while \overline{E} is "H" and as data I/O pin of even addresses while \overline{E} is "L" when the BYTE pin level is "L". However, if an internal memory is read, external data is ignored while \overline{E} is "L".

When the BYTE pin level is "H" or $2 \cdot V_{CC}$, port P2 functions as an address output pin while \widetilde{E} is "H" and as data I/O pin of even and odd addresses while \widetilde{E} is "L". However, if an internal memory is read, external data is ignored while \overline{E} is "L".

Port P4 and its data direction register which are located at address 0A₁₆ and 0C₁₆ are treated differently in evaluation chip mode. When these addresses are accessed, the data bus width is treated as 16 bits regardless of the BYTE pin level, and the access cycle is treated as internal memory regardless of the wait bit.

When a voltage twice the V_{CC} voltage is applied to the

BYTE pin, the addresses corresponding to the internal ROM area are also treated as 16-bit data bus.

The functions of ports $P4_0$ and $P4_1$ are the same as in memory expansion mode.

Ports P4₂ to P4₈ become ϕ_1 , MX, QCL, VDA, and VPA output pins respectively. Port P4₇ becomes the \overline{DBC} input pin. ϕ_1 from port P4₂ divided the clock to X_{IN} pin by 2 is always output in spite of bit 7 of processor mode register.

The MX signal normally contains the contents of flag m, but the contents of flag x is output if the CPU is using flag x.

QCL is the queue buffer clear signal. It becomes "H" when the instruction queue buffer is cleared, for example, when a lump instruction is executed.

VDA is the valid data address signal. It becomes "H" while the CPU is reading data from data buffer or writing data to data buffer. It also becomes "H" when the first byte of the instruction (operation code) is read from the instruction queue buffer.

VPA is the valid program address signal. It becomes "H" while the CPU is reading an instruction code from the instruction queue buffer.

DBC is the debug control signal and is used for debugging. Table 5 shows the relationship between the CNVss pin input levels and processor modes.

Table 5. Relationship between the CNV_{SS} pin input levels and processor modes

CNV ₈₈	Mode	Description
V _{ss} V _{cc}	Single-chip Memory expansion Microprocessor Evaluation chip	Single-chip mode upon start- ing after reset. Other modes can be selected by changing the processor mode bit by software.
V _{cc}	Microprocessor Evaluation chip	Microprocessor mode upon starting after reset. Evaluation chip mode can be selected by changing the processor mode bit by software.
2 · Voc	Evaluation chip	· Evaluation chip mode only.

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CLOCK GENERATING CIRCUIT

Figure 67 shows a block diagram of the clock generator.

When an STP instruction is executed, the internal clock ϕ stops oscillating at "L" level. At the same time, FFF₁₆ is written to watchdog timer and the watchdog timer input connection is forced to f₃₂. This connection is broken and connected to the input determined by the watchdog timer frequency selection flag when the most significant bit of the watchdog timer is cleared or reset.

Oscillation resumes when an interrupt is received, but the internal clock ϕ remains at "L" level until the most significant bit of the watchdog timer is cleared. This is to avoid the unstable interval at the start of oscillation when using a ceramic resonator.

When a WIT instruction is executed, the internal clock ϕ stops at "L" level, but the oscillator does not stop. The clock is restarted when an interrupt is received. Instructions can be executed immediately because the oscillator is not stopped.

The stop or wait state is released when an interrupt is received or when reset is issued. Therefore, interrupts must be enabled before executing a STP or WIT instruction.

Figure 68 shows a circuit example using a ceramic (or quartz crystal) resonator. Use the manufacturer's recommended values for constants such as capacitance which differ for each resonator. Figure 69 shows an example of using an external clock signal.

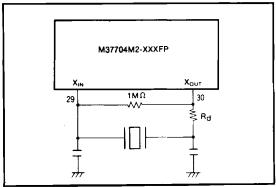


Fig. 68 Circuit using a ceramic resonator

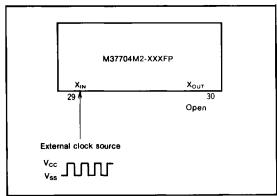


Fig. 69 External clock input circuit

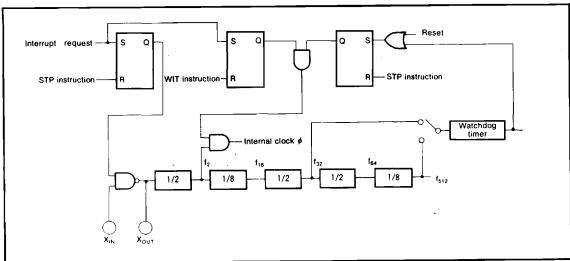


Fig. 67 Block diagram of a clock generator



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ADDRESSING MODES

The M37704M2-XXXFP has 28 powerful addressing modes. Refer to the Series MELPS 7700 addressing mode description for the details of each addressing mode.

MACHINE INSTRUCTION LIST

The M37704M2-XXXFP has 103 machine instructions. Refer to the Series MELPS 7700 machine instruction list for details.

DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.

- (1) M37704M2-XXXFP mask ROM order confirmation form
- (2) Mark specification form for 80P6N
- (3) ROM data (EPROM 3 sets)

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		−0.3~7	V
AVcc	Analog supply voltage		−0.3~7	V
V _i	Input voltage RESET, CNV _{SS} , BYTE		-0.3~12	V
V _i	Input voltage P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ , P3 ₀ ~P3 ₃ , P4 ₀ ~P4 ₇ , P5 ₀ ~P5 ₇ , P6 ₀ ~P6 ₇ , P7 ₀ ~P7 ₇ , P8 ₀ ~P8 ₇ , V _{REF} , X _{IN}		-0.3~V _{cc} +0.3	v
V _o	Output voltage P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ , P3 ₀ ~P3 ₃ , P4 ₀ ~P4 ₇ , P5 ₀ ~P5 ₇ , P6 ₀ ~P6 ₇ , P7 ₀ ~P7 ₇ , P8 ₀ ~P8 ₇ , X ₀₁₇ , Ē		-0.3~V _{cc} +0.3	v
Pd	Power dissipation	Ta=25°C	300	mW
Topr	Operating temperature		-10~70	ď
Tstg	Storage temperature		−40~125	°C

RECOMMENDED OPERATING CONDITIONS ($V_{cc}=5V\pm10\%$, $T_a=-10\sim70^{\circ}$ C, unless otherwise noted)

Symbol	Parameter		Unit		
Oyiniou.	- arameter	Min.	Тур.	Max.	O.III
V _{cc}	Supply voltage	4.5	5.0	5.5	٧
AVcc	Analog supply voltage		V _{CC}		٧
Vss	Supply voltage		0		٧
AV _{SS}	Analog supply voltage		0		٧
V _{IH}	High-level input voltage P0 ₀ ~P0 ₇ , P3 ₀ ~P3 ₃ , P4 ₀ ~P4 ₇ , P5 ₀ ~P5 ₇ , P6 ₀ ~P6 ₇ , P7 ₀ ~P7 ₇ , P8 ₀ ~P8 ₇ , X _{IN} , RESET, CNV _{SS} , BYTE	0.8V _{CC}		V _{cc}	v
VIH	High-level input voltage P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ (in single-chip mode)	0.8V _{CC}		Vcc	V
ViH	High-level input voltage P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ (in memory expansion mode and microprocessor mode)	0.5 v cc		Vec	v
ViL	Low-level input voltage P0 ₀ ~P0 ₇ , P3 ₀ ~P3 ₃ , P4 ₀ ~P4 ₇ , P5 ₀ ~P5 ₇ , P6 ₀ ~P6 ₇ , P7 ₀ ~P7 ₇ , P8 ₀ ~P8 ₇ , X _{IN} , RESET, CNV _{SS} , BYTE	0		0. 2V _{CC}	٧
V _{IL}	Low-level input voltage P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ (in single-chip mode)	0		0. 2V _{CC}	٧
VIL	Low-level input voltage P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ (in memory expansion mode and microprocessor mode)	0		0.16V _{cc}	v
lон(реак)	High-level peak output current P0 ₀ ~P0, P1 ₀ ~P1, P2 ₀ ~P2, P3 ₀ ~P3 ₃ , P4 ₀ ~P4, P5 ₀ ~P5, P6 ₀ ~P6, P7 ₀ ~P7, P8 ₀ ~P8,			-10	mA
l _{он(avg)}	High-level average output current P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ , P3 ₀ ~P3 ₃ , P4 ₀ ~P4 ₇ , P5 ₀ ~P5 ₇ , P6 ₀ ~P6 ₇ , P7 ₀ ~P7 ₇ , P8 ₀ ~P6 ₇			-5	mA
lou(peak)	Low-level peak output current P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ , P3 ₀ ~P3 ₃ , P4 ₀ ~P4 ₇ , P5 ₆ , P5 ₇ , P6 ₀ ~P6 ₇ , P7 ₀ ~P7 ₇ , P8 ₀ ~P8 ₇			10	mA
lou(peak)	Low-level peak output current P5 ₀ ~P5 ₅			20	mA
lo _L (avg)	Low-level average output current P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ , P3 ₀ ~P3 ₉ , P4 ₀ ~P4 ₇ , P5 ₈ , P5 ₇ , P6 ₀ ~P6 ₇ , P7 ₀ ~P7 ₇ , P8 ₀ ~P8 ₇			5	mA
loL(avg)	Low-level average output current P5 ₆ ~P5 ₅			15	mA
f(X _{IN})	External clock frequency input M37704M2-XXXFP, M37704S1FP M37704M2AXXXFP, M37704S1AFP			8	мна

Note 1. Average output current is the average value of a 100ms interval.

2. The sum of lou(peak) for ports P0, P1, P2, P3, and P8 must be 80mA or less, the sum of lou(peak) for ports P0, P1, P2, P3, and P8 must be 80mA or less, the sum of lou(peak) for ports P4, P5, P6, and P7 must be 110mA or less, and the sum of loH(peak) for ports P4, P5, P6, and P7 must be 80mA or less.



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M37704M2-XXXFP

ELECTRICAL CHARACTERISTICS (V_{CC}=5V, V_{SS}=0V, T₈=25°C, f(X_{IN})=8MHz, unless otherwise noted)

Symbol	Parameter	Test co	nditions	Limits			Unit
Эуппон	Fai alliete:	100.00	il dividual	Min.	Тур.	Max.	Unit
V _{OH}	High-level output voltage P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ , P3 ₀ , P3 ₁ , P3 ₃ , P4 ₀ ~P4 ₇ , P5 ₀ ~P5 ₇ , P6 ₀ ~P6 ₇ , P7 ₀ ~P7 ₇ , P8 ₀ ~P8 ₇	I _{OH} =-10mA		3			٧
V _{он}	High-level output voltage P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ , P3 ₀ , P3 ₁ , P3 ₃	I _{OH} =-400μA		.4.7			>
VoH	High-level output voltage P3 ₂	I _{OH} = -10mA		3. 1			\ \
▼ ОН	Trigit-level output voitage 7 52	I _{OH} =-400μA		4.8			
V _{OH}	High-level output voltage É	I _{OH} =-10mA		3. 4		<u> </u>	v
ч он	Trigitator output tomage 2	I _{OH} =-400μA		4. 8			
VoL	Low-level output voltage P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ , P3 ₀ , P3 ₁ , P3 ₃ , P4 ₀ ~P4 ₇ , P5 ₆ , P5 ₇ , P6 ₀ ~P6 ₇ , P7 ₀ ~P7 ₇ , P8 ₀ ~P8 ₇	I _{OL} =10mA				2	v
VoL	Low-level output voltage P5 ₀ ~P5 ₅	I _{OL} =20mA				2	٧
VoL	Low-level output voltage P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ , P3 ₀ , P3 ₁ , P3 ₃	I _{OL} =2mA				0. 45	٧
Vol	Low-level output voltage P3 ₂	I _{OL} =10mA I _{OL} =2mA				1.9	v
VOL	Low-level output voltage F32					0.43	L.
Vol	Low-level output voltage E	IoL=10mA				1.6	v
	Eow love output voltage E	I _{OL} =2mA				0.4	
V ₇₊ V ₇₋	Hysteresis HOLD, RDY, TA0 _{IN} ~TA4 _{IN} , TB0 _{IN} ~TB2 _{IN} , INT ₀ ~INT ₂ , AD _{TRG} , CTS ₀ , CTS ₁ , CLK ₀ , CLK ₁			0. 4		1	v
V _{T+} -V _{T-}	Hysteresis RESET			0.2	1	0.5	٧
V _{T+} -V _{T-}	Hysteresis X _{IN}			0.1		0. 3	٧
l _{iH}	High-level input current P00~P07, P10~P17, P20~P27, P30~P33, P40~P47, P50~P57, P60~P67, P70~P77, P80~P87, X _{IN} , RESET, CNV _{SS} , BYTE	V ₁ =5V				5	μΑ
I _{IL}	Low-level input current P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ , P3 ₀ ~P3 ₃ , P4 ₀ ~P4 ₇ , P5 ₀ ~P5 ₇ , P6 ₀ ~P6 ₇ , P7 ₀ ~P7 ₇ , P8 ₀ ~P8 ₇ , X _{IN, RESET, CNV_{ss.} BYTE}	V ₁ =0V				-5	μΑ
VRAM	RAM hold voltage	When clock is stoppe	d.	2			V
,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,		In single-chip mode	f(X _{IN})=8MHz, square waveform		6	12	mA
Icc	Power supply current	output only pin is open and other pins	Ta=25°C when clock is stopped.			1	م یر
		are V _{SS} during reset.	Ta=70°C when clock is stopped.			10	

$\textbf{A-D} \quad \textbf{CONVERTER} \quad \textbf{CHARACTERISTICS} \; (v_{cc} = 5v, \, v_{ss} = 0v, \, T_{g} = 25 °C, \, f(x_{iN}) = 8 \text{MHz, unless otherwise noted})$

Symbol	Parameter	Test conditions	Ĺ	Limits		
		1 det conditions	Min.	Тур.	Max.	Unit
_	Resolution	V _{REF} =V _{CC}			8	Bits
	Absolute accuracy	V _{REF} =V _{CC}		_	±3	LSB
RLADDER	Ladder resistance	V _{REF} =V _{CC}	2		10	kΩ
tconv	Conversion time		28. 5		1	μз
VREF	Reference voltage		2		Vcc	V
VIA	Analog input voltage		0		VREF	v

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TIMING REQUIREMENTS (v_{cc} =5 $v\pm10\%$, v_{ss} =0v, T_a =25C, $f(x_{in})$ =8MHz, unless otherwise noted)

External clock input

		Test conditions		Unit		
Symbol	Parameter		Min.	Тур.	Max.	Unit
l _c	External clock input cycle time		125			ns
t _{W(H)}	External clock input high-level pulse width		50			ns
t _{W(L)}	External clock input low-level pulse width	·	50			ns
tr	External clock rise time				20	ns
tr	External clock fall time				20	กร

Single-chip mode

Cb-al	Parameter	Test conditions	1		Unit	
Symbol	Parameter	lest conditions	Min.	Тур	Max.	Unit
tsu(POD-E)	Port P0 input setup time		200			ns
tsu(PID-E)	Port P1 input setup time		200			ns
t _{SU(P2D-E)}	Port P2 input setup time		200			ns
tsu(P3D-E)	Port P3 input setup time		200			ns
tsu(P4D-E)	Port P4 input setup time		200			ns
tsu(P5D-E)	Port P5 input setup time		200			ns
tsu(P6D-E)	Port P6 input setup time		200			ns
tsu(P7D-E)	Port P7 Input setup time		200			ns
tsu(PaD-E)	Port P8 input setup time		200			ns
th(E-POD)	Port P0 input hold time		0			ns
th(E-PID)	Port P1 input hold time		0			ns
th(E-P2D)	Port P2 input hold time		0			ns
th(E-P3D)	Port P3 input hold time		0			ns
th(E-P4D)	Port P4 input hold time		0			ns
th(E-P5D)	Port P5 input hold time		0		T	กร
th(E-P6D)	Port P6 input hold time		0	Ī		ns
th(E-P7D)	Port P7 input hold time		0			ns
th(E-PSD)	Port P8 input hold time		0		Ī	ns

Memory expansion mode and microprocessor mode

		Test conditions		Unit		
Symbol	Parameter	lest conditions	Min.	Тур.	Max.	Onit
tsu(P1D-E)	Port P1 input setup time		60			ns
tsu(P2D-E)	Port P2 input setup time		60			ns
tsu(RDY-#1)	RDY Input setup time		70			กร
th(E-P1D)	Port P1 Input hold time		0			ns
th(E-P2D)	Port P2 Input hold time		0			ns
th(#1-RDY)	RDY input hold time		0			ns

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Timer A input (Count input in event counter mode)

	Parameter	Test conditions		Unit		
Symbol	Parameter	i est conditions	Min. Typ.	Max.	UNK	
t _{C(TA)}	TAI _{IN} input cycle time		250			ns
tw(TAH)	TAi _{IN} input high-level pulse width		125			ne
tw(TAL)	TAi _{IN} input low-level pulse width		125			ns.

Timer A input (Gating input in timer mode)

Combal	Parameter	Test conditions	Limits			Unit
Symbol			Min.	Typ.	Max.	Othic
t _{C(TA)}	TAI _{IN} Input cycle time		1000			ris
tw(TAH)	TAI _{IN} Input high-level pulse width		500			ns
tw(TAL)	TAi _{IN} input low-level pulse width		500			ne

Timer A input (External trigger input in one-shot pulse mode)

Combal	Parameter	Test conditions		1 to 14		
Symbol	Parameter		Min.	Тур.	Max.	Unit
t _{C(TA)}	TAI _{IN} input cycle time		500			ns .
t _{W(TAH)}	TAi _{IN} input high-level pulse width		250			ns
tw(TAL)	TAi _{IN} input low-level pulse width		250			ns.

Timer A input (External trigger input in pulse width modulation mode)

Completed.	Symbol Parameter tw(TAH) TAin input high-level pulse width	Test conditions		Unit		
Symbol	Parameter	lest conditions	Min.	Тур.	Max.	Unit
tw(TAH)			250			ns
tw(TAL)	TAi _{IN} input low-level pulse width		250			ns

Timer A input (Up-down input in event counter mode)

Symbol	Parameter	Test conditions		Limits		
	Parameter	I BR COnditions	Min.	Тур.	Max.	Unit
t _{C(UP)}	TAI _{OUT} input cycle time		5000			ns
tw(uph)	TAiout input high-level pulse width		2500			ns
tw(upL)	TAiout Input low-level pulse width		2500			กร
tsu(UP-TIN)	TAi _{OUT} input setup time		1000			ns
th(Tautie)	TAI _{OUT} input hold time		1000			ns.



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Timer B input (Count input in event counter mode)

Symbol	Parameter	Tank dist		11-11		
Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t _{C(TB)}	TBi _{IN} Input cycle time (one edge count)		250			ns
t _W (твн)	TBI _{IN} input high-level pulse width (one edge count)		125			ns
tw(TBL)	TBI _{IN} input low-level pulse width (one edge count)		125			ns
t _{C(TB)}	TBi _{IN} input cycle time (both edges count)		500			ns
t _{W(TBH)}	TBi _{IN} input high-level pulse width (both edges count)		250			ns
tw(TBL)	TBI _{IN} input low-level pulse width (both edges count)		250			ns

Timer B input (Pulse period measurement mode)

O.m.b.al	B	Test conditions		Unit		
Symbol	Parameter	lest conditions	Min.	Тур.	Max.	Unit
t _{C(TB)}	TBi _{IN} input cycle time		1000			N8
tw(TBH)	TBI _{IN} input high-level pulse width		500			ns
tw(TBL)	TBi _{IN} input low-level pulse width		500			ns

Timer B input (Pulse width measurement mode)

Oumb at	Parameter	Test conditions	Limits			Unit
Symbol	rarameter	1981 CONCILIONS	Min.	Тур.	Max.	Unit
t _{C(TB)}	TBI _{IN} input cycle time		1000			N8
t _{W(TBH)}	TBi _{IN} input high-level pulse width		500			ns
t _{W(TBL)}	TBi _{IN} input low-level pulse width		500			ns

A-D trigger input

Symbol	Da	Test conditions		Limits		Unit
Symbol	Parameter	Fest conditions	Min.	Тур.	Max.	Unit
t _{C(AD)}	AD _{TRG} Input cycle time (minimum allowable trigger)		2000			ns
tw(ADL)	AD _{TRG} input low-level pulse width		250			ns :

Serial I/O

0	Parameter	F4 dial	Limits			
Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
to(ok)	CLKi input cycle time		500			ns
tw(ckH)	CLKi input high-level pulse width		250			ns
tw(CKL)	CLKI input low-level pulse width		250			ns
td(c-a)	TxDi output delay time				150	ns
th(c-a)	TxDi hold time		30			ns
tsu(D-C)	RxDi Input setup time		60			ns
th(c-p)	RxDi Input hold time		90			ns

External interrupt INTi input

Symbol	Parameter	Test conditions		Limits		Unit
Symbol	rarameter	rest conditions	Min.	Тур.	Max.	Unit
tw(INH)	INTi input high-level pulse width		250			ns
t _{W(INL)}	INTI input low-level pulse width		250			ns

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SWITCHING CHARACTERISTICS ($V_{cc}=5V\pm10\%$, $V_{ss}=0V$, $T_a=25\%$, $f(X_{in})=8MHz$, unless otherwise noted) Single-chip mode

Symbol	Parameter				1 1-1A	
Symbol	Parameter	Test conditions	Min.	Тур.	Мах.	Unit
td(E=P0Q)	Port P0 data output delay time				200	ns
	Port P1 data output delay time				200	ns
td(E_P2Q)	Port P2 data output delay time	1			200	ns
td(E-P3Q)	Port P3 data output delay time	· ·			200	ns
td(E-P4Q)	Port P4 data output delay time	Figure 70			200	ns
td(E_P50)	Port P5 data output delay time				200	ns
td(EP6Q)	Port P6 data output delay time				200	ns
td(EP7Q)	Port P7 data output delay time		[200	ns
td(E-P8Q)	Port P8 data output delay time				200	กร

Memory expansion mode and microprocessor mode (when wait bit = "1")

Symbol	Parameter	Test conditions	Limits			Unit
Symbol	rarameter	Test conditions	Min.	Тур.	Max.	Unit
td(POA-E)	Port P0 address output delay time		100			ns
td(E-P1Q)	Port P1 data output delay time (BYTE="L")]			120	ns
t _{PXZ(E-P1Z)}	Port P1 floating start delay time (BYTE="L")				5	ns
td(PIA-E)	Port P1 address output delay time		100			ns
td(E-P2Q)	Port P2 data output delay time				120	ns
tPXZ(E-P2Z)	Port P2 floating start delay time				5	ns
td(P2A-E)	Port P2 address output delay time		100			ns
td(E-HLDA)	HLDA output delay time	Figure 70			100	ns
td(ALE-E)	ALE output delay time		4			ns
tw(ALE)	ALE pulse width		100			ns
td(BHE-E)	BHE output delay time		100			ns
td(R/W-E)	R/W output delay time		100			ns
td(E-ø1)	ø₁ output delay time		0		30	ns
th(E-POA)	Port P0 address hold time	1	50			ns
th(ALE-PIA)	Port P1 address hold time (BYTE="L")		9			ns
th(E-P1Q)	Port P1 data hold time (BYTE="L")		50			กร
tpZX(E-P1Z)	Port P1 floating release delay time (BYTE="L")		50			ns
th(E-PIA)	Port P1 address hold time (BYTE="H")		50			ns
th(ALE-P2A)	Port P2 address hold time		9			ns
th(E_P2Q)	Port P2 data hold time		50			ns
t _{PZX(E-P2Z)}	Port P2 floating release delay time		50			ns
th(E-BHE)	BHE hold time		20		<u> </u>	ns
th(E-R/W)	R/W hold time		20			ns
t _{W(EL)}	E pulse width	1	220			na

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Memory expansion mode and microprocessor mode (when wait bit = "0", and external memory area is accessed)

Symbol	Parameter	Test conditions		Limits		Unit
Symbol	rarameter	1 est conditions	Min.	Тур.	Max.	Unit
td(POA-E)	Port P0 address output delay time		350			ns
td(E-P1Q)	Port P1 data output delay time (BYTE="L")				120	ns
t _{PXZ(E-P1Z)}	Port P1 floating start delay time (BYTE="L")				5	ns
td(PIA-E)	Port P1 address output delay time		350			ns
td(E-P2Q)	Port P2 data output delay time				120	ns
t _{PXZ} (E-P2Z)	Port P2 floating start delay time				5	ns
td(P2A-E)	Port P2 address output delay time	•	350			ns
td(E-HLDA)	HLDA output delay time				100	ns
td(ALE-E)	ALE output delay time		4		,	ns
tw(ALE)	ALE pulse width		350			ns
td(BHE-E)	BHE output delay time		350			ns
td(R/W-E)	R/W output delay time	Figure 70	350			n\$
t _{d(E-≠1)}	φ ₁ output delay time		. 0		30	ns
th(E-POA)	Port P0 address hold time		50			ns
th(ALE-PIA)	Port P1 address hold time (BYTE="L")		9			ns
th(E-P1Q)	Port P1 data hold time (BYTE="L")		50			ns
t _{PZX} (E-P1Z)	Port P1 floating release delay time (BYTE="L")		50			กร
th(E-PIA)	Port P1 address hold time (BYTE="H")		50			ns
th(ALE-P2A)	Port P2 address hold time		9			ns
th(E-P2Q)	Port P2 data hold time		50			ns
t _{PZX(E-P2Z)}	Port P2 floating release delay time		50			ns
th(E-BHE)	BHE hold time		20			ns
th(E-R/W)	R/W hold time		20			ns
tw(EL)	E pulse width		220			ns

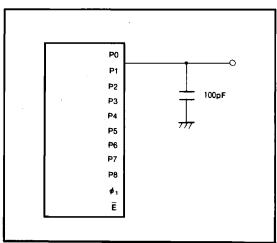


Fig. 70 Testing circuit for ports P0~P8, φ1

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M37704M2AXXXFP

$\textbf{ELECTRICAL} \quad \textbf{CHARACTERISTICS} \; (v_{cc} = 5 \text{V, } v_{ss} = 0 \text{V, } T_{\textbf{a}} = 25 \text{C, } f(X_{\textbf{N}}) = 16 \text{MHz, unless otherwise noted})$

Symbol	Parameter	Test co	nditions		Limits		Unit
				Min.	Тур.	Max.	
V _{OH}	High-level output voltage P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ , P3 ₀ , P3 ₁ , P3 ₃ , P4 ₀ ~P4 ₇ , P5 ₀ ~P5 ₇ , P6 ₀ ~P6 ₇ , P7 ₀ ~P7 ₇ , P8 ₀ ~P8 ₇	I _{OH} =-10mA	I _{OH} = −10mA				v
V _{OH}	High-level output voltage P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ , P3 ₀ , P3 ₁ , P3 ₃	I _{OH} =-400μA		4. 7			٧
V _{OH}	High-level output voltage P3₂	I _{OH} =-10mA I _{OH} =-400μA		3. 1 4. 8			v
	_	I _{OH} = −10mA		3. 4			-
V _{OH}	High-level output voltage E	I _{OH} =-400µA		4. 8			V
V _{OL}	Low-level output voltage P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ , P3 ₀ , P3 ₁ , P3 ₃ , P4 ₄ ~P4 ₇ , P5 ₆ , P5 ₇ , P6 ₀ ~P6 ₇ , P7 ₀ ~P7 ₇ , P8 ₀ ~P8 ₇	I _{OL} =10mA				2	>
VoL	Low-level output voltage P5 ₀ ~P5 ₆	I _{OL} =20mA				2	٧
VoL	Low-level output voltage P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ , P3 ₀ , P3 ₁ , P3 ₃	IoL=2mA				0, 45	v
V _{OL}	Low-level output voltage P3 ₂	I _{OL} =10mA				1.9	v
VOL	Low-level output voltage F32	I _{OL} =2mA				0. 43	
VoL	Low-level output voltage E	I _{OL} =10mA			<u></u>	1.6	v
•OL	Edwiger output voilage E	I _{OL} =2mA				0.4	
V _{T+} V _{T-}	Hysteresis HOLD, RDY, TA0 _{IN} ~TA4 _{IN} , TB0 _{IN} ~TB2 _{IN} , INT ₀ ~INT ₂ , AD _{TRG} , CTS ₀ , CTS ₁ , CLK ₀ , CLK ₁			0. 4		1	>
V _{T+} -V _T	Hysteresis RESET			0.2		0.5	>
V _{T+} -V _{T-}	Hysteresis X _{IN}			0. 1	_	0.3	
l _{lie}	High-level input current P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ , P3 ₀ ~P3 ₃ , P4 ₀ ~P4 ₇ , P5 ₀ ~P5 ₇ , P6 ₀ ~P6 ₇ , P7 ₀ ~P7 ₇ , P8 ₀ ~P8 ₇ , X _{IN} , RESET, CNV _{SS} , BYTE	V:=5V				5	μΑ
l _{IL}	Low-level input cufrent P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₉ ~P2 ₇ , P3 ₀ ~P3 ₃ , P4 ₀ ~P4 ₇ , P5 ₀ ~P5 ₇ , P6 ₀ ~P6 ₇ , P7 ₀ ~P7 ₇ , P8 ₀ ~P8 ₇ , X _{IN, RESET, CNV_{SS}, BYTE}	v ₁ -0v				-5	μА
VRAM	RAM hold voltage	When clock is stoppe	d.	2			٧
		In single-chip mode	f(X _{IN})=16MHz, square waveform		12	24	m/
lcc	Power supply current	output only pin is open and other pins	T _a =25°C when clock is stopped.			1	
		are V _{SB} during reset.	Ta=70°C when clock is stopped.			10	μА

A-D CONVERTER CHARACTERISTICS (V_{CC}=5V, V₈₈=0V, T₈=25°C, f(X_{IN})=16MHz, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits		
Symbol	Parameter	1 #St Conditions	Min.	Тур.	Max.	Unit
_	Resolution	V _{REF} =V _{CC}		1	8	Bits
	Absolute accuracy	V _{REF} =V _{CC}			±3	LSB
RLADDER	Ladder resistance	V _{REF} =V _{CC}	2		10	kΩ
tconv	Conversion time		14. 25			μ\$
VREF	Reference voltage		2		Vcc	V
VIA	Analog input voltage		0		VREF	V



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TIMING REQUIREMENTS (v_{cc} =5 $v\pm10\%$, v_{ss} =0v, τ_a =25 τ , $t(x_{in})$ =16MHz, unless otherwise noted)

External clock input

Symbol	December	Test conditions	Limits			Unit
	Parameter	lest conditions	Min.	Тур.	Max.	0,,,,
tc	External clock input cycle time		62			ns.
t _{W(H)}	External clock input high-level pulse width		25			ns
t _{w(L)}	External clock input low-level pulse width		25			ns
tr	External clock rise time				10	ns
tf	External clock fall time				10	ns

Single-chip mode

	Bernandor.	T4 dial	Limits			Unit
Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t _{SU(POD-E)}	Port P0 input setup time		100			ns
tsu(PID-E)	Port P1 input setup time		100			ns
t _{SU(P2D-E)}	Port P2 input setup time		100			ns
tsu(P3D-E)	Port P3 input setup time		100			ns
tsu(P4D-E)	Port P4 input setup time		100			ns
t _{SU(P5D-E)}	Port P5 input setup time		100]		ns
tsu(P6D-E)	Port P6 input setup time		100			ns
tsu(P7D-E)	Port P7 input setup time		100			ns
tsu(PBD-E)	Port P8 input setup time		100			ns
th(E-POD)	Port P0 input hold time		0			ns
th(E-P1D)	Port P1 input hold time		0			ns
th(E-P2D)	Port P2 input hold time		0			ns
th(E-P3D)	Port P3 input hold time		0			ns
th(E-P4D)	Port P4 input hold time		0			ns
th(E-P5D)	Port P5 input hold time		0			ns
th(E-P6D)	Port P6 input hold time		0	T		ns
th(E-P7D)	Port P7 input hold time		0			ns
th(E-P8D)	Port P8 input hold time		0			ns

Memory expansion mode and microprocessor mode

	Parameter	Took conditions		Unit		
Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
tsu(PID-E)	Port P1 input setup time		45			ns
tsu(P2D-E)	Port P2 input setup time		45	·		ns
tsu(RDY-#1)	RDY input setup time (when wait bit = "1")		60			ns
th(E-P1D)	Port P1 Input hold time		0			ns
th(E-P2D)	Port P2 input hold time		0			ns
th(#1-RDY)	RDY input hold time		0			ns

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Timer A input (Count input in event counter mode)

Ob.al	Parameter	Test conditions		Unit		
Symbol			Min.	Тур.	Max.	Onk
t _{C(TA)}	TAI _{IN} input cycle time		125			N8
tw(TAH)	TAin input high-level pulse width		62			ns
tw(TAL)	TAin input low-level pulse width		62			ns

Timer A Input (Gating Input in timer mode)

Symbol	Parameter	Test conditions	Limits			Unit
			Min,	Тур.	Max.) Omit
t _{C(TA)}	TAi _{IN} Input cycle time		500			ns .
tw(TAH)	TAi _{IN} input high-level pulse width		250			ns
tw(TAL)	TAi _{IN} input low-level pulse width		250			ns

Timer A input (External trigger input in one-shot pulse mode)

Sbal	Symbol Parameter	Test conditions	Limits			Unit
Symbol			Min.	Тур.	Max.	UNIL
t _{C(TA)}	TAi _{IN} input cycle time		250			ns .
tw(TAH)	TAi _{IN} input high-level pulse width		125			ns
tw(TAL)	TAi _{IN} input low-level pulse width		125			ns

Timer A Input (External trigger input in pulse width modulation mode)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Тур.	Max.) Unit
t _{W(TAH)}	TAi _{IN} input high-level pulse width		125			ns
tw(TAL)	TAi _{IN} input low-level pulse width		125			ns

Timer A input (Up-down input in event counter mode)

Symbol	Parameter	Test conditions		Unit		
	Parameter	i est conditions	Min.	Тур.	Max.	Unit
t _{C(UP)}	TAI _{OUT} input cycle time		2500			ns
tw(uph)	TAiout input high-level pulse width		1250			กร
tw(upL)	TAiout Input low-level pulse width		1250			ns
tsu(UP-TIN)	TAiout input setup time		500			ns
th(TIN-UP)	TAI _{OUT} input hold time		500			ns

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Timer B input (Count input in event counter mode)

Symbol	Parameter	Took oon distance		Unit		
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{C(TB)}	TBi _{IN} Input cycle time (one edge count)		125			ns
tw(TBH)	TBi _{IN} input high-level pulse width (one edge count)		62			ns
tw(TBL)	TBi _{IN} input low-level pulse width (one edge count)		62			ns
t _{C(TB)}	TBi _{IN} input cycle time (both edges count)		250			ns
t _{w(твн)}	TBI _{IN} input high-level pulse width (both edges count)		125			ns
tw(TBL)	TBi _{IN} input low-level pulse width (both edges count)		125			ns

Timer B input (Pulse period measurement mode)

Symbol	Parameter	Test conditions		Unit		
			Min.	Тур.	Max.	Unit
t _{C(TB)}	TBI _{IN} input cycle time		500			ns
t _{W(TBH)}	TBi _{IN} input high-level pulse width		250			ns
tw(TBL)	TBi _{IN} input low-level pulse width		250			ns

Timer B input (Pulse width measurement mode)

Symbol	Parameter	Test conditions	Limits			Unit
	Parameter	rest conditions	Min.	Тур.	Max.	Unik
t _{C(TB)}	TBi _{IN} Input cycle time		500			ns
t _{w(твн)}	TBi _{IN} Input high-level pulse width		250			ns
tw(TBL)	TBi _{IN} input low-level pulse width		250			ns

A-D trigger input

Symbol	Parameter	Test conditions		Limits		Limit
Symbol			Min.	Тур.	Max.	Unit
t _C (AD)	AD _{TRG} input cycle time (minimum allowable trigger)		1000			ns.
tw(ADL)	AD _{TRG} input low-level pulse width		125			^ ns

Serial I/O

Symbol	Parameter	Toot conditions	Limits /			14-15
		Test conditions	Min.	Тур.	Max.	Unit
t _{C(CK)}	CLKi Input cycle time		250			ns
tw(ckH)	CLKi input high-level pulse width		125			ns
tw(ckL)	CLKi input low-level pulse width		125			ns
td(c-a)	TxDi output delay time				90	ns
th(c-o)	TxDi hold time		30			ns
tsu(D-C)	RxDI input setup time	,	30			na
th(c-c)	RxDI input hold time		90			ns

External interrupt INTi input

0	Parameter	Test conditions		Limits		Unit
Symbol		rest conditions	Min.	Тур.	Max.	UNK
tw(INH)	INTi input high-level pulse width		250			ns
tw(INL)	INTi input low-level pulse width	·	250			ns

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SWITCHING CHARACTERISTICS ($v_{cc}=5v\pm10\%$, $v_{ss}=0v$, $\tau_a=25$ °C, $f(X_{IN})=16$ MHz, unless otherwise noted) Single-chip mode

Symbol		20 1	Limits			Unit
	Parameter	Test conditions	Min.	Тур.	Max.	JINI
td(E-POQ)	Port P0 data output delay time				100	ns
td(E-P10)	Port P1 data output delay time				100	ns
td(E-P2Q)	Port P2 data output delay time				100	ns
td(E-P3Q)	Port P3 data output delay time				100	ns
td(E-P4Q)	Port P4 data output delay time	Figure 70			100	ns
td(E-PSQ)	Port P5 data output delay time		1		100	ns
td(E-PeQ)	Port P6 data output delay time				100	ns
td(E-P7Q)	Port P7 data output delay time				100	NS
td(EP8Q)	Port P8 data output delay time				100	กธ

Memory expansion mode and microprocessor mode (when wait bit = "1")

Symbol	Parameter	Test conditions	Limits			Unit
		lest conditions	Min.	Typ.	Max.	Unit
td(POA-E)	Port P0 address output delay time		30			ns
td(E-P1Q)	Port P1 data output delay time (BYTE="L")				80	ns
t _{PXZ} (E-P1Z)	Port P1 floating start delay time (BYTE="L")				5	ns
td(PIA-E)	Port P1 address output delay time		30			ns
td(E-P2Q)	Port P2 data output delay time				80	ris
t _{PXZ} (E-P2Z)	Port P2 floating start delay time				5	ns
td(P2A-E)	Port P2 address output delay time	.]	30			ns
td(E-HLDA)	HLDA output delay time				50	ns
td(ALE-E)	ALE output delay time		4			ns
t _{W(ALE)}	ALE pulse width		40			ns
td(BHE-E)	BHE output delay time		30			ns
td(R/W-E)	R/W output delay time	Figure 70	30			ns
td(E-#1)	φ ₁ output delay time	Figure 70	0		20	ns
th(E-POA)	Port P0 address hold time		25			ns
th(ALE-PIA)	Port P1 address hold time (BYTE="L")		9			ns
th(E-P10)	Port P1 data hold time (BYTE="L")		25			ns
t _{PZX(E-P1Z)}	Port P1 floating release delay time (BYTE="L")		25			ns
th(E-PIA)	Port P1 address hold time (SYTE="H")		25			na
th(ALE-P2A)	Port P2 address hold time		9			ns
th(E-P2Q)	Port P2 data hold time		25			ns
t _{PZX} (E-P2Z)	Port P2 floating release delay time		25			ns
th(E-BHE)	BHE hold time		20			ns
th(E-R/W)	R/W hold time		20			กร
tw(EL)	E pulse width		95			ns

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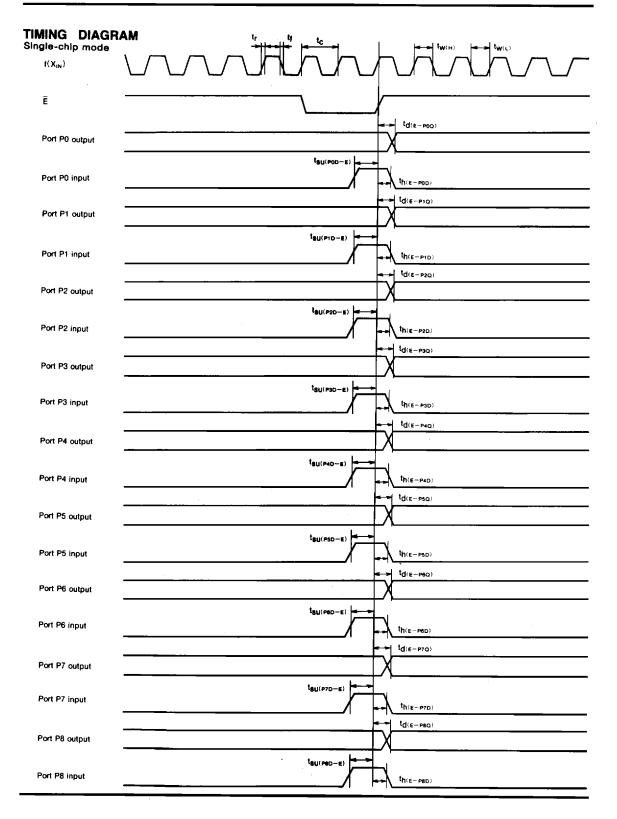
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Memory expansion mode and microprocessor mode (when wait bit = "0", and external memory area is accessed)

Symbol Parameter	Perameter	Test conditions	Limits			Unit
	rest conditions	Min.	Typ.	Max.	Unit	
td(POA-E)	Port P0 address output delay time		155			กร
td(E-P1Q)	Port P1 data output delay time (BYTE=="L")				80	ns
t _{PXZ(E-P1Z)}	Port P1 floating start delay time (BYTE="L")				5	ns
td(PIA-E)	Port P1 address output delay time		155			ns
td(E-P2Q)	Port P2 data output delay time				80	ns
t _{PXZ(E-P2Z)}	Port P2 floating start delay time				5	ns
td(P2A-E)	Port P2 address output delay time		155			ns
td(E-HLDA)	HLDA output delay time				50	ns
td(ALE-E)	ALE output delay time		4			ns
tw(ALE)	ALE pulse width		165			ns
td(BHE-E)	BHE output delay time		155			ns
td(R/W-E)	R/W output delay time	515,000 70	155			ns
td(E-ø1)	∮₁ output delay time	Figure 70	0		20	ns
th(E~PGA)	Port P0 address hold time		25			ns
th(ALE-PIA)	Port P1 address hold time (BYTE="L")		9			ns
th(E-P1Q)	Port P1 data hold time (BYTE="L")		25			ns
t _{PZX(E-P1Z)}	Port P1 floating release delay time (BYTE="L")		25			ักธ
th(E-PIA)	Port P1 address hold time (BYTE="H")		25			ns
th(ALE-P2A)	Port P2 address hold time		9			ns
th(E-P2Q)	Port P2 data hold time		25			ns
t _{PZX(E-P2Z)}	Port P2 floating release delay time		25			ns
th(E-BHE)	BHE hold time		20		1	ns
th(E-R/W)	R/W hold time		20			ns
tw(EL)	E pulse width		220		ļ	ns

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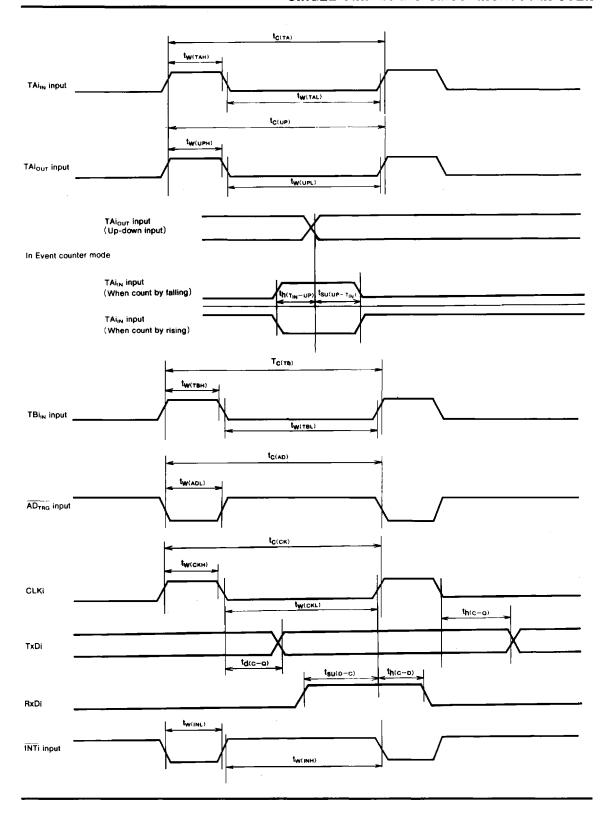
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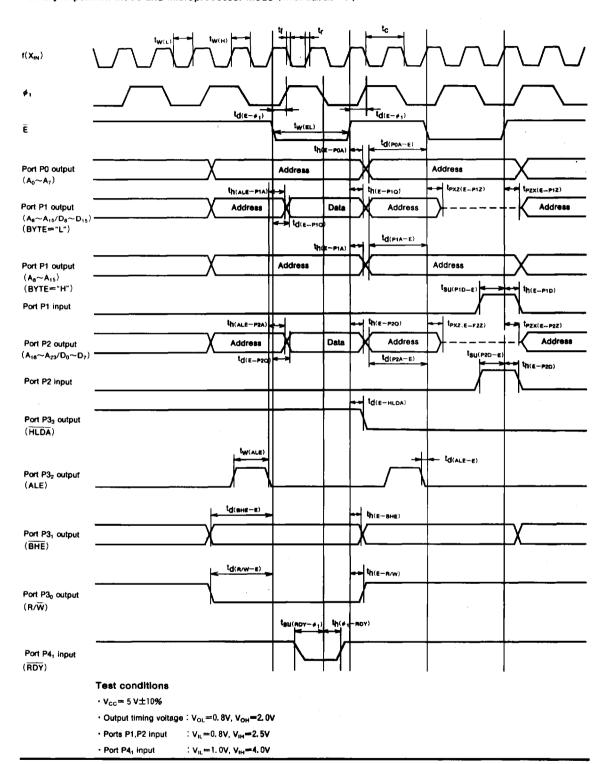
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SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER

Memory expansion mode and microprocessor mode (When wait bit="1")





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Memory expansion mode and microprocessor mode(when wait bit="0", and external memory area is accessed)

