AMD Enhanced 24-Pin PAL* Family

24-Pin IMOX™ Programmable Array Logic (PAL) Elements

PRELIMINARY

DISTINCTIVE CHARACTERISTICS

- AMD's superior IMOX technology
  - Guarantees $t_{PD} = 15$ ns max
- Individually programmable output polarity on each output
- Eight logical product terms per output
- Programming yields > 98% are realized via platinum-silicide fuse technology and the use of added test words
- Post Programming Functional Yield (PPFY) of 99.9%
- PRELOAD feature permits full logical verification
- Reliability assured through more than 70 billion fuse hours of life testing with no failures
- Full AC and DC parametric testing at the factory through on-board testing circuitry
- > 3000V ESD input protection per pin
- JEDEC-Standard LCC and PLCC pinout

GENERAL DESCRIPTION

AMD Enhanced 24-pin PAL devices are high-speed, electrically programmable array logic elements. They utilize the familiar sum-of-products (AND-OR) structure allowing users to program custom logic functions to fit most applications precisely. Typically they are a replacement for low-power Schottky SSI/MSI logic circuits, reducing chip count by more than 5 to 1 and greatly simplifying prototyping and board layout. Additional product terms, two additional outputs, and programmable output polarity are enhancements over industry-standard 24-pin PAL devices.

Five different devices are available, including both registered and combinatorial devices. All devices have user-programmable output polarity on all outputs. A variety of speed options allow the designer maximum flexibility in matching precise system requirements. The Product Selector Guide below shows the available speed options. The second table gives details about the functionality of the five available devices.

Please see the following pages for Block Diagrams.

PRODUCT SELECTOR GUIDE

AMD PAL Speed/Power Families

Family	t_{PD} ns (Max.)		t_S ns (Min.)		t_{CO} ns (Max.)		I_{CC} mA (Max.)	I_{OL} mA (Min.)	
	C Devices	M Devices	C Devices	M Devices	C Devices	M Devices	C/M Devices	C Devices	M Devices
Very High-Speed ("B") Versions	15	20	15	20	12	15	210	24	12
High-Speed ("A") Versions	25	30	25	30	15	20	210	24	12
High-Speed, Half-Power ("AL") Versions	25	30	25	30	15	20	105	24	12

Part Number	Array Inputs	Logic	Output Enable	Outputs/Polarity	Package Pins
22P10	12 Dedicated, 10 Bidirectional	Ten (8)-Wide AND-OR	Programmable	Bidirectional/Programmable	24
20RP4	10 Dedicated, 4 Feedback, 6 Bidirectional	Four (8)-Wide AND-OR	Dedicated	Registered/Programmable	24
		Six 8-Wide AND-OR	Programmable	Bidirectional/Programmable	
20RP6	10 Dedicated, 6 Feedback, 4 Bidirectional	Six (8)-Wide AND-OR	Dedicated	Registered/Programmable	24
		Four 8-Wide AND-OR	Programmable	Bidirectional/Programmable	
20RP8	10 Dedicated, 8 Feedback, 2 Bidirectional	Eight (8)-Wide AND-OR	Dedicated	Registered/Programmable	24
		Two 8-Wide AND-OR	Programmable	Bidirectional/Programmable	
20RP10	10 Dedicated, 10 Feedback	Ten (8)-Wide AND-OR	Dedicated	Registered/Programmable	24

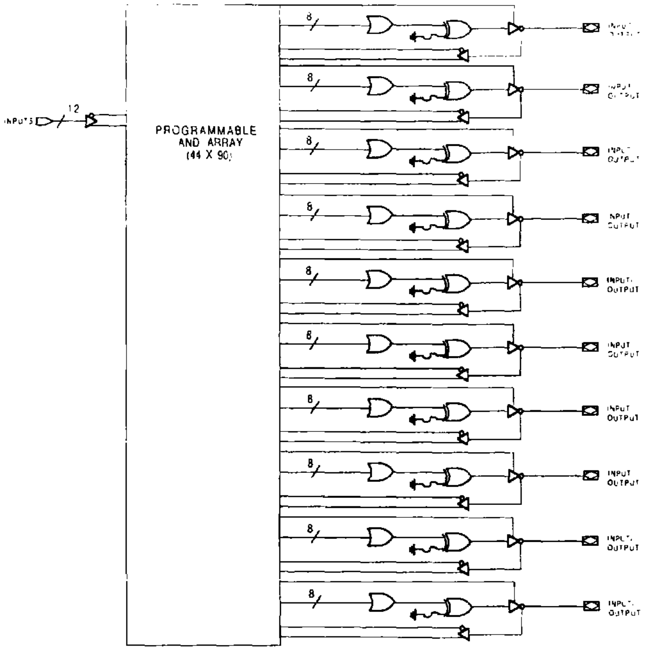
---

*PAL is a registered trademark of and is used under license from Monolithic Memories, Inc.

Publication # 08791 Rev. A Amendment /0
Issue Date: October 1986

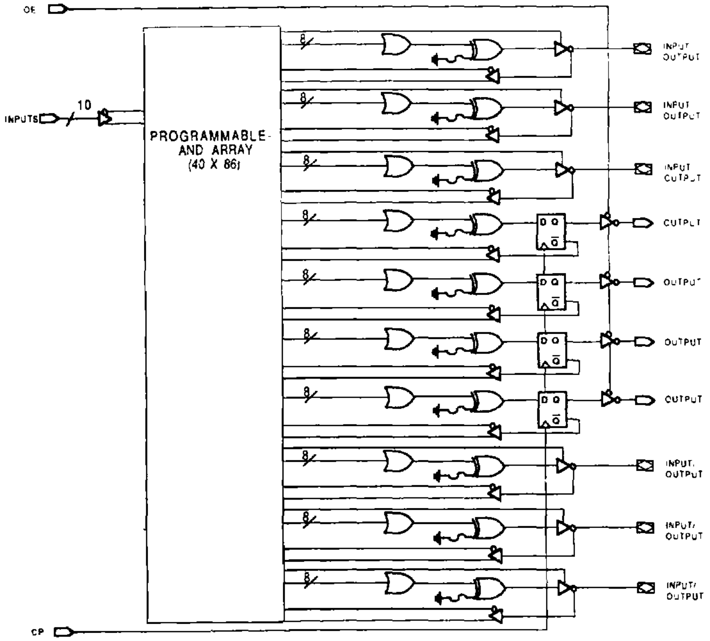
BLOCK DIAGRAMS

AmPAL22P10



LD001100

AmPAL20RP4



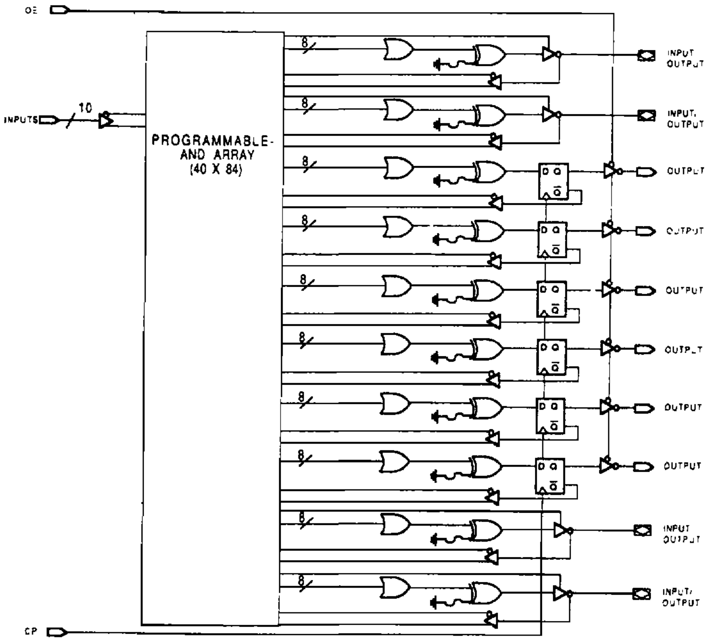
LD001110

---

*PAL is a registered trademark of and is used under license from Monolithic Memories, Inc.

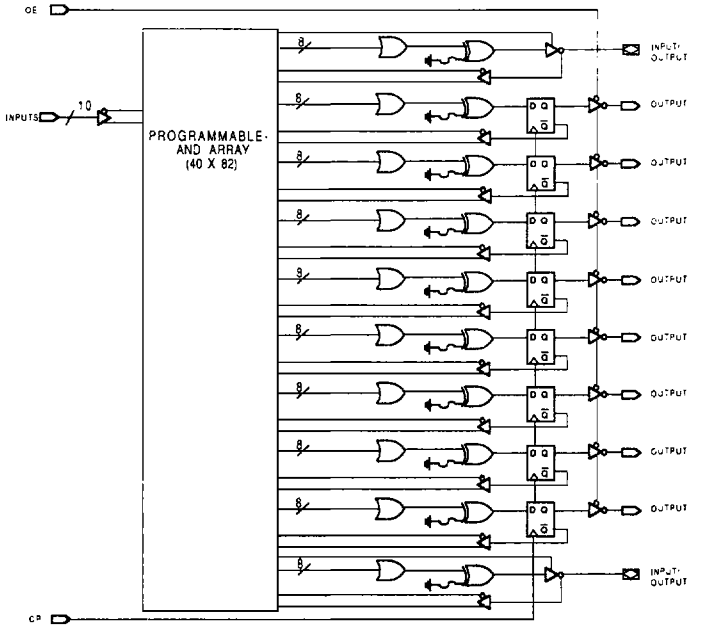
BLOCK DIAGRAMS (Cont'd.)

AmPAL20RP6



LD001120

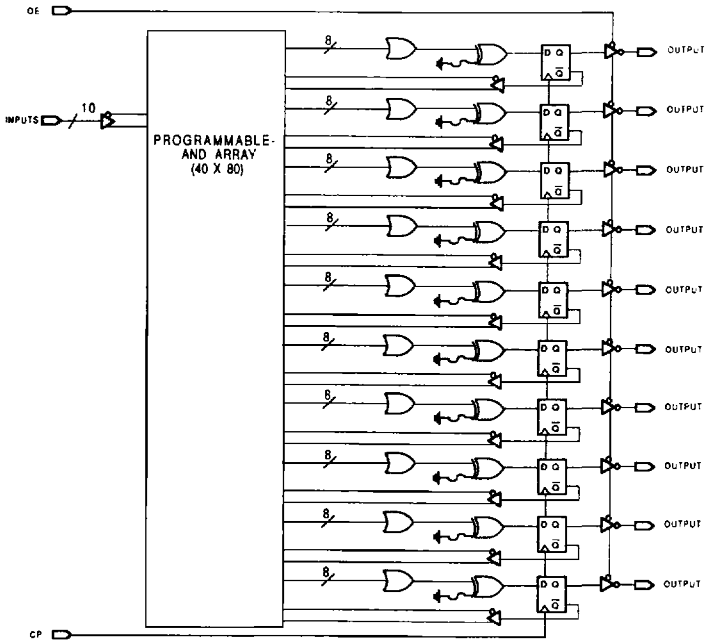
AmPAL20RP8



LD001130

BLOCK DIAGRAMS (Cont'd.)

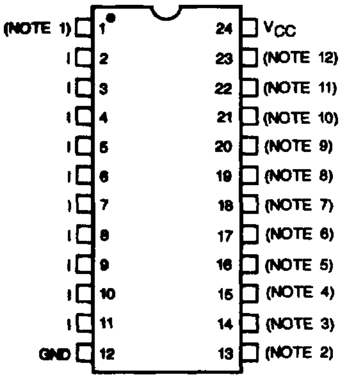
AmPAL20RP10



LD001140

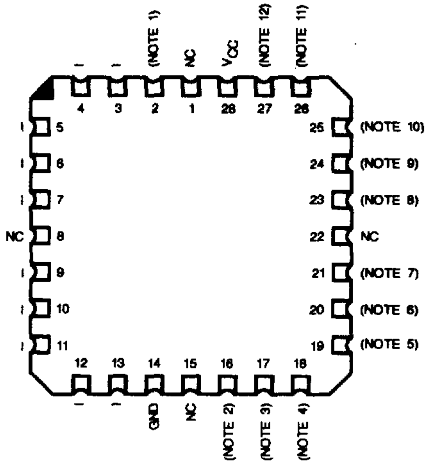
CONNECTION DIAGRAMS
Top View

DIPs*



CD010250

LCC**



CD010260

Note: Pin 1 is marked for orientation.

Notes:

	22P10	20RP4	20RP6	20RP8	20RP10
1	I	CLK	CLK	CLK	CLK
2	I	OE	OE	OE	OE
3	I/O	I/O	I/O	I/O	O
4	I/O	I/O	I/O	O	O
5	I/O	I/O	O	O	O
6	I/O	O	O	O	O
7	I/O	O	O	O	O
8	I/O	O	O	O	O
9	I/O	O	O	O	O
10	I/O	I/O	O	O	O
11	I/O	I/O	I/O	O	O
12	I/O	I/O	I/O	I/O	O

***Also available** in 24-Pin Ceramic Flatpack. Pinouts identical to DIPs.
****Also available** in 28-Pin Plastic Leaded Chip Carrier. Pinouts identical to LCC.

PIN DESIGNATIONS

I = Input
I/O = Input/Output
O = Output
V$_{CC}$ = Supply Voltage
GND = Ground
CLK = Clock
OE = Output Enable
NC = No Connect

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:
- **A. Device Number**
- **B. Speed Option** (if applicable)
- **C. Package Type**
- **D. Temperature Range**
- **E. Optional Processing**

AMPAL22P10 B P C

E. OPTIONAL PROCESSING
Blank = Standard processing
B = Burn In

D. TEMPERATURE RANGE
C = Commercial (0 to +75°C)
E = Extended Commercial (-55 to +125°C)

C. PACKAGE TYPE
P = 24-Pin Plastic DIP (PD 024)
D = 24-Pin Ceramic DIP (CD 024)
J = 28-Pin Plastic Leaded Chip Carrier (PL 028)
L = 28-Pin Ceramic Leadless Chip Carrier (CL 028)

B. SPEED/POWER
See Product Selector Guide

A. DEVICE NUMBER/DESCRIPTION
AMD Enhanced 24-Pin PAL Family
24-Pin IMOX Programmable Array Logic

Valid Combinations	
AMPAL22P10B/A/AL	PC, DC, DCB, DE, JC, LC, LE
AMPAL20RP4B/A/AL	
AMPAL20RP6B/A/AL	
AMPAL20RP8B/A/AL	
AMPAL20RP10B/A/AL	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION (Cont'd.)

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**

B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish

AMPAL22P10 B /B L A

E. LEAD FINISH
A = Hot Solder DIP
C = Gold

D. PACKAGE TYPE
L = 24-Pin Ceramic DIP (CD 024)
3 = 28-Pin Ceramic Leadless Chip Carrier (CL 028)
K = 24-Pin Ceramic Flatpack (CF 024)

C. DEVICE CLASS
/B = Class B

B. SPEED/POWER
See Product Selector Guide

A. DEVICE NUMBER/DESCRIPTION
AMD Enhanced 24-Pin PAL Family
24-Pin IMOX Programmable Array Logic

Valid Combinations	
AMPAL22P10B/A/AL	/BLA, /B3C, /BKA
AMPAL20RP4B/A/AL	
AMPAL20RP6B/A/AL	
AMPAL20RP8B/A/AL	
AMPAL20RP10B/A/AL	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups
1, 2, 3, 7, 8, 9, 10, & 11

FUNCTIONAL DESCRIPTION

AMD Enhanced 24-Pin PAL Family Characteristics

All members of the AMD Enhanced 24-Pin PAL Family have common electrical characteristics and programming procedures. All parts are produced with a fusible link at each input to the AND gate array, and connections may be selectively removed by applying appropriate voltages to the circuit.

Initially the AND gates are connected, via fuses, to both the true and complement of each input. By selective programming of fuses the AND gates may be "connected" to only the true input (by blowing the complement fuse), to only the complement input (by blowing the true fuse), or to neither type of input (by blowing both fuses) establishing a logical "don't care." When both the true and complement fuses are left intact a logical false results on the output of the AND gate, while all fuses blown results in a logical true state. For combinatorial outputs, the AND gates are connected to fixed-OR gates whose outputs become device outputs. For registered outputs, the AND gates are connected to fixed-OR gates whose outputs become output register inputs.

All parts are fabricated with AMD's fast programming, highly reliable Platinum-Silicide Fuse technology. Utilizing an easily implemented programming algorithm, these products can be rapidly programmed to any customized pattern. Extra test words are pre-programmed during manufacturing to insure extremely high field programming yields (> 98%), and provide extra test paths to achieve excellent parametric correlation.

Power-Up Reset

The registered devices in the AMD PAL family have been designed to reset during system power-up. Following power-up, all registers will be initialized to zero, setting all the outputs to a logic 1. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization.

PRELOAD

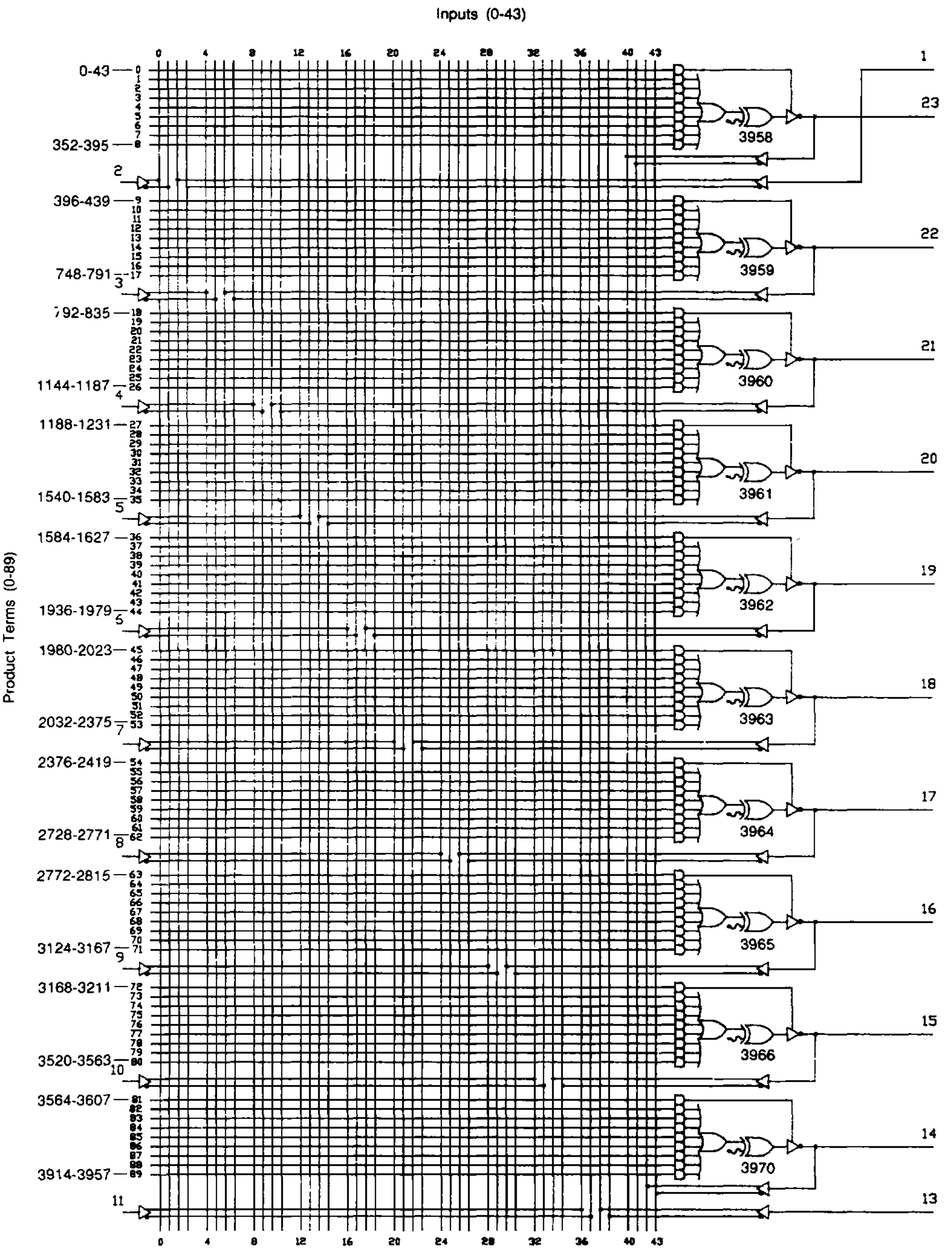
AMD PAL devices are designed with unique PRELOAD circuitry that provides an easy method of testing registered devices for logical functionality. PRELOAD allows any arbitrary state value to be loaded into the registered output of an AMD PAL device.

A typical functional test sequence would be to verify all possible state transitions for the device being tested. This requires the ability to set the state registers into an arbitrary "present state" value and to set the device inputs to any arbitrary "present input" value. Once this is done, the state machine is clocked into a new state or "next state." The next state is then checked to validate the transition from the present state. In this way any state transition can be checked.

Without PRELOAD, it is difficult and in some cases impossible to load an arbitrary present state value. This can lead to logic verification sequences that are either incomplete or excessively long. Long test sequences result when the feedback from the state register "interferes" with the inputs, forcing the machine to go through many transitions before it can reach an arbitrary state value. Therefore the test sequence will be mostly state initialization and not actual testing. The test sequence becomes excessively long when a state must be reentered many times to test a wide variety of input combinations.

In addition, complete logic verification may become impossible when states that need to be tested cannot be entered with normal state transitions. For example, even though necessary, the state entered when a machine powers up cannot be tested, because it cannot be entered from the main sequence. Similarly, "forbidden" or don't care states that are not normally entered need to be tested to ensure that they return to the main sequence.

PRELOAD eliminates these problems by providing the capability to go directly to any desired arbitrary state. Thus test sequences may be greatly shortened, and all possible states can be tested, greatly reducing test time and development costs, and guaranteeing proper in-system operation.



LD001270

Figure 1. AmPAL22P10 Logic Diagram and JEDEC Fuse Numbering

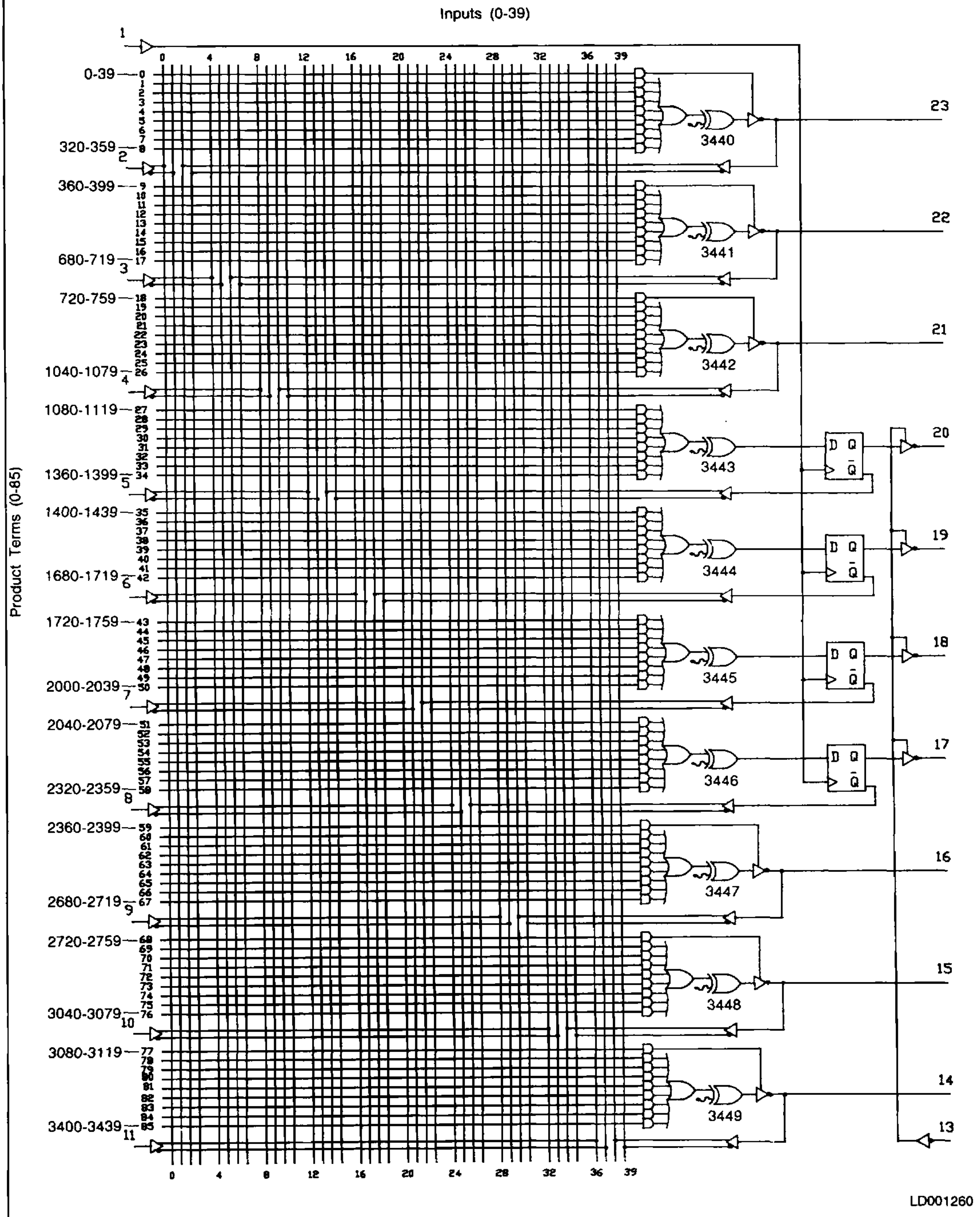
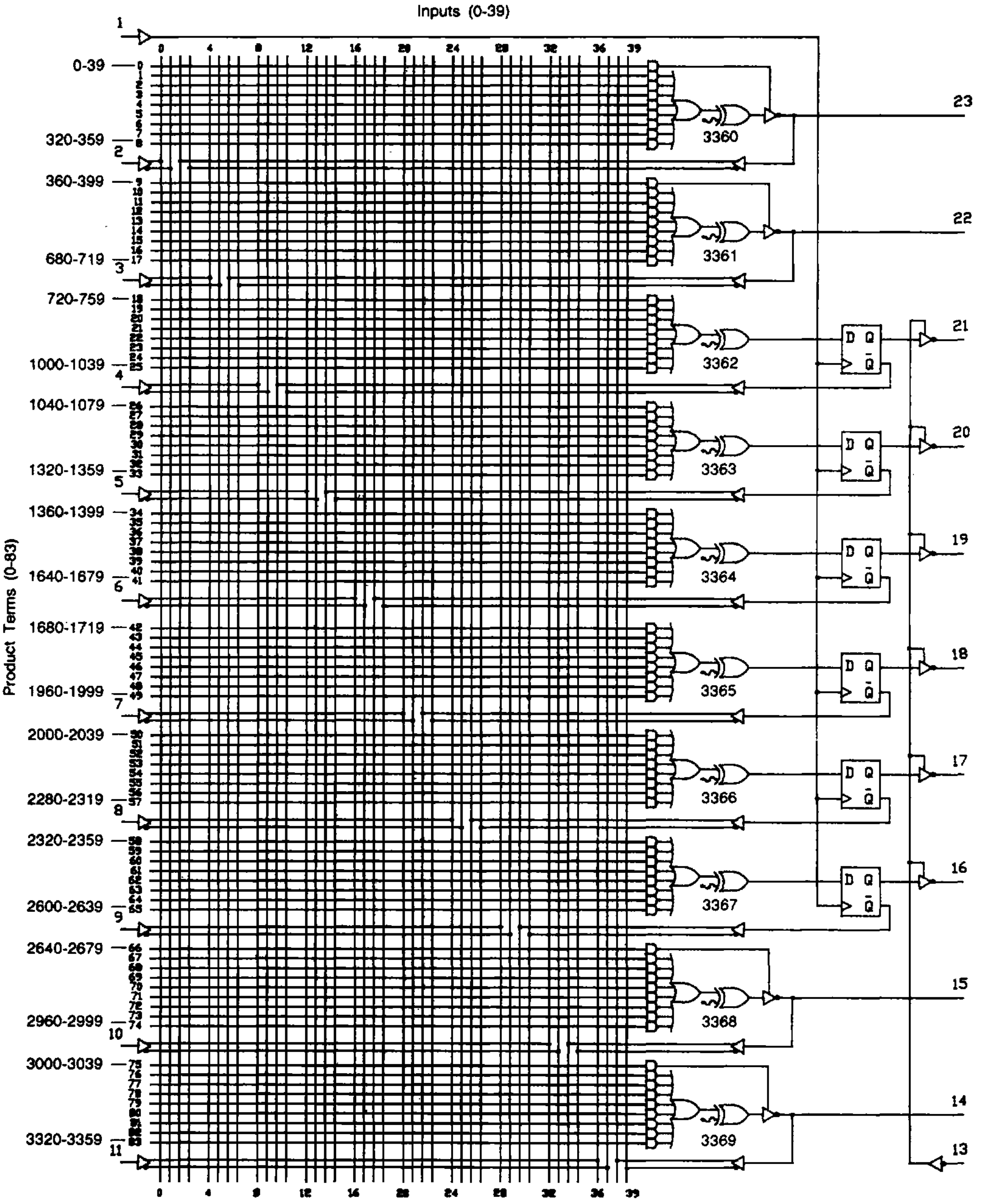


Figure 2. AmPAL20RP4 Logic Diagram and JEDEC Fuse Numbering



LD001250

Figure 3. AmPAL20RP6 Logic Diagram and JEDEC Fuse Numbering

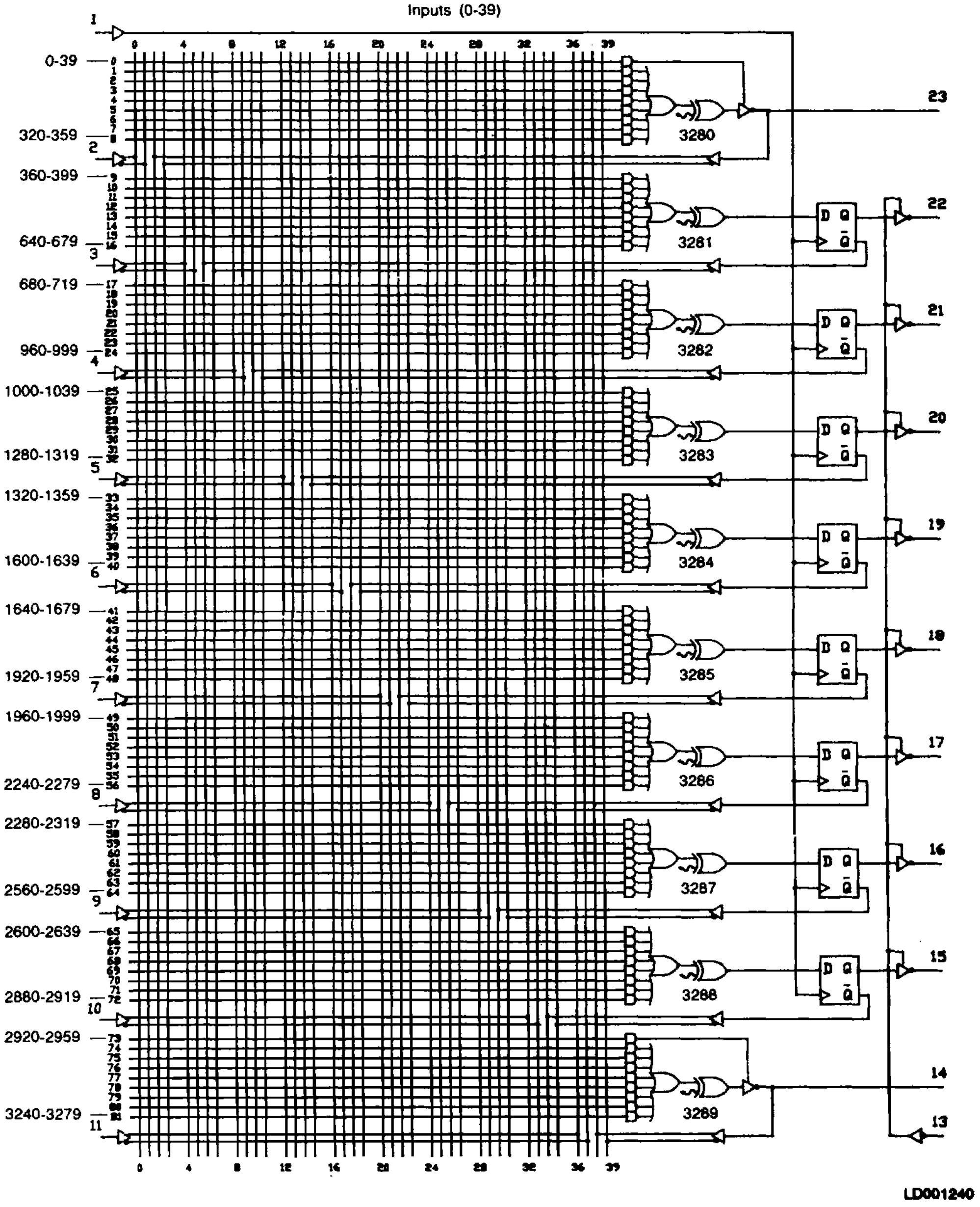
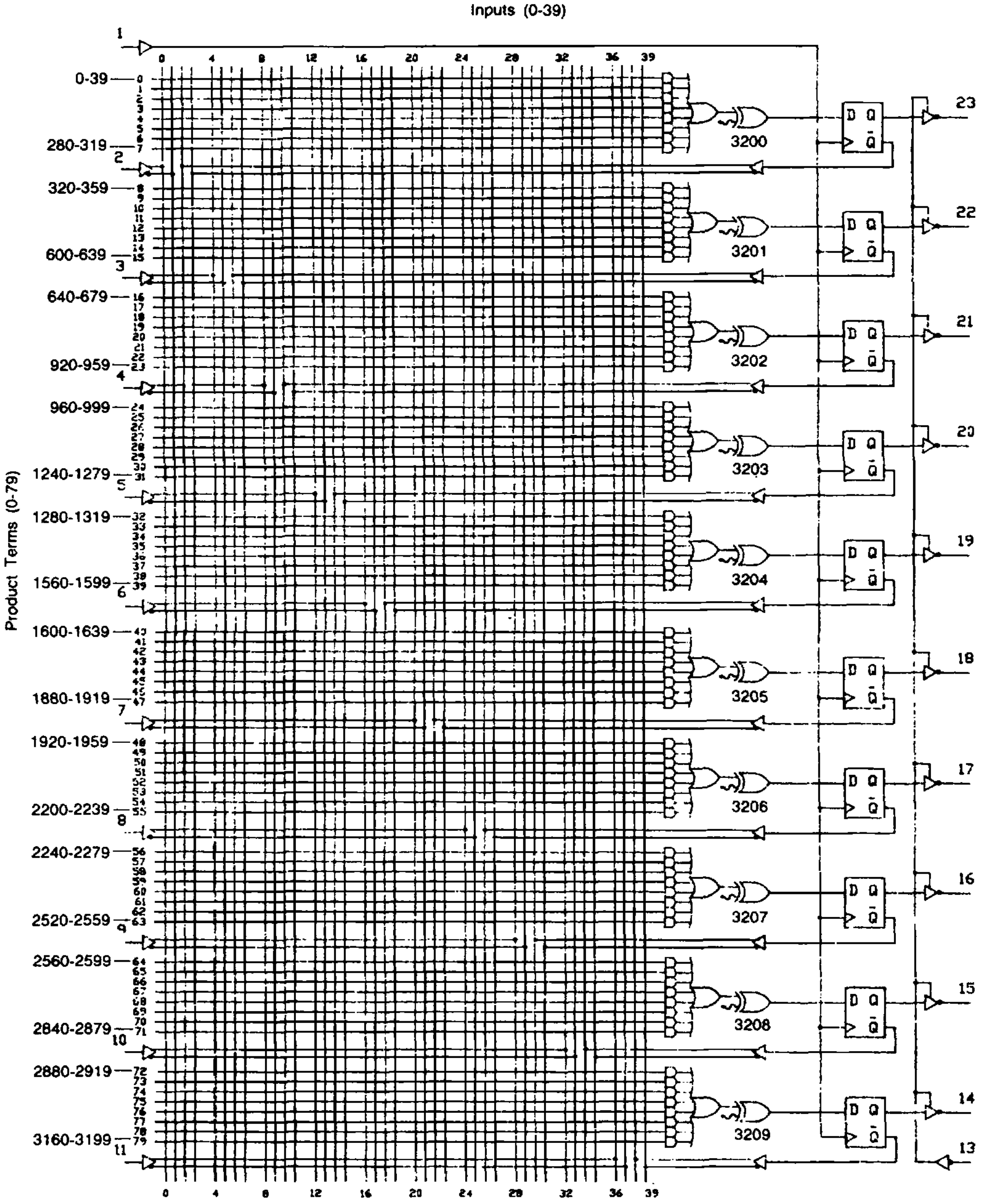


Figure 4. AmPAL20RP8 Logic Diagram and JEDEC Fuse Numbering



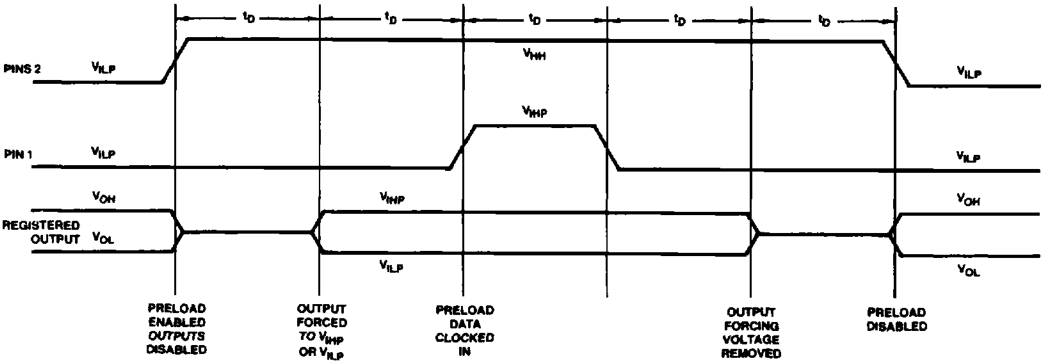
LD001280

Figure 5. AmPAL20RP10 Logic Diagram and JEDEC Fuse Numbering

PRELOAD of Registered Outputs

The AMD Enhanced 24-pin PAL devices incorporate circuitry to allow loading each register synchronously to either a HIGH or LOW state. This feature simplifies testing since any initial state for the registers can be set to optimize test sequencing.

The pin levels and timing necessary to perform the PRELOAD function are detailed below:



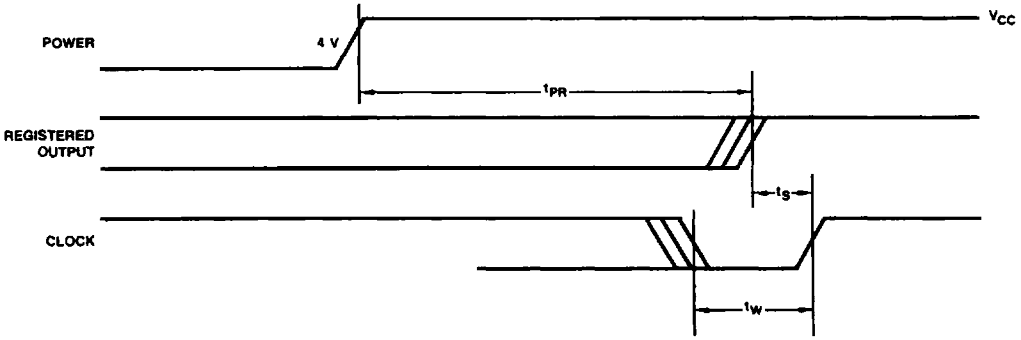
WF022294

Level forced on registered output pin during PRELOAD cycle	Register Q output state after cycle
V_{IHP}	HIGH
V_{ILP}	LOW

Power-Up Reset

The registered devices in the AMD Enhanced 24-Pin PAL Family have been designed with the capability to reset during system power-up. Following power-up, all registers will be reset to LOW. The output state will be HIGH. This feature provides flexibility to the designer and is especially valuable in simplifying state-machine initialization. A timing diagram and parameter table are shown below. Due to the asynchronous operation of the power-up RESET and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up RESET. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.



WF022300

Parameters	Description	Min.	Typ.	Max.	Units
t_{PR}	Power-Up Reset Time		600	1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics			
t_W	Clock Width				

ABSOLUTE MAXIMUM RATINGS

Storage Temperature .... −65 to +150°C
Supply Voltage to Ground Potential
(Pin 24 to Pin 12) Continuous .... −0.5 to +7.0 V
DC Voltage Applied to Outputs
(Except During Programming) .... −0.5 V to +V_{CC} Max.
DC Voltage Applied to Outputs
During Programming .... 16 V
Output Current Into Outputs During
Programming (Max Duration of 1 sec) .... 200 mA
DC Input Voltage .... −0.5 to +5.5 V
DC Input Current .... −30 to +5 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_A) .... 0 to +75°C
Supply Voltage (V_{CC}) .... +4.75 to +5.25 V
Extended Commercial (E) Devices
Temperature (T_A) .... −55°C Min.
Temperature (T_C) .... +125°C Max.
Supply Voltage (V_{CC}) .... +4.50 to +5.50 V
Military (M) Devices*
Temperature (T_A) .... −55°C Min.
Temperature (T_C) .... +125°C Max.
Supply Voltage (V_{CC}) .... +4.50 to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

*Military product 100% tested at T_C = +25°C, +125°C, and −55°C.

DC CHARACTERISTICS over operating range unless otherwise specified; included in Group A, Subgroup 1, 2, 3 tests unless otherwise noted

Parameter Symbol	Parameter Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = −3.2 mA COM'L	2.4	[illegible]		V
			I_{OH} = −2 mA MIL				
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = −24 mA COM'L			[illegible]	V
			I_{OL} = −12 mA MIL				
V_{IH} (Note 2)	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs		[illegible]		5.5	V
V_{IL} (Note 2)	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs				0.8	V
I_{IL}	Input LOW Current	V_{CC} = Max., I_{IN} = 0.40 V			−20	−100	μA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 2.7 V				25	μA
I_I	Input HIGH Current	V_{CC} = Max., V_{IN} = 5.5 [illegible]				1.0	mA
I_{SC}	Output Short-Circuit Current	V_{CC} = Max., [illegible] 0.5 [illegible]		−30	−60	−90	mA
I_{CC}	Power Supply Current	V_{CC} = Ma[illegible]	[illegible],			210	mA
			[illegible]AL			105	
V_I	Input Clamp Voltage	[illegible]C = Min., [illegible] mA			−0.9	−1.2	V
I_{OZH}	Output Leakage C[illegible] (Note 4)	[illegible] = Max., V_{IL} [illegible].8 V V[illegible] 2.0 [illegible]	V_O = 2.7 V			100	μA
I_{OZL}			V_O = 0.4 V			−100	

Notes: 1. Typical limits [illegible] and T[illegible] C.
2. These are [illegible]ute va[illegible]s [illegible] resp[illegible] device ground and all overshoots due to system or tester noise are included.
3. Not more th[illegible] one [illegible] sh[illegible] tested at a time. Duration of the short circuit should not be more than one second. V[illegible] V [illegible] en[illegible] avoid test problems caused by tester ground degradation.
4. [illegible] pin [illegible] the wo[illegible]case of I_{OZX} or I_{IX} (where X = H or L).

CAPACIT[illegible]

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Units
C_{IN}	Input Capacitance	V_{IN} = 2.0 V @ f = 1 MHz	Pins 1, 13	11	pF
			Others	6	
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V @ f = 1 MHz		9	

*These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified; included in Group A Subgroup 9, 10, 11 tests unless otherwise noted

COMMERCIAL RANGE

No.	Parameter Symbol	Parameter Description	"B" Version Typ. (Note 1)	"B" Version Min.	"B" Version Max.	"A" & "AL" Versions Typ. (Note 1)	"A" & "AL" Versions [illegible]	"A" & "AL" Versions M[illegible]	Units
1	t_{PD}	Input or Feedback to Non-Registered Output 22P10, 20RP4, 20RP6, 20RP8			15			[illegible]	ns
2	t_{EA}	Input to Output Enable 22P10, 20RP4, 20RP6, 20RP8			[illegible]			[illegible]	ns
3	t_{ER}	Input to Output Disable 22P10, 20RP4, 20[illegible] 20RP8			[illegible]			25	ns
4	t_{PZX}	Pin 13 to Output Enable 2[illegible]4, [illegible] 20RP10			15			20	ns
5	t_{PXZ}	P[illegible] Output Disable 20[illegible] 2[illegible]10			12			20	ns
6	[illegible]CO	Cl[illegible]put [illegible]P4, 20R[illegible] 20[illegible]8, 20RP10			12			15	ns
[illegible]	[illegible]	Inp[illegible]r Feedback[illegible] Time 20RP4, 20RP6, 20R[illegible]		15			25		ns
8	[illegible]	[illegible]ld Time 20RP4, 20RP6, 20RP8, 20RP10		0			0		ns
9	t_P	Clock Period ($t_S + t_{CO}$)		27			40		ns
10	t_{WL}/t_{WH}	Clock Width		10/12			15/15		ns
11	$f_{MAX.}$	Maximum Frequency			37.0			25.0	MHz

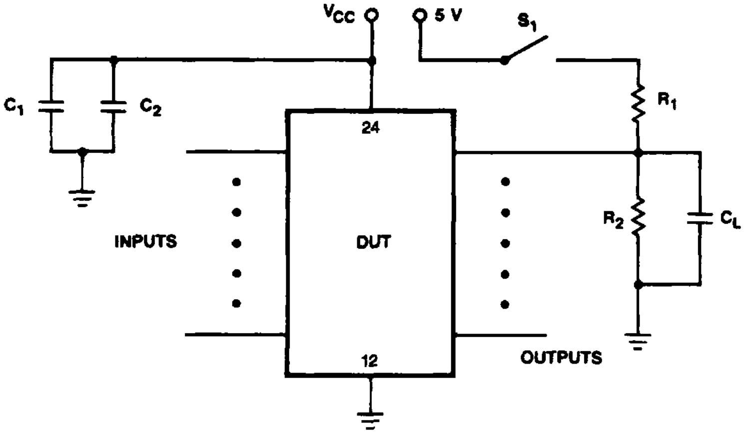
Notes: 1. Typical limits are at $V_{CC} = 5.0$ V and $T_A = 25°C$.
2. t_{PD} is tested with switch S_1 closed and $C_L = 50$ pF.
3. For three-state outputs, output enable times are tested with $C_L = 50$ pF to the 1.5 V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. Output disable times are tested with $C_L = 5$ pF. HIGH to high impedance tests are made to an output voltage of $V_{OH} - 0.5$ V with S_1 open; LOW to high impedance tests are made to the $V_{OL} + 0.5$ V level with S_1 closed.

MILITARY RANGE

No.	Parameter Symbol	Parameter Description	"B" Version Typ. (Note 1)	"B" Version Min.	"B" Version Max.	"A" & "AL" Versions Typ. (Note 1)	"A" & "AL" Versions [illegible]	"A" & "AL" Versions M[illegible]	Units
1	t_{PD}	Input or Feedback to Non-Registered Output 22P10, 20RP4, 20RP6, 20RP8			20			[illegible]	ns
2	t_{EA}	Input to Output Enable 22P10, 20RP4, 20RP6, 20RP8			25			[illegible]	ns
3	t_{ER}	Input to Output Disable 22P10, 20RP4, 20[illegible] 20RP8			[illegible]			30	ns
4	t_{PZX}	Pin 13 to Output Enable 2[illegible]4, [illegible] 20RP10			20			25	ns
5	t_{PXZ}	P[illegible] Output Disable 20[illegible] 2[illegible]10			20			25	ns
6	[illegible]	Cl[illegible] Output [illegible]P4, [illegible] 20RP8, 20RP10			15			20	ns
[illegible]	[illegible]	Inp[illegible]r Feedback[illegible] Time 20RP4, 20RP6, 20R[illegible]		20			30		ns
8	[illegible]H	[illegible]ld Time 20RP4, 20RP6, 20RP8, 20RP10		0			0		ns
9	t_P	Clock Period ($t_S + t_{CO}$)		35			50		ns
10	t_{WL}/t_{WH}	Clock Width		12/12			20/20		ns
11	$f_{MAX.}$	Maximum Frequency			28.6			20.0	MHz

Notes: 1. Typical limits are at $V_{CC} = 5.0$ V and $T_A = 25°C$.
2. t_{PD} is tested with switch S_1 closed and $C_L = 50$ pF.
3. For three-state outputs, output enable times are tested with $C_L = 50$ pF to the 1.5 V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. Output disable times are tested with $C_L = 5$ pF. HIGH to high *impedance tests are made to an output voltage of $V_{OH} - 0.5$ V with S_1 open; LOW to high impedance tests are made to the* $V_{OL} + 0.5$ V level with S_1 closed.

SWITCHING TEST CIRCUIT

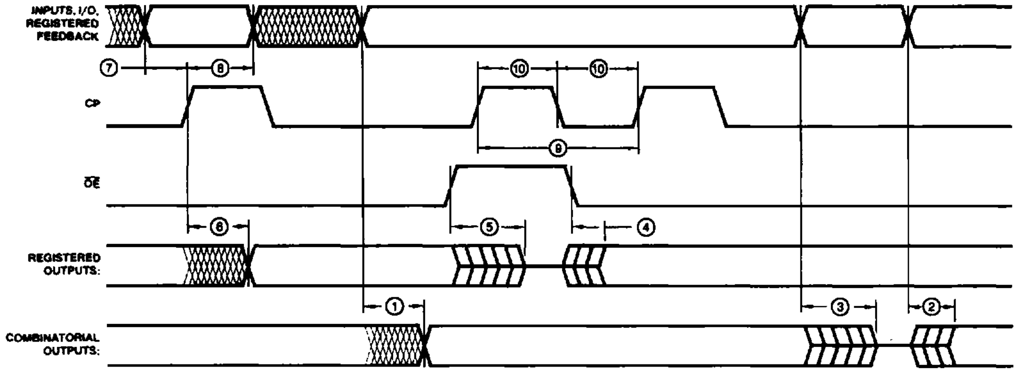


TC003051

Note: C_1 and C_2 are to bypass V_{CC} to ground.

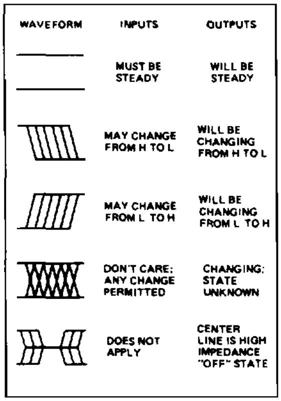
TEST OUTPUT LOADS		
Pin Name	**Commercial**	**Military**
R_1	200 Ω	390 Ω
R_2	390 Ω	750 Ω
C_1	1 μF	1 μF
C_2	0.1 μF	0.1 μF
C_L	50 pF	50 pF

SWITCHING WAVEFORMS



WF002571

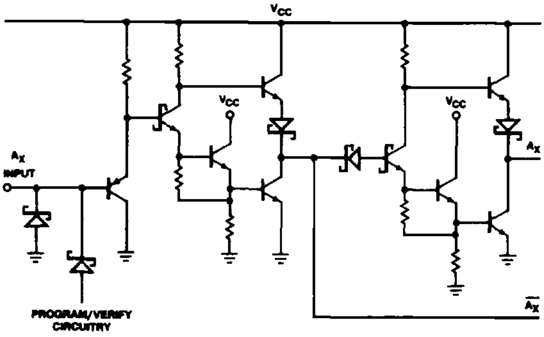
KEY TO TIMING DIAGRAM



WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

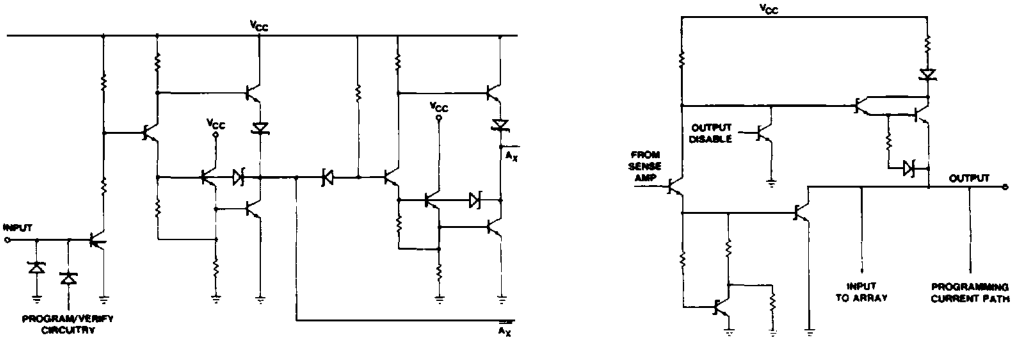
KS000010

INPUT CIRCUITRY



IC000720

OUTPUT CIRCUITRY



IC000801

Programming and Verification

AMD Enhanced 24-Pin PAL Family devices are programmed and verified using AMD's standard programmable logic algorithm. The fuse to be programmed is selected by input line number (array row), product term (array column), and by output (one at a time). The fuse is then programmed and verified by applying a simple sequence of voltages to two control pins (1 and 13).

Input line numbers are addressed using a full decode scheme via TTL levels on pins 6-11 where 6 is the LSB and 11 is the MSB. Even-numbered input lines represent the true version of a signal and odd-numbered lines represent the complement. Input line addressing is shown in Table 1. Note that input line 63 is utilized for selecting the fuses used for programming output polarity.

Product terms are addressed using a 1-of-16 addressing scheme on pins 2-5 where pin 2 is the LSB and 5 is the MSB. Product term addressing is shown in Table 2. Logical and architectural product terms are selected via TTL levels on the four addressing pins.

Fuse selection by output must be done one output at a time (following control pin 1 going to V_{HH}), as shown in the programming timing diagram.

Once fuses have been selected, the simple programming and verification sequence may be completed as shown in the programming timing diagram. AC and DC requirements for programming are shown in the programming parameter table.

Security Fuse Programming

A single fuse is provided on each device to prevent unauthorized copying of PAL fuse patterns. Once blown, the circuitry enabling fuse verification and registered output PRELOAD is permanently disabled.

Programming of the security fuse is the same as an array fuse. Verification of a blown security fuse is accomplished by verifying the whole fuse array as if every fuse is blown.

Programming Yield

AMD PAL devices have been designed to ensure extremely high programming yields (> 98%). To help ensure that a part was correctly programmed, once programming is completed, the entire fuse array should be verified at both LOW and HIGH V_{CC}. Reverification can be accomplished by reading all ten outputs in parallel rather than one at a time. This verification cycle checks that the array fuses have been blown and can be sensed by the outputs under varying conditions.

AMD PAL devices contain many internal test features, including circuitry and extra fuses which allow AMD to test the ability of each part to perform programming before shipping, to assure high programming yields and correct logical operation for a correctly programmed part. Programming yield losses are most likely due to poor programming socket contact, programming equipment out of calibration, or improper usage of said equipment.

PROGRAMMING PARAMETERS $T_A = 25°C$

Parameter Symbol	Parameter Description		Min.	Typ.	Max.	Units
V_{HH}	Control Pin Extra High Level	Pin 1 @ 5-10 mA	10	11	12	V
		Pin 13 @ 5-10 mA	10	11	12	
V_{OP}	Program Voltage Pins 14-23 @ 15-200 mA		14	15	16	V
V_{IHP}	Input HIGH Level During Programming and Verify		2.4	5	5.5	V
V_{ILP}	Input LOW Level During Programming and Verify		0.0	0.3	0.5	V
V_{CCP}	V_{CC} During Programming @ I_{CC} = 50-275 mA		5	5.2	5.5	V
V_{CCL}	V_{CC} During First Pass Verification @ I_{CC} = 50-275 mA		4.4	4.5	4.6	V
V_{CCH}	V_{CC} During Second Pass Verification @ I_{CC} = 50-275 mA		5.4	5.5	5.6	V
V_{Blown}	Successful Blown Fuse Sense Level @ Output			0.3	0.5	V
V_{OP}/dt	Rate of Output Voltage Change		20		250	V/µs
dV_{13}/dt	Rate of Fusing Enable Voltage Change (Pin 13 Rising Edge)		100		1000	V/µs
t_P	Fusing Time First Attempt		40	50	100	µs
	Subsequent Attempts		4	5	10	ms
t_D	Delays Between Various Level Changes		100	200	1000	ns
t_V	Period During which Output is Sensed for V_{Blown} Level				500	ns
V_{ONP}	Pull-Up Voltage On Outputs Not Being Programmed		$V_{CCP} - 0.3$	V_{CCP}	$V_{CCP} + 0.3$	V
R	Pull-Up Resistor On Outputs Not Being Programmed		1.9	2	2.1	kΩ

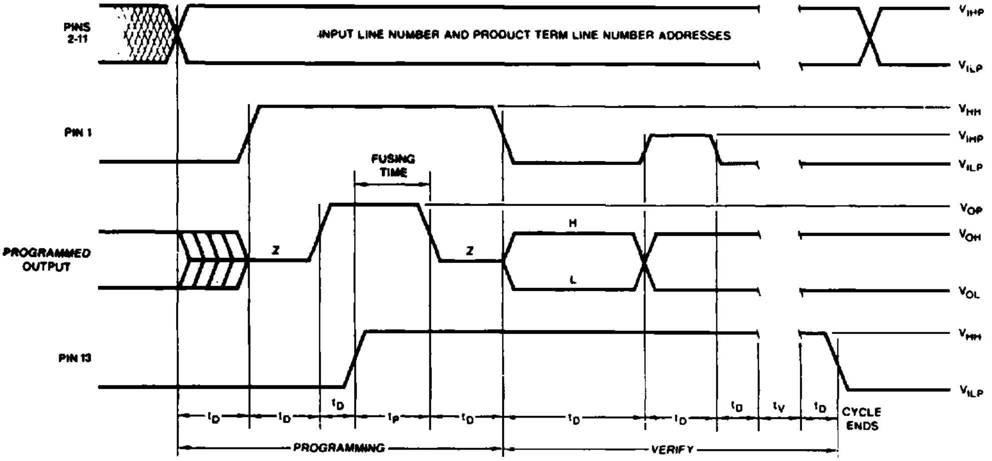
Design Aid Software for AMD Enhanced 24-Pin PAL Family

Name	Vendor	Versions	Notes
ABEL	Data I/O (206) 881-6444	IBM PC VAX/VMS VAX/UNIX	
CUPL	P-CAD Systems (408) 971-1300	IBM PC VAX/VMS VAX/UNIX CPM 80/86	
AmCUPL	Advanced Micro Devices (408) 732-2400	IBM PC	Supported by P-CAD Systems

AMD Qualified Programmers

Name	Programmer Model(s)	AMD PAL Personality Module	Socket Adapter
Data I/O 10525 Willow Road N.E. Redmond, WA 93052	Systems 19, 29	950-1942-0044	303A-011A
	60	N/A	Under Development
Stag Microsystems 528-5 Weddell Drive Sunnyvale, CA 94086	Model PPZ	Under Development	On Board
	ZL30	Under Development	
Valley Data Sciences 2426 Charleston Road Mountain View, CA 94043	160 Series	Under Development	On Board

PROGRAMMING TIMING DIAGRAM



PF001101

TABLE 1. INPUT ADDRESSING

Input Line Number	Input Line Number Address Pin States					
	6	7	8	9	10	11
0	L	L	L	L	L	L
1	L	L	L	L	L	H
2	L	L	L	L	H	L
3	L	L	L	L	H	H
4	L	L	L	H	L	L
5	L	L	L	H	L	H
6	L	L	L	H	H	L
7	L	L	L	H	H	H
8	L	L	H	L	L	L
9	L	L	H	L	L	H
10	L	L	H	L	H	L
11	L	L	H	L	H	H
12	L	L	H	H	L	L
13	L	L	H	H	L	H
14	L	L	H	H	H	L
15	L	L	H	H	H	H
16	L	H	L	L	L	L
17	L	H	L	L	L	H
18	L	H	L	L	H	L
19	L	H	L	L	H	H
20	L	H	L	H	L	L
21	L	H	L	H	L	H
22	L	H	L	H	H	L
23	L	H	L	H	H	H
24	L	H	H	L	L	L
25	L	H	H	L	L	H
26	L	H	H	L	H	L
27	L	H	H	L	H	H
28	L	H	H	H	L	L
29	L	H	H	H	L	H
30	L	H	H	H	H	L
31	L	H	H	H	H	H
32	H	L	L	L	L	L
33	H	L	L	L	L	H
34	H	L	L	L	H	L
35	H	L	L	L	H	H
36	H	L	L	H	L	L
37	H	L	L	H	L	H
38	H	L	L	H	H	L
39	H	L	L	H	H	H
40*	H	L	H	L	L	L
41*	H	L	H	L	L	H
42*	H	L	H	L	H	L
43*	H	L	H	L	H	H
63**	H	H	H	H	H	H

* Used for AmPAL22P10 only

** Used for programming polarity

L = V_{ILP}

H = V_{IHP}

TABLE 2-1. PRODUCT TERM ADDRESSING (AmPAL22P10)

Product Term Select Address Pin				Programming Access and Verify Pin									
5	4	3	2	23	22	21	20	19	18	17	16	15	14
L	L	L	L	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]
L	L	L	H	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]
L	L	H	L	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]
L	L	H	H	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]
L	H	L	L	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]
L	H	L	H	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]
L	H	H	L	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]
L	H	H	H	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]
H	L	L	L	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]
H	L	L	H	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]
H	H	H	H	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]
				Logical/Architectural Product Term Line Number									

L = V_{ILP}
H = V_{IHP}
OE = Output Enable
POL = Polarity
SF = Security Fuse

TABLE 2-2. PRODUCT TERM ADDRESSING (AmPAL20RP4)

Product Term Select Address Pin				Programming Access and Verify Pin									
5	4	3	2	23	22	21	20	19	18	17	16	15	14
L	L	L	L	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]
L	L	L	H	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]
L	L	H	L	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]
L	L	H	H	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]
L	H	L	L	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]
L	H	L	H	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]
L	H	H	L	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]
L	H	H	H	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]
H	L	L	L	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]
H	L	L	H	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]
H	H	H	H	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]
				Logical/Architectural Product Term Line Number									

L = V_{ILP}
H = V_{IHP}
OE = Output Enable
POL = Polarity
SF = Security Fuse

TABLE 2-3. PRODUCT TERM ADDRESSING (AmPAL20RP6)

Product Term Select Address Pin				Programming Access and Verify Pin									
5	4	3	2	23	22	21	20	19	18	17	16	15	14
L	L	L	L	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
L	L	L	H	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
L	L	H	L	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
L	L	H	H	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
L	H	L	L	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
L	H	L	H	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
L	H	H	L	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
L	H	H	H	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
H	L	L	L	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
H	L	L	H	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
H	H	H	H	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]

Logical/Architectural Product Term Line Number

L = V_{ILP}
H = V_{IHP}
OE = Output Enable
POL = Polarity
SF = Security Fuse

TABLE 2-4. PRODUCT TERM ADDRESSING (AmPAL20RP8)

Product Term Select Address Pin				Programming Access and Verify Pin									
5	4	3	2	23	22	21	20	19	18	17	16	15	14
L	L	L	L	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
L	L	L	H	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
L	L	H	L	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
L	L	H	H	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
L	H	L	L	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
L	H	L	H	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
L	H	H	L	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
L	H	H	H	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
H	L	L	L	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
H	L	L	H	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
H	H	H	H	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]

Logical/Architectural Product Term Line Number

L = V_{ILP}
H = V_{IHP}
OE = Output Enable
POL = Polarity
SF = Security Fuse

TABLE 2-5. PRODUCT TERM ADDRESSING (AmPAL20RP10)

Product Term Select Address Pin				Programming Access and Verify Pin									
5	4	3	2	23	22	21	20	19	18	17	16	15	14
L	L	L	L	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]
L	L	L	H	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]
L	L	H	L	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]
L	L	H	H	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]
L	H	L	L	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]
L	H	L	H	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]
L	H	H	L	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]
L	H	H	H	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]
H	L	L	L	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]
H	L	L	H	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]
H	H	H	H	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]
				Logical/Architectural Product Term Line Number									

L = V_{ILP}
H = V_{IHP}
OE = Output Enable
POL = Polarity
SF = Security Fuse