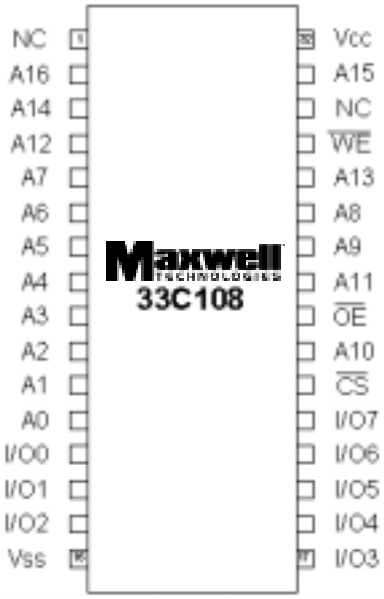
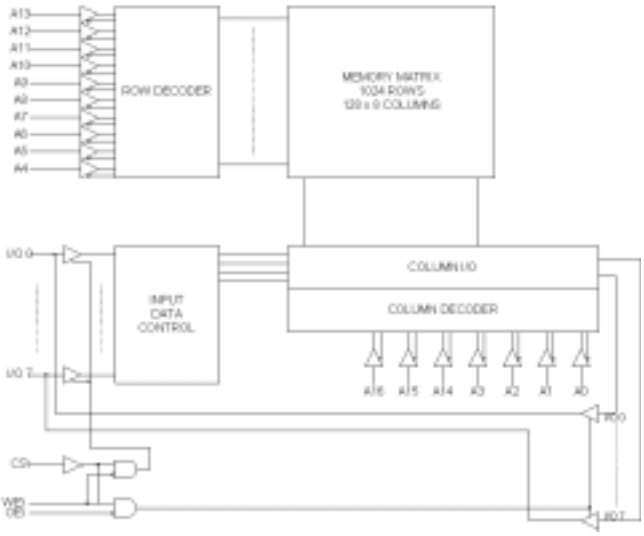
33C108
1 Megabit (128K x 8-Bit) CMOS SRAM





Functional Block Diagram

FEATURES:

- RAD-PAK® Technology radiation-hardened against natural space radiation
- 128K x 8 bit organization
- Total dose hardness:
  - > 100 krad (Si)
  - dependent upon space mission
- Excellent Single Event Effects:
  - SEL_{TH}: No LU > 68 MeV/mg/cm^2
  - SEU_{TH}: < 3 MeV/mg/cm^2
- Package:
  - 32-Pin RAD-PAK® flat pack
- Fast access time:
  - 20, 25 and 30 ns maximum times available
- Single 5V + 10% power supply
- Fully static operation
  - No clock or refresh required
- Three state outputs
- TTL compatible inputs and outputs
- Low power:
  - Standby: 60mA (TTL) and 10mA (CMOS)
  - Operation: 180mA (20ns), 170mA (25ns) and 160mA (30ns)

DESCRIPTION:

Maxwell Technologies' 33C108 high-density 1 Megabit SRAM microcircuit features a greater than 100 krad (Si) total dose tolerance. Using Maxwell's radiation-hardened RAD-PAK® packaging technology, the 33C108 realizes a higher density, higher performance, and lower power consumption. Its fully static design eliminates the need for external clocks, while the CMOS circuitry reduces power consumption and provides higher reliability. The 33C108 is equipped with eight common input/output lines, chip select and output enable, allowing for greater system flexibility and eliminating bus contention. The 33C108 features the same advanced 128K x 8 SRAM, high-speed, and low-power demand as the commercial counterpart.

Maxwell Technologies' patented RAD-PAK packaging technology incorporates radiation shielding in the microcircuit package. It eliminates the need for box shielding while providing the required radiation shielding for a lifetime in orbit or space mission. In a GEO orbit, RAD-PAK provides greater than 100 krad (Si) radiation dose tolerance. This product is available with screening up to Class S.

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TABLE 1. PINOUT DESCRIPTION

PIN	SYMBOL	DESCRIPTION
12-5, 27, 26, 23, 25, 4, 28, 3, 31, 2	A0-A16	Address Inputs
29	$\overline{WE}$	Write Enable
22	$\overline{CS}$	Chip Select
24	$\overline{OE}$	Output Enable
13-15, 17-21	I/O 1-I/O 7	Data Inputs/Outputs
32	V_{CC}	Power (+5.0V)
16	V_{SS}	Ground
1, 30	NC	No Connection

TABLE 2. 33C108 ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNIYS
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5	V_{CC} +0.5V	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.5	7.0	V
Power Dissipation	P_D	--	1.0	W
Storage Temperature	T_S	-65	+150	°C
Operating Temperature	T_A	-55	+125	°C
Thermal Impedance	Tjc	--	6.04	°C/W

TABLE 3. 33C108 RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage	V_{CC}	4.5	5.5	V
Ground	V_{SS}	0	0	V
Input High Voltage[1]	V_{IH}	2.2	V_{CC} + 0.5	V
Input Low Voltage[2]	V_{IL}	-0.5	0.8	V

1. V_{IH}(min) = +2.0V AC (pulse width ≤ 10 ns) for I ≤ 20 mA.
2. V_{IL}(min) = -2.0V AC (pulse width ≤ 10 ns) for I ≤ 20 mA.

TABLE 4. 33C108 DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 4.5 to 5.5V; V_{SS} = 0 V; T_A = -55 to +125°C, unless otherwise specified)

PARAMETER	SUBGROUPS	SYMBOL	MIN	MAX	UNITS
Input Leakage Current $V_{IN} = V_{SS}$ to V_{CC}	1, 2, 3	I_{LI}	-2	2	µA
Output Leakage Current $\overline{CS} = V_{IH}$, $V_{OUT} = V_{SS}$ to V_{CC}	1, 2, 3	I_{LO}	-2	2	µA
Output Low Voltage, I_{OL} = 8 mA	1, 2, 3	V_{OL}	--	0.4	V
Output High Voltage, I_{OH} = -4 mA	1, 2, 3	V_{OH}	2.4	--	V
Average Operating Current Min cycle, 100% Duty $\overline{CS}$ =V_{IL}, I_{OUT} = 0mA $V_{IN} = V_{IH}$ or V_{IL}	1, 2, 3	I_{CC}			mA
-20			--	180	
-25			--	170	
-30			--	160	
Standby Power Supply Current $\overline{CS}$= V_{IH}, cycle time ≥ 25ns	1, 2, 3	ISB	--	60	mA
CMOS Standby Current $\overline{CS} \geq V_{CC}$ - 0.2V, f = 0 MHz, $V_{IN} \geq V_{CC}$ - 0.2V or$V_{IN} <$ 0.2V	1, 2, 3	I_{SB1}		10	

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(V_{CC} = 4.5 to 5.5V; V_{SS} = 0 V; T_A = -55 to +125° C, unless otherwise specified)

PARAMETER	SUBGROUPS	SYMBOL	MIN	MAX	UNITS
Input Capacitance V_{IN} = 0V[1]	1, 2, 3	C_{IN}	--	7	pF
Output Capacitance VI/O = 0V[1]	1, 2, 3	C_{OUT}	--	8	pF

1. Guaranteed by design.

TABLE 5. 33C108 FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	MODE	I/O PIN	SUPPLY CURRENT
H	X	X	Not Select	High-Z	ISB, ISB1
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

TABLE 6. 33C108 AC ELECTRICAL CHARACTERISTICS FOR READ CYCLE

(V_{CC} = 4.5 to 5.5V; V_{SS} = 0 V; T_A = -55 to +125°C, unless otherwise specified)

PARAMETER	SUBGROUPS	SYMBOL	MIN	TYP	MAX	UNITS
Read Cycle Time	9, 10, 11	t_{rc}				ns
-20			20	--	--	
-25			25	--	--	
-30			30	--	--	
Address Access Time	9, 10, 11	t_{AA}				ns
-20			--	--	20	
-25			--	--	25	
-30			--	--	30	
Chip Select Access Time	9, 10, 11	t_{CO}				ns
-20			--	--	20	
-25			--	--	25	
-30			--	--	30	
Output Enable to Output Valid	9, 10, 11	t_{OE}				ns
-20			--	--	10	
-25			--	--	12	
-30			--	--	14	
Chip Select to Output in Low-Z[1]	9, 10, 11	t_{LZ}				ns
-20			--	3	--	
-25			--	3	--	
-30			--	3	--	
Output Enable to Output in Low-Z [1]	9, 10, 11	t_{OLZ}				ns
-20			--	0	--	
-25			--	0	--	
-30			--	0	--	
Chip Deselect to Output in High-Z [1]	9, 10, 11	t_{HZ}				ns
-20			--	5	--	
-25			--	6	--	
-30			--	8	--	
Output Disable to Output in High-Z[1]	9, 10, 11	t_{OHZ}				ns
-20			--	5	--	
-25			--	6	--	
-30			--	8	--	

TABLE 6. 33C108 AC ELECTRICAL CHARACTERISTICS FOR READ CYCLE

(V_{CC} = 4.5 to 5.5V; V_{SS} = 0 V; T_A = -55 to +125°C, unless otherwise specified)

PARAMETER	SUBGROUPS	SYMBOL	MIN	TYP	MAX	UNITS
Output Hold from Address Change	9, 10, 11	t_{OH}				ns
-20			--	3	--	
-25			--	5	--	
-30			--	6	--	
Chip Select to Power Up Time[1]	9, 10, 11	t_{PU}				ns
-20			0	0	--	
-25			0	0	--	
-30			0	0	--	
Chip Select to Power Down Time[1]	9, 10, 11	t_{PD}				ns
-20			--	10	--	
-25			--	15	--	
-30			--	20	--	

1. Guaranteed by design.

TABLE 7. 33C108 AC ELECTRICAL CHARACTERISTICS FOR WRITE CYCLE

(V_{CC} = 4.5 to 5.5V; V_{SS} = 0 V; T_A = -55 to +125°C, unless otherwise specified)

PARAMETER	SUBGROUPS	SYMBOL	MIN	TYP	MAX	UNITS
Write Cycle Time	9, 10, 11	t_{WC}				ns
-20			20		--	
-25			25		--	
-30			30		--	
Chip Select to End of Write	9, 10, 11	t_{CW}				ns
-20			14		--	
-25			15		--	
-30			17		--	
Address Setup Time	9, 10, 11	t_{AS}				ns
-20			0		--	
-25			0		--	
-30			0		--	
Address Valid to End of Write	9, 10, 11	t_{AW}				ns
-20			14		--	
-25			15		--	
-30			17		--	
Write Pulse Width(OE High)	9, 10, 11	t_{WP}				ns
-20			14		--	
-25			15		--	
-30			17		--	
Write Pulse Width(OE Low)	9, 10, 11	T_{WP1}				ns
-20			--	20	--	
-25			--	25	--	
-30			--	30	--	

TABLE 7. 33C108 AC ELECTRICAL CHARACTERISTICS FOR WRITE CYCLE

(V_{CC} = 4.5 to 5.5V; V_{SS} = 0 V; T_A = -55 to +125° C, unless otherwise specified)

PARAMETER	SUBGROUPS	SYMBOL	MIN	TYP	MAX	UNITS
Write Recovery Time	9, 10, 11	t_{WR}				ns
-20			0		--	
-25			0		--	
-30			0		--	
Write to Output in High-Z [1]	9, 10, 11	t_{WHZ}				ns
-20			--	5	--	
-25			--	5	--	
-30			--	6	--	
Data to Write Time Overlap	9, 10, 11	t_{DW}				ns
-20			9		--	
-25			10		--	
-30			11		--	
End Write to Output Low-Z[1]	9, 10, 11	t_{OW}				ns
-20			--	6	--	
-25			--	7	--	
-30			--	8	--	
Data Hold from Write Time	9, 10, 11	t_{DH}				ns
-20			0		--	
-25			0		--	
-30			0		--	

1. Guaranteed by design.

FIGURE 1. TIMING WAVEFORM OF READ CYCLE(1)

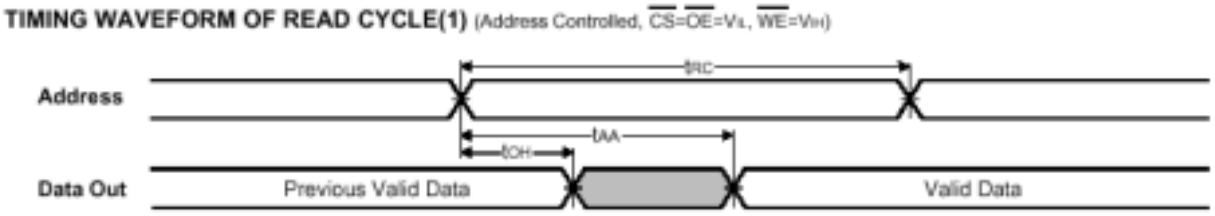
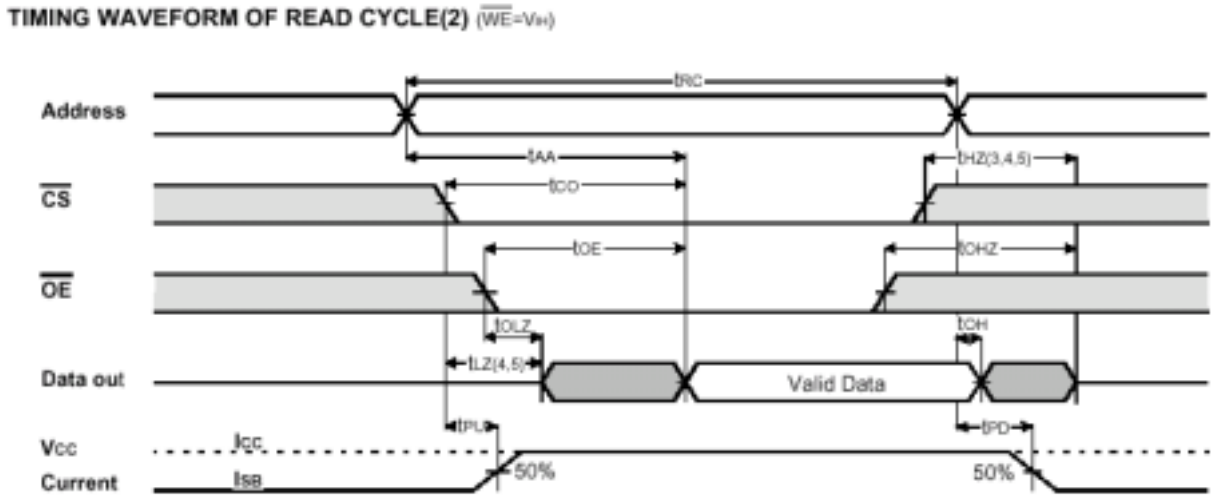


FIGURE 2. TIMING WAVEFORM OF READ CYCLE (2)



Read Cycle Notes:

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced form the last valid address to the first transition address.
3. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL} levels.
4. At any given temperature and voltage condition, $t_{HZ(max)}$ is less than $t_{LZ(min)}$ both for a given device and from device to device.
5. Transition is measured + 200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with CS = V_{IL}.
7. Address valid prior to coincident with CS transition low.
8. For common I/O applications, minimization or elimination of bus contention condition is necessary during read and write cycle.

FIGURE 3. TIMING WAVEFORM OF WRITE CYCLE(1)

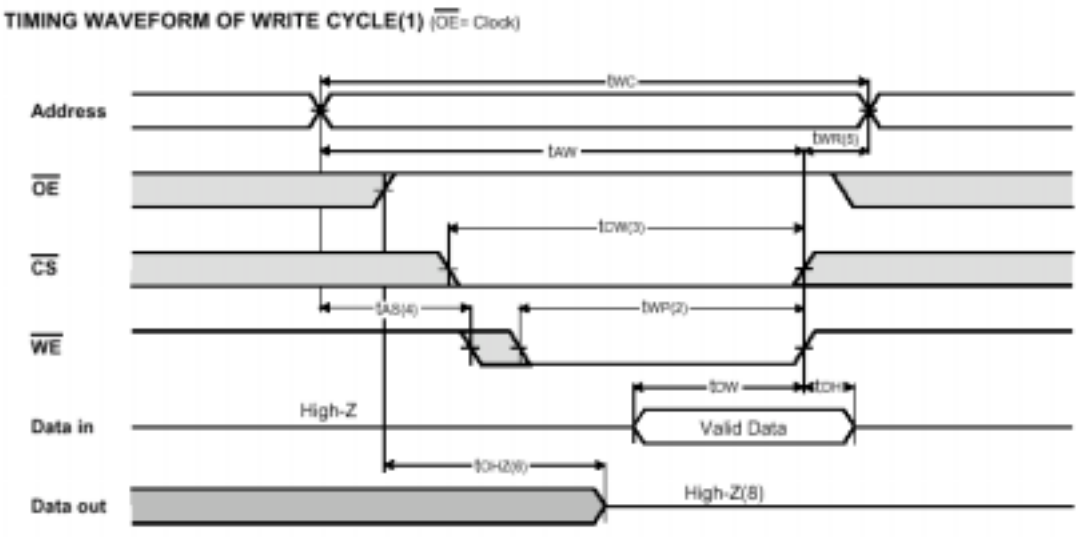


FIGURE 4. TIMING WAVEFORM OF WRITE CYCLE(2)

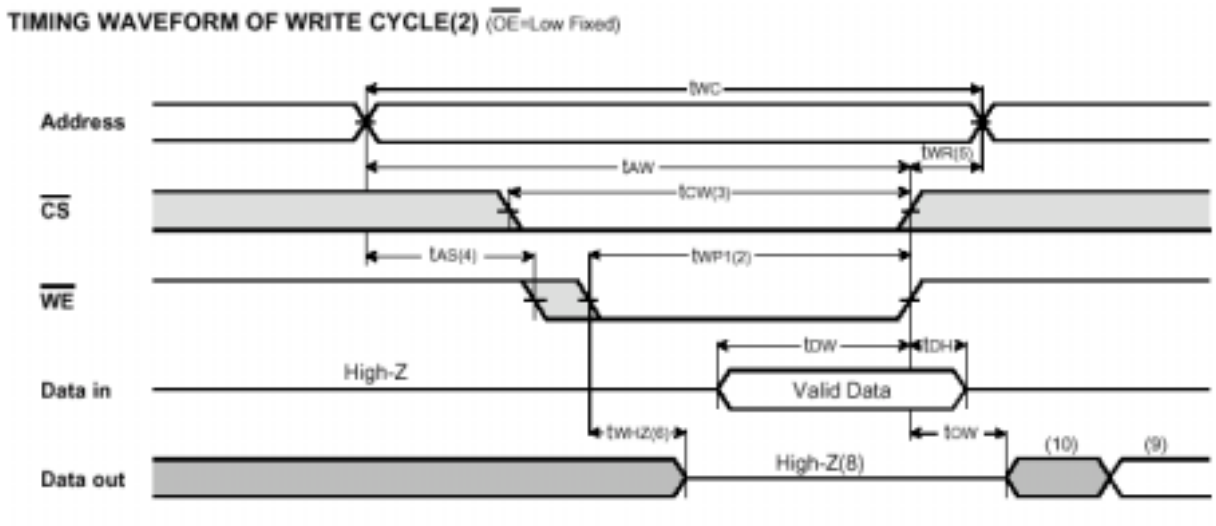
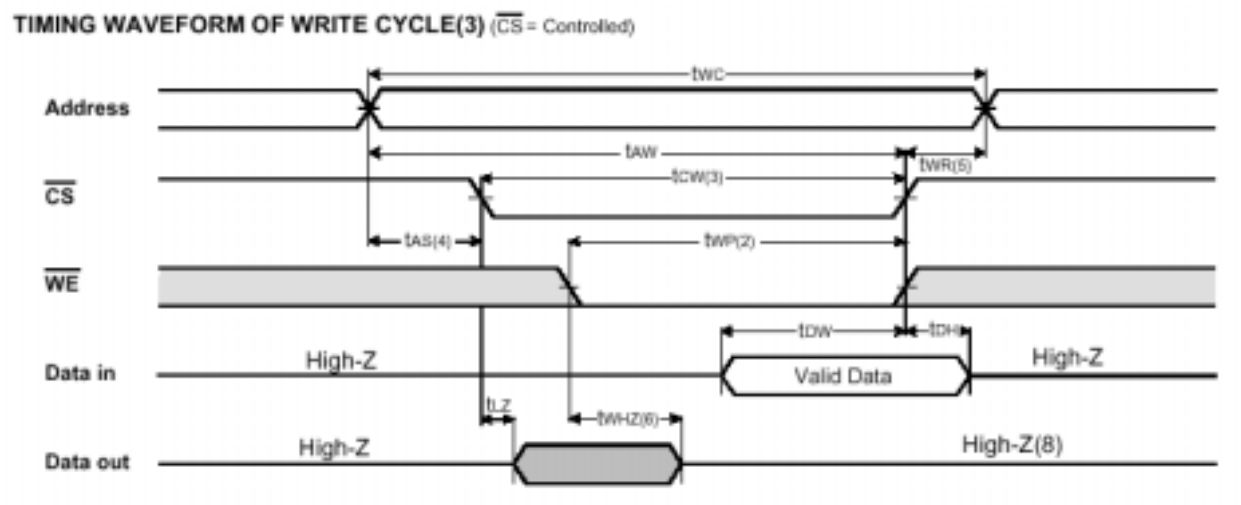


FIGURE 5. TIMING WAVEFORM OF WRITE CYCLE (3)



WRITE CYCLE NOTE:

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ going low and $\overline{WE}$ going low: A write ends at the earliest transition among $\overline{CS}$ going high and $\overline{WE}$ going high. t_{wp} is measured from beginning of write to the end of write.
3. t_{cw} is measured from the later of $\overline{CS}$ going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured form the end of write to the address change. TWR applied in case a write ends as $\overline{CS}$, or $\overline{WR}$ going high.
6. If $\overline{OE}$, $\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. $\overline{IC}$ $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. D_{OUT} is the read data of the new address.
10. When $\overline{CS}$ is low: I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FIGURE 6. SRAM HEAVY ION CROSS SECTION

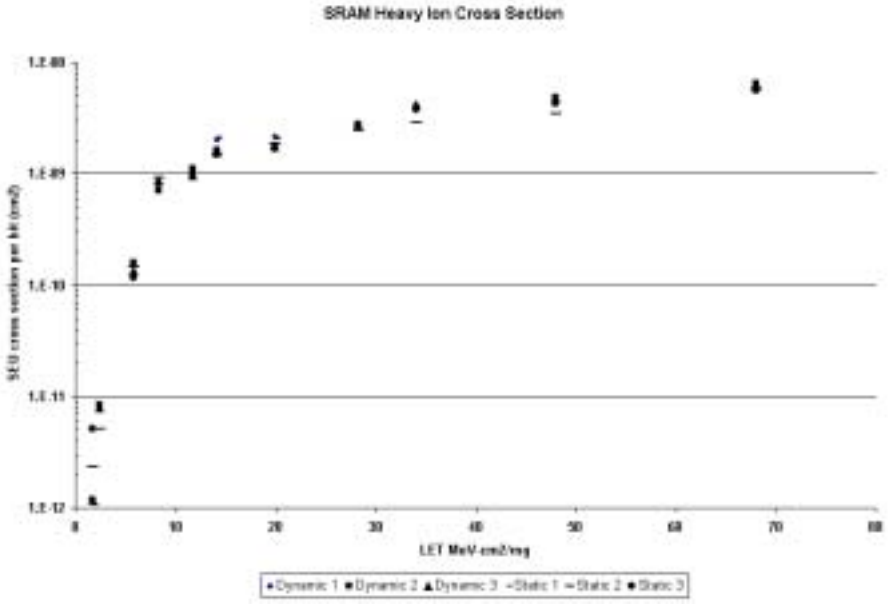
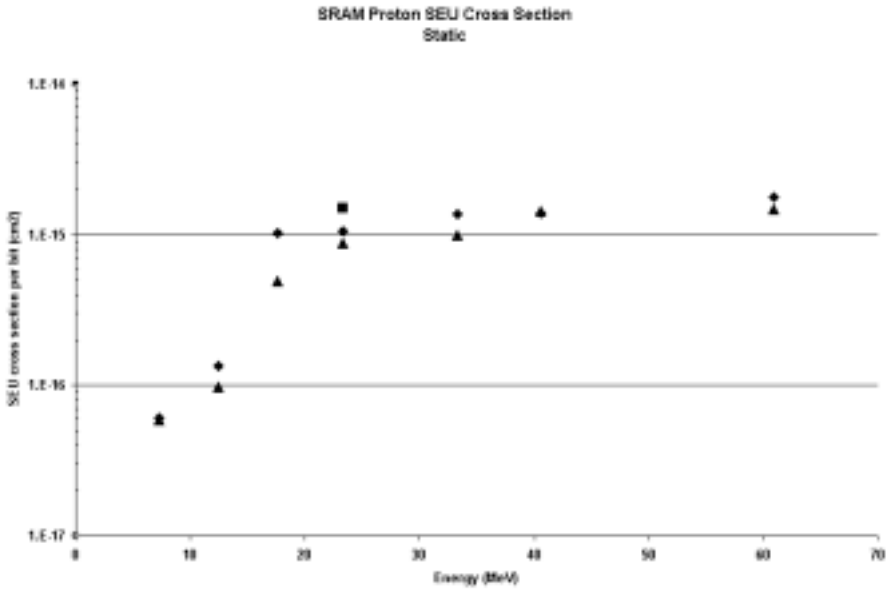
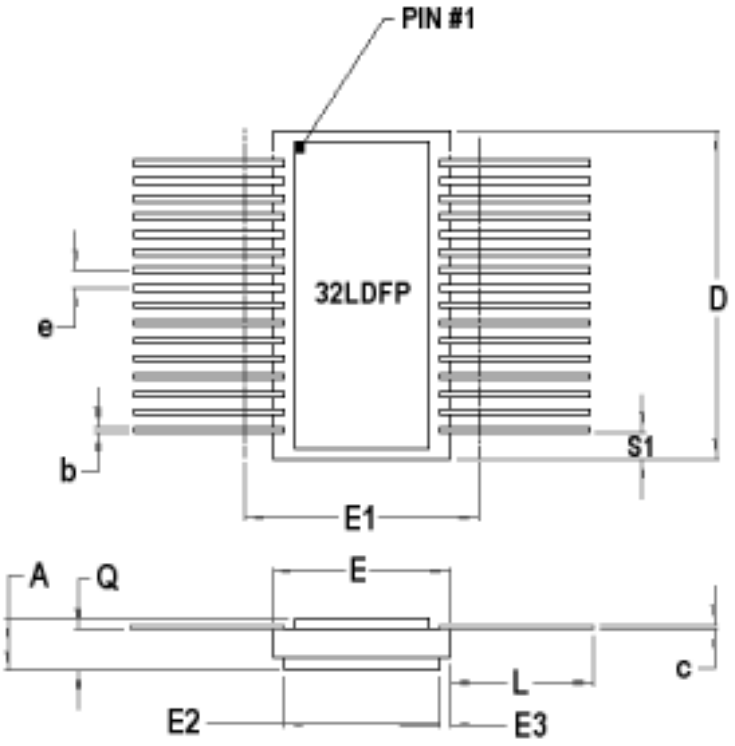


FIGURE 7. SRAM PROTON SEU CROSS SECTION STATIC





32 PIN RAD-PAK® FLAT PACKAGE

SYMBOL	DIMENSION		
	MIN	NOM	MAX
A	0.120	0.135	0.155
b	0.013	0.015	0.020
c	0.008	0.010	0.012
D	--	0.930	0.940
E	0.635	0.645	0.655
E1	--	--	0.690
E2	0.550	0.565	--
E3	0.030	0.040	--
e	0.050 BSC		
L	0.390	0.400	0.410
Q	0.026	0.098	--
S1	0.005	0.082	--
N	32		

F32-06

Note: All dimensions in inches

Important Notice:

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