4Kx36 Synchronous FIFO MODULE *ADVANCED**

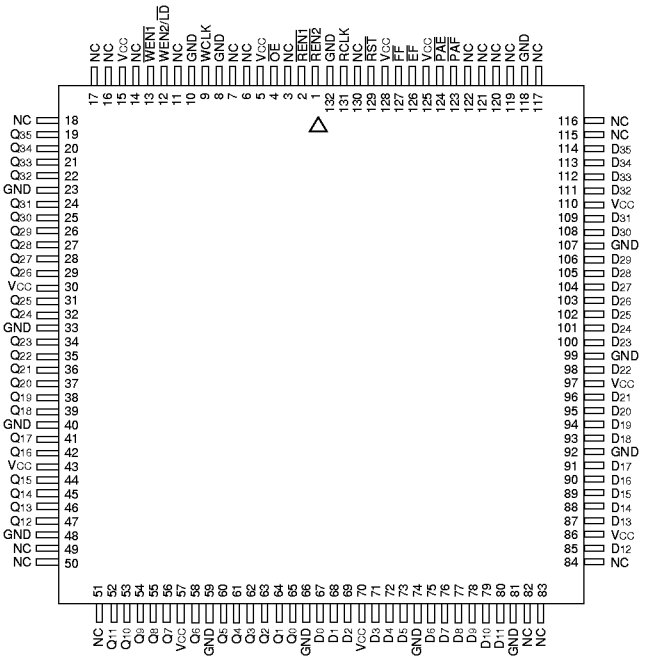
FEATURES

- High Speed Operation: 66.7, 40, 28.6MHz
- Packaging:
  - 132-pin Hermetic Ceramic Quad Flatpack, CQFP, 24mm (0.950") sq.
- Synchronous First-In First-Out (FIFO) Buffer Memory
- Fully Asynchronous and Simultaneous Read and Write
- Status Flags: Empty, Full, and Programmable Almost Empty and Almost Full.
- 5V ± 10% Power Supply
- Industrial and Military Temperature Ranges
- Low Power CMOS
- TTL Compatible
- Built-in Decoupling Caps and Multiple Ground Pins for Low Noise Operation

** This data sheet describes a product that may or may not be under development and is subject to change or cancellation without notice.*

FIG. 1 PIN CONFIGURATION FOR WTP4K36-XGX

TOP VIEW



PIN DESCRIPTION

$D_{0\text{-}35}$	Data Inputs
$Q_{0\text{-}35}$	Data Outputs
$\overline{RST}$	Reset Input
$\overline{WEN1}$	Write Enable 1
WEN2/$\overline{LD}$	Write Enable 2/Load
$\overline{REN1}$, $\overline{REN2}$	Read Enables
WCLK	Write Clock Input
RCLK	Read Clock Input
$\overline{OE}$	Output Enable
$\overline{FF}$	Full Flag Output
$\overline{EF}$	Empty Flag Output
$\overline{PAE}$	Programmable Almost Empty Flag Output
$\overline{PAF}$	Programmable Almost Full Flag Output
Vcc	Power Supply
GND	Ground
NC	Not Connected

FUNCTIONAL DESCRIPTION

- The WTP4K36-XGX is high-speed low power, First-In First-Out (FIFO) memory with clock read and write. Programmable features include Almost Full/Almost Empty Flags. This device provides solutions for a wide variety of data buffering needs, including high-speed data acquisition, multiprocessor interfaces, and communication buffering.
- The FIFO has 36-bit input and output ports that are controlled by separate clocks and enable signals. The input port is controlled by a free-running clock (WCLK) and two Write-Enable pins ($\overline{WEN1}$, WEN2/$\overline{LD}$).
- When $\overline{WEN1}$ is low and WEN2/$\overline{LD}$ is high, data is written into the FIFO on the rising edge of the WCLK signal. While $\overline{WEN1}$, WEN2/$\overline{LD}$ is held active, data is continually written into the FIFO on each WCLK cycle. The output port is controlled in a similar manner by a free-running read clock (RCLK) and two Read-Enable pins ($\overline{REN1}$, $\overline{REN2}$). In addition, the device has an Output Enable pin ($\overline{OE}$). The Read (RCLK) and Write (WCLK) clocks may be tied together for single-clock operation or the two clocks may be run independently for asynchronous read/write operations.
- Depth expansion is possible using one Enable Input for system control, while the other enable is controlled by expansion logic to direct the flow of data.
- The FIFO provides four status pins: Empty, Full, Almost Empty, and Almost Full. The Almost Empty/Almost Full Flags are programmable to single word granularity. The programmable flags default to Empty - 7 and Full - 7.

  The flags are synchronous. They change state relative to either the Read Clock (RCLK) or the Write Clock (WCLK). When entering or exiting the Empty and Almost Empty states, the flags are updated exclusively by RCLK. The flags denoting Almost Full and Full states are updated exclusively by WCLK. The synchronous flag architecture guarantees that the flags maintain their status for at least one cycle.

SIGNAL DESCRIPTIONS

DATA INPUT (D_{0-35})

Data Inputs for 36-bit wide data.

DATA OUTPUT (Q_{0-35})

Data Outputs for 36-bit wide data.

RESET ($\overline{RST}$)

Resets device to empty condition. A reset is required before an initial read or write operation after power-up.

WRITE ENABLE 1 ($\overline{WEN1}$)

The only write enable when device is configured to have programmable flags. Data is written on a Low-to-High transition of WCLK when $\overline{WEN1}$ is asserted and $\overline{FF}$ is High. If FIFO is configured to have two write enables, data is written in Low-to-High transition of WCLK when $\overline{WEN1}$ is Low and WEN2/$\overline{LD}$ and $\overline{FF}$ are High.

WRITE ENABLE 2 (WEN2/$\overline{LD}$)

If High at reset, this pin operates as a second write enable. If Low at reset, this pin operates as a control to write or read the programmable flag offsets. $\overline{WEN1}$ must be Low and WEN2 must be High to write data into the FIFO. Data will not be written into the FIFO if the FF is Low. If the FIFO is configured to have programmable flags, WEN2/$\overline{LD}$ is held Low to write or read the programmable flag offsets.

READ ENABLE INPUTS ($\overline{REN1}$, $\overline{REN2}$)

Enables the device for Read Operation.

WRITE CLOCK (WCLK)

The rising edge clocks data into the FIFO when $\overline{WEN1}$ is Low and WEN2/$\overline{LD}$ is High and the FIFO is not Full. When $\overline{LD}$ is asserted, WCLK writes data into the programmable flag-off-set register.

READ CLOCK (RCLK)

The rising edge clocks data out of the FIFO when $\overline{REN1}$ and $\overline{REN2}$ are Low and the FIFO is not Empty. When WEN2/$\overline{LD}$ is Low, RCLK reads data out of the programmable flag-offset register.

EMPTY FLAG ($\overline{EF}$)

When Empty Flag ($\overline{EF}$) is Low, the FIFO is empty. $\overline{EF}$ is synchronized to RCLK.

FULL FLAG ($\overline{FF}$)

When Full Flag ($\overline{FF}$) is Low, the FIFO is full. $\overline{FF}$ is synchronized to WCLK.

PROGRAMMABLE ALMOST EMPTY ($\overline{PAE}$)

When Programmable Almost Empty ($\overline{PAE}$) is Low, the FIFO is almost empty based on the almost empty offset value programmed into the FIFO.

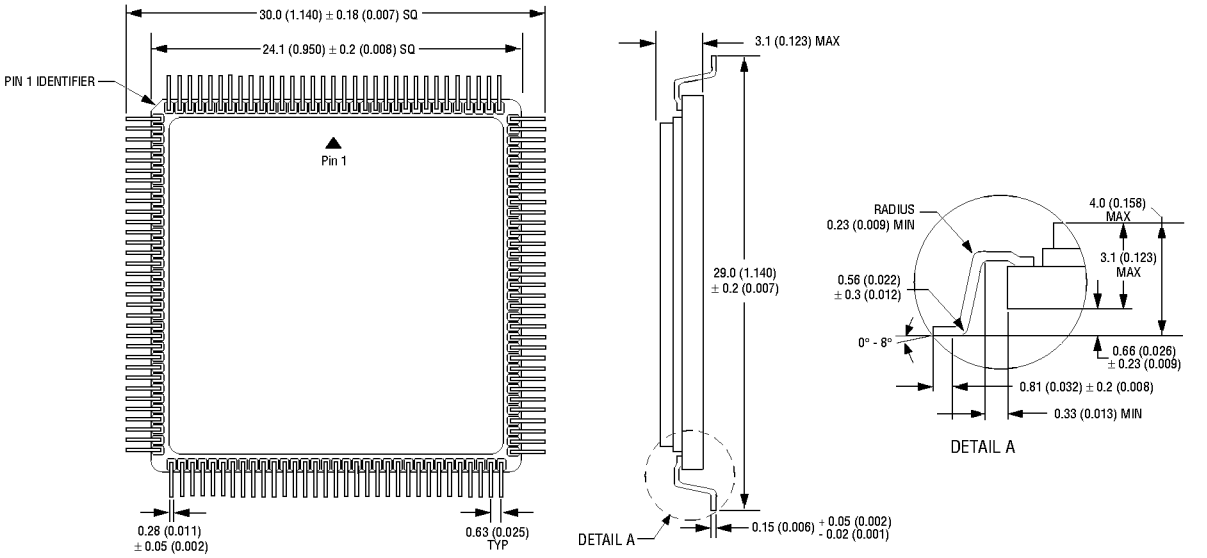
PROGRAMMABLE ALMOST FULL ($\overline{PAF}$)

When Programmable Almost Full ($\overline{PAF}$) is Low, the FIFO is almost full based on the almost full offset value programmed into the FIFO.

OUTPUT ENABLE ($\overline{OE}$)

When Output Enable ($\overline{OE}$) is Low, the FIFO's data outputs drive the bus to which they are connected. If $\overline{OE}$ is High, the FIFO's outputs are in High Z (high-impedance) state.

PACKAGE 505: 132 PIN, CERAMIC QUAD FLAT PACK, CQFP (G)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION

W TP 4K 36 - XX G X X

LEAD FINISH:
Blank = Gold plated leads
A = Solder dip leads

DEVICE GRADE:
M = Military -55°C to +125°C
I = Industrial -40°C to +85°C

PACKAGE TYPE:
G = 24mm sq,132-pin Ceramic Quad Flatpack, CQFP (Package 505)

ACCESS TIME (ns)

ORGANIZATION, 4Kx36

Synchronous FIFO

WHITE MICROELECTRONICS